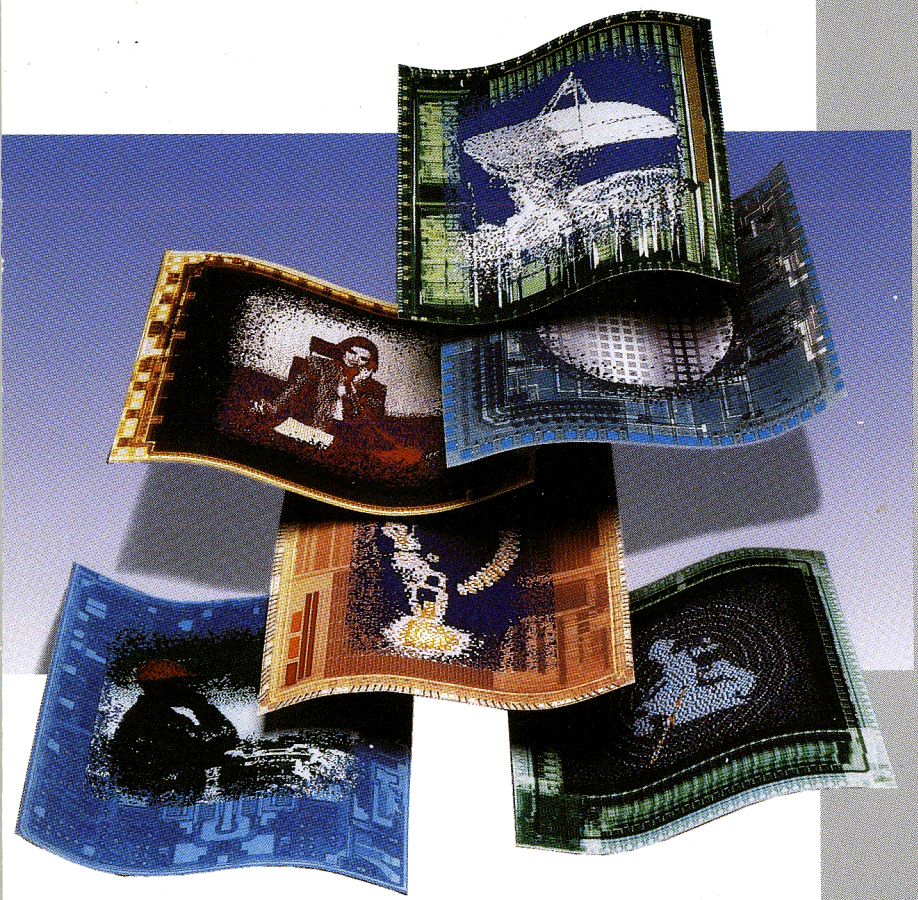
# Data Converters & Datacoms

July 1991

## IC Handbook



GEC PLESSEY

SEMICONDUCTORS

# DATA CONVERSION and DATACOMS

## IC Handbook

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# Foreword

This new Data Conversion and Datacoms IC Handbook directly succeeds our January 1989 Data Converters and Voltage References IC Handbook. As such, it features our world-renowned ultra high speed ADCs and DACs – including the SP98608 450MHz 8-bit DAC and the SP97508 110MHz 8-bit ADC. Also included is the GPS range of sub-nanosecond comparators, which set new standards in performance and supersede the previous industry standard SP96XX series.

Featured again in this handbook is the broad range of microprocessor compatible ADCs and DACs manufactured on our low cost CDI bipolar process. The compact nature of these designs allows for higher levels of integration and, reflecting customer demand, GPS already offers a number of dual DACs and ADC/DAC combinations. The CDI process also supports an extensive portfolio of Voltage Reference ICs with flagship parts like the SR25D, a 2.50V reference in an ultra-miniature SOT-23 surface mount package. There now 1.23V and 5.00V versions, also in the SOT-23 package, as well as references in the more conventional metal can, TO-92 and in 8-lead miniature plastic surface mount DIL.

GPS has recently accelerated its development of video bandwidth converters to target Imaging and Graphics applications. This includes designs which are pin-for-pin replacements for industry standard devices. Already available and featured in this handbook are the VP1058 25MHz 8-bit Video ADC and the VP101 Triple 8-bit 50MHz Graphics DAC. Further graphics DACs and designs incorporating palette memories are scheduled for launch in the next 12 months and will be featured in supplements to this handbook (Please enquire for the latest information).

As well as updating the previous Data Converters and Voltage References IC Handbook, this edition incorporates GPS Datacoms products. These devices are closely aligned to to data conversion requirements and are common to many applications. We provide several essential 'glue' circuits, including some ECLIII devices and a range of 32 and 64-word FIFO memories. Computer and Telecoms networking applications are supported by a number of specialised devices: our SP9970 and SP9930 provide critical clock recovery and multiplex/demultiplex capabilities for FDDI (Fibre Distributed Data Interface) Local Area Networks, while our 50MB/s chipset (SP9960, SL9901 and SP9921) integrates all the interface requirements for a self-contained point-to-point serial data link over a fibre optic cable.

Once again GEC Plessey Semiconductors can claim to offer 'one-stop shopping' for all your data conversion needs but as always you, our customers, determine our next developments so if you can't find a product to solve your problem then let us know.

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# Product index - Data Converters

## High Speed DACs

| Type No. | Function | Minimum clock rate (MHz) | DAC max. rise time (ns) (10% to 90%) | Process | Page |
|---|---|---|---|---|---|
| **MA6670** | 8-bit flash DAC | 35 | 2.5 | CMOS | 1-15 |
| **MA6672** | 10-bit flash DAC | 35 | 2.5 | CMOS | 1-19 |
| **MV95308** | 8-bit video DAC | 30 | 6.0 | CMOS | 1-23 |
| **MV95338** | Triple 8-bit video DAC | 30 | 9.0 | CMOS | 1-28 |
| **MV95408** | 8-bit video DAC | 50 | 5.5 | CMOS | 1-35 |
| **SP98608** | 8-bit latched multiplying DAC | 450 | 0.8 | Bipolar | 1-108 |
| **VP101** | Triple 8-bit video DAC | 30/50 | 9.0 | CMOS | 1-113 |
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| **ZN454** | Triple 4-bit video DAC | 100 | 5.0 | Bipolar | 1-244 |
| **ZN515** | 8-bit video DAC | 100 | 5.0 | Bipolar | 1-295 |

## Advanced Function DACs

| Type No. | Function | Linearity error (LSB) | Settling time ($\mu$s) | On-chip reference | Special features | Page |
|---|---|---|---|---|---|---|
| **ZN425** | 8-bit DAC/ADC | ±0.5 | 1.0 | Yes | 8-bit counter | 1-127 |
| **ZN426** | 8-bit DAC | ±0.5 | 1.0 | Yes | Low cost | 1-134 |
| **ZN428** | 8-bit microprocessor-compatible DAC | ±0.5 | 0.8 | Yes | Data latch | 1-155 |
| **ZN429** | 8-bit DAC | ±0.5 | 1.0 | No | Low cost | 1-164 |
| **ZN435** | 8-bit multifunction DAC/ADC | ±0.5 | 0.8 | Yes | Up/down counter | 1-188 |
| **ZN508** | Dual 8-bit microprocessor-compatible DAC | ±0.5, ±1.0 | 0.8 | Yes | Separate $V_{REF}$ inputs and data latches for each DAC | 1-275 |
| **ZN525** | 8-bit multifunction DAC/ADC | ±0.5 | 0.8 | Yes | Up/down counter Enhanced control circuitry | 1-296 |
| **ZN558** | 8-bit microprocessor-compatible DAC | ±0.5 | 0.8 | Yes | Data latch | 1-314 |
| **ZN7528** | Dual 8-bit DAC | ±0.5 | 1.0 | No | Close DAC-to-DAC matching | 1-332 |

## RAM DAC

| Type No. | Function | Minimum clock rate (MHz) | Linearity error (LSB) | Overlay | Process | Page |
|---|---|---|---|---|---|---|
| **ZN455** | Triple 4-bit video RAM DAC | 100 | ±0.25 | 16×12 | Bipolar | 1-251 |

## Advanced Function ADCs

| Type No. | Function | Linearity options (LSB) | Conversion time ($\mu$s) | On-chip clock | Special features | Page |
|---|---|---|---|---|---|---|
| **ZN427** | 8-bit microprocessor-compatible ADC | ±0.5 | 10 | No | Three-state data outputs | 1-139 |
| **ZN432** | 10-bit ADC | ±0.5, ±1.0 | 20 | No | Serial and parallel data outputs | 1-172 |
| **ZN433** | 10-bit tracking ADC | ±0.5 | 1(1) | No | Serial and parallel data outputs | 1-180 |
| **ZN439** | 8-bit microprocessor-compatible ADC | ±0.25, ±5, ±1.0 | 5 | Yes | Advanced microprocessor interface with double-buffered latches | 1-201 |
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| **ZN448** | 8-bit microprocessor-compatible ADC | ±0.5 | 9 | Yes | Three-state data outputs | 1-227 |
| **ZN449** | 8-bit microprocessor-compatible ADC | ±1.0 | 9 | Yes | Three-state data outputs, low cost | 1-227 |
| **ZN501** | 10-bit microprocessor-compatible ADC | ±0.5 | 20 | No | Three-state data outputs | 1-261 |
| **ZN509** | 8-bit ADC with serial output | ±0.5 | 8 | Yes | Single supply, low cost | 1-284 |
| **ZN682** | 2-channel 8-bit microprocessor ADC | ±0.5 | 8 | Yes | Continuous conversion on specified channel | 1-325 |
| **ZN683** | 2-channel 8-bit microprocessor ADC | ±1.0 | 8 | Yes | Continuous conversion on specified channel | 1-325 |
| **ZN684** | 4-channel 8-bit microprocessor ADC | ±0.5 | 8 | Yes | Continuous conversion on specified channel | 1-325 |
| **ZN685** | 4-channel 8-bit microprocessor ADC | ±1.0 | 8 | Yes | Continuous conversion on specified channel | 1-325 |
| **ZN688** | 8-channel 8-bit microprocessor ADC | ±0.5 | 8 | Yes | Continuous conversion on specified channel | 1-325 |
| **ZN689** | 8-channel 8-bit microprocessor ADC | ±1.0 | 8 | Yes | Continuous conversion on specified channel | 1-325 |

NOTES
1. Assumes continuous tracking
2. All Advanced Function ADCs have on-chip reference

# Product index - Data Converters (continued)

## High Speed ADCs

| Type No. | Function | Minimum clock rate (MHz) | Process | Page |
|---|---|---|---|---|
| **MA6560** | 8-bit flash ADC | 20 | CMOS | 1-3 |
| **MA6561** | Radiation hard 8-bit flash ADC | 50 | CMOS Silicon on Sapphire | 1-9 |
| **SP94308** | 8-bit video system ADC | 20 | Bipolar | 1-80 |
| **SP973T8** | 8-bit flash ADC (TTL/CMOS outputs) | 30 | Bipolar | 1-86 |
| **SP97504** | 4-bit expandable ADC (replaces SP9754) | 110 | Bipolar | 1-92 |
| **SP97506** | 6-bit wide input bandwidth ADC (250MHz -3dB) | 110 | Bipolar | 1-96 |
| **SP97508** | 8-bit flash ADC | 110 | Bipolar | 1-101 |
| **VP1058** | 8-bit video ADC | 25 | Bipolar | 1-121 |

## ADC-DAC Combinations

| Type No. | Function | Linearity options (LSB) | ADC conversion time ($\mu$s) | DAC settling time ($\mu$s) | Special features | Page |
|---|---|---|---|---|---|---|
| **ZN540** | 8-bit microprocessor-compatible ADC with dual DAC | ±0.5 | 5 | 1 | Programmable clock prescaler, double-buffered latches, on-chip reference | 1-304 |
| **ZN541** | 8-bit microprocessor-compatible ADC with dual DAC | ±1.0 | 5 | 1 | Programmable clock prescaler, double-buffered latches, on-chip reference | 1-304 |

## ADC Support

| Type No. | Function | Supply voltage (V) | Process | Page |
|---|---|---|---|---|
| **SL9999** | 400MHz ADC driver/operational amplifier | +9 to −15<br>− 5 to −15 | Bipolar | 1-40 |
| **SP92701** | Single sub-nanosecond ECL line receiver and driver | − 5.2 | Bipolar | 1-48 |

## High speed comparators

| Type No. | Function | Supply voltage (V) | Input voltage (V) | Offset voltage (mV) | Response time (ps) | Setup time (ps, typ.) | Process | Page |
|---|---|---|---|---|---|---|---|---|
| **SP93802** | Dual comparator (1) | +5, −5.2 | ±4 | ±5 | 950 | 150 | Bipolar | 1-51 |
| **SP93804** | Quad comparator(1) | +5, −5.2 | ±4 | ±5 | 950 | 150 | Bipolar | 1-62 |
| **SP93808** | Octal comparator(1) | +5, −5.2 | ±4 | ±5 | 950 | 150 | Bipolar | 1-71 |

NOTE 1. Includes glitch capture

# Product index - Voltage References

## Micropower Fixed Voltage References

| Type No. | Nominal voltage (V) | Guaranteed knee current (μA) | Slope resistance (Ω) | Maximum temperature coefficient (ppm/°C) | Operating temperature range (°C) | Page |
|---|---|---|---|---|---|---|
| **REF12D** | 1.26 | 90 | 4.0 | 80 | – 40 to + 85 | 2-3 |
| **REF12Z** | 1.26 | 90 | 4.0 | 56 | – 40 to + 85 | 2-3 |
| **REF25D** | 2.50 | 60 | 2.0 | 80 | – 40 to + 85 | 2-9 |
| **REF25Z** | 2.50 | 60 | 2.0 | 110 | – 40 to + 85 | 2-9 |
| **REF2525Z** | 2.50 | 60 | 2.0 | 25 | – 40 to + 85 | 2-15 |
| **REF50D** | 5.00 | 60 | 3.5 | 80 | – 40 to + 85 | 2-21 |
| **REF50Z** | 5.00 | 60 | 3.5 | 110 | – 40 to + 85 | 2-21 |

## SOT-23 Micropower Bandgap Voltage References

| Type No. | Nominal voltage (V) | Guaranteed knee current (μA) | Slope resistance (Ω) | Maximum temperature coefficient (ppm/°C) | Operating temperature range (°C) | Page |
|---|---|---|---|---|---|---|
| **SR12D** | 1.23 | 90 | 2.5 | 125 | – 40 to + 85 | 2-27 |
| **SR25D** | 2.50 | 80 | 2.0 | 150 | – 40 to + 85 | 2-30 |
| **SR50D** | 5.00 | 80 | 2.0 | 220 | – 40 to + 85 | 2-33 |

## Fixed Voltage References

| Type No. | Nominal voltage (V) | Reference current (mA) Min. | Reference current (mA) Max. | Slope resistance (Ω) | Maximum temperature coefficient (ppm/°C) | Operating temperature range (°C) | Page |
|---|---|---|---|---|---|---|---|
| **ZN404** | 2.45 | 2 | 120 | 0.4 | 145 | 0 to + 70 | 2-37 |
| **ZN404D** | 2.45 | 2.0 | 120 | 0.4 | 145 | – 20 to + 70 | 2-37 |
| **ZN423** | 1.26 | 1.5 | 12 | 1.5 | 101 | – 55 to + 125 | 2-41 |
| **ZN423Z** | 1.26 | 1.5 | 12 | 1.5 | 101 | 0 to + 70 | 2-41 |
| **ZN458** | 2.45 | 2 | 120 | 0.2 | 99 | – 20 to + 70 | 2-46 |
| **ZN458A** | 2.45 | 2 | 120 | 0.2 | 49 | – 20 to + 70 | 2-46 |
| **ZN458B** | 2.45 | 2 | 120 | 0.2 | 29 | – 20 to + 70 | 2-46 |

# Product index - Voltage References (continued)

## Low Power Trimmable Voltage References

| Type No. | Nominal voltage (V) | Tol. (%) | Trim range (%) | Reference current (mA) Min. | Reference current (mA) Max. | Temp. coeff. (ppm/°C) | Slope resistance (Ω) | Operating temperature range (°C) | Page |
|---|---|---|---|---|---|---|---|---|---|
| **ZNREF025 A1** | 2.50 | 1 | ±5 | 0.15 | 10.0 | 50 | 2 | – 55 to + 125 | 2-50 |
| **ZNREF025 C1** | | 1 | | | | | | – 40 to + 85 | |
| **ZNREF025 C2** | | 2 | | | | | | – 40 to + 85 | |
| **ZNREF040 A1** | 4.01 | 1 | ±5 | 0.15 | 75.0 | 50 | 3 | – 55 to + 125 | 2-54 |
| **ZNREF040 C1** | | 1 | | | | | | – 40 to + 85 | |
| **ZNREF040 C2** | | 2 | | | | | | – 40 to + 85 | |
| **ZNREF050 A1** | 4.90 | 1 | ±5 | 0.15 | 60.0 | 50 | 2 | – 55 to + 125 | 2-58 |
| **ZNREF050 C1** | | 1 | | | | | | – 40 to + 85 | |
| **ZNREF050 C2** | | 2 | | | | | | – 40 to + 85 | |
| **ZNREF062 A1** | 6.17 | 1 | ±5 | 0.15 | 50.0 | 50 | 3 | – 50 to + 110 | 2-62 |
| **ZNREF062 C1** | | 1 | | | | | | – 40 to + 85 | |
| **ZNREF062 C2** | | 2 | | | | | | – 40 to + 85 | |
| **ZNREF100 A1** | 9.80 | 1 | ±2.5 | 0.15 | 50.0 | 50 | 4 | – 55 to + 125 | 2-66 |
| **ZNREF100 C1** | | 1 | | | | | | – 40 to + 85 | |
| **ZNREF100 C2** | | 2 | | | | | | – 40 to + 85 | |

# Product index - Networking and Communications

## Cascadable First In/First Out Memories, TTL/CMOS Compatible

| Type No. | Function | Min. clock frequency (MHz) | Supply voltage (V) | Process | Page |
|---|---|---|---|---|---|
| **MJ2812** | 32 × 8 bits, with output enable | 2 | 5 | NMOS | 3-3 |
| **MJ2813** | 32 × 9 bits, with output enable | 2 | 5 | NMOS | 3-3 |
| **MJ2841** | 64 × 4 bits | 1.75 | 5 | NMOS | 3-8 |
| **MV66030-25** | 64 × 9 bits, with tristate outputs and output enable | 25 | 5 | CMOS | 3-12 |
| **MV66030-10** | 64 × 9 bits, with tristate outputs and output enable | 10 | 5 | CMOS | 3-12 |
| **MV66401-25** | 64 × 4 bits, with bistate outputs and output enable | 25 | 5 | CMOS | 3-19 |
| **MV66401-10** | 64 × 4 bits, with bistate outputs and output enable | 10 | 5 | CMOS | 3-19 |
| **MV66402-25** | 64 × 5 bits, with bistate outputs and output enable | 25 | 5 | CMOS | 3-19 |
| **MV66402-10** | 64 × 5 bits, with bistate outputs and output enable | 10 | 5 | CMOS | 3-19 |
| **MV66403-25** | 64 × 4 bits, with tristate outputs and output enable | 25 | 5 | CMOS | 3-19 |
| **MV66403-10** | 64 × 4 bits, with tristate outputs and output enable | 10 | 5 | CMOS | 3-19 |
| **MV66404-25** | 64 × 5 bits, with tristate outputs and output enable | 25 | 5 | CMOS | 3-19 |
| **MV66404-10** | 64 × 5 bits, with tristate outputs and output enable | 10 | 5 | CMOS | 3-19 |

## Standard ECL

| Type No. | Function | Supply voltage (V) | Frequency (MHz) | Power (mW) | Page |
|---|---|---|---|---|---|
| **SP1648** | Voltage controlled oscillator | +5 or– 5.2 | 225 | 150 | 3-26 |
| **SP1658** | Voltage controlled multivibrator | – 5.2 | 155 | 130 | 3-32 |

## Very Fast ECL

| Type No. | Function | Supply voltage (V) | Speed (min.) | Page |
|---|---|---|---|---|
| **SP16F60** | Dual 4-input OR/NOR gate (pin/function compatible with MC1660) | – 5.2 | $t_{PD}$ = 0.55ns | 3-36 |
| **SP9131** | Dual D-type flip-flop (ultra fast version of MC10131) | – 5.2 | 520MHz | 3-38 |

## Fibre Optic Links/LANs

| Type No. | Function | Frequency | Supply voltage (V) | Process | Page |
|---|---|---|---|---|---|
| **SL9901** | Transimpedance amplifier | 50MHz | +5 or– 5.2 | Bipolar | 3-42 |
| **SP9921** | Manchester biphase-mark decoder | 50MB/s | +5 or– 5.2 | Bipolar | 3-45 |
| **SP9930** | FDDI clock recovery and de-serialising receiver | 125MB/s | +5 and– 5.2 | Bipolar | 3-52 |
| **SP9944E** | Data regenerator | 200MB/s (NRZ) | +5 or– 5.2 | Bipolar | 3-61 |
| **SP9960** | Manchester biphase-mark encoder and LED driver | 50MB/s | +5 or– 5.2 | Bipolar | 3-67 |
| **SP9970** | FDDI parallel to serial line driver | 125MB/s | +5 and– 5.2 | Bipolar | 3-72 |

# Product List-Alpha Numeric

## Section 1-Data Converters

## Section 1-Data Converters (continued)



## Section 2-Voltage References



## Section 3-Networking and Communications

# Section 3-Networking and Communications (continued)

# The Quality Concept

Quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes (followed by strict control and on-going assessment) that quality products will be produced.

All designs conform to standard layout rules, all processes are thoroughly evaluated and all new piece part designs and suppliers are investigated before authorisation for production use.

The same basic procedures are used on all products up to and including device packing. It is only then that extra operations are performed for certain customers in terms of lot qualification or release procedure.

By working to common procedures, all users benefit; the high reliability user gains the advantage of scale (hence improving the confidence factor in the quality achieved), while the volume user gains from the benefits of basic high reliability design concepts.

GEC Plessey Semiconductors (GPS) have the following factory approvals:

**BS9000**
**AQAP1**
**BS9450** (Capability Approval)
**MIL-STD-883C Class B** (In conformance with the requirements of MIL-STD-883C Notice 11, paragraph 1.2.1)
**DESC** (Department of Electronics Supply Center - device approvals)

# Screening

Different screening procedures are carried out by GPS; a brief description of the differences involved are set out in Tables 1 and 2.

*Table 1*

| Stage/ operation | Standard product | GPS Hi-rel A | GPS Hi-rel B | MIL-STD-883C Class B | BSS2 BS9400 Level S2 | MIL-STD-883C Class S[4] |
|---|---|---|---|---|---|---|
| Wafer-fab | | | | | | Wafer-lot accept Method 5007 |
| Probe test | 100% | 100% | 100% | 100% | 100% | 100% |
| Visual inspect chips | Usually 2010 Cond.B | 2010 Cond.B | 2010 Cond.B | 2010 Cond.B | BS9400 1.2.10 Cond.B[1] | 2010 Cond.A |
| Assemble | | | | | | Includes 100% bond pull |
| Screen | None | Method 5004 Class B | As Table 2 | Method 5004 Class B | BS9400 1.2.9 Level B[2] | Method 5004 Class S |
| Test | 100% | 100% | 100% | 100% | 100% | 100% |
| Conformance testing | None | Method 5005 Class B Group A Group B Group C Group D | None | Method 5005 Class B Group A Group B Group C Group D | BS9400[3] Group A Group B Group C Group D | Method 5005 Class S Group A Group B Group C Group D |

NOTES

1. Visual inspection BS9400 1.2.10 Cond. B is similar to MIL-STD 883 Method 2010 Cond. B.
2. Screening BS9400 1.2.9 Level B is equivalent to MIL-STD-883 Method 5004 Class B EXCEPT it does not include 100% hot and cold test.
3. Conformance testing BS9400 is similar to MIL-STD-883 Class B EXCEPT:
   Group A does not necessarily include hot and cold testing
   Group B does include 160 hour operating life test
   Group C does include 2000 hour operating life test and hot and cold testing
   Group D only usually includes 8000 hour life test and dimension checks.
4. MIL-STD-883C Class S/ESA SCC9000: GPS has supplied numerous devices to customer specifications for Space and Satellite applications. Please contact your local GPS sales office for information.

*Table 2*

| Stage/operation | GPS Hi-rel B (References are to MIL-STD-883C) | MIL-STD-883C Class B Method 5004[5] |
|---|---|---|
| Internal Visual | Method 2010 Test Condition B 100% | Method 2010 Test Condition B 100% |
| Stabilisation Bake | Method 1008<br>24Hrs at Condition C 100% | Method 1008<br>24Hrs at Condition C 100% |
| Temperature Cycling | Method 1010 Test Condition C 100% | Method 1010 Test Condition C 100% |
| Constant Acceleration | Method 2010<br>Condition E Y1 only 100% | Method 2010<br>Condition E Y1 only 100% |
| Visual Inspection | – | 100% |
| Initial Electrical | Those parameters requiring Delta calculations. 100% | Those parameters requiring Delta calculations. 100% |
| Burn-In | Method 1015<br>160Hrs at 125°C min. 100% | Method 1015<br>160Hrs at 125°C min. 100% |
| Post Burn-In Electrical Test | Full Electrical Test to Guarantee datasheet. 100% | Those parameters requiring Delta calculations. 100% |
| PDA Calculation | 5% max. All lots | 5% max. All lots |
| Final Electrical Test | Done as Post Burn-In Test. 100% | Full Group A tests as Method 5005 100% |
| Seal (a) Fine<br>Seal (b) Gross | Method 1014 100% | Method 1014 100% |
| Qualification/Quality Conformance Test | – | Method 5005 Class B<br>Samples as necessary |
| External Visual | GPS Spec. sample | Method 2009 100% |

NOTE 5. See Section 5 for further information.

# Package Codes

Package codes for the integrated circuits detailed in this handbook are given below. Dimensioned outline drawings are given in Section 6.

| Code | Type | Description |
|---|---|---|
| **CM** | TO-n(metal) | Cylindrical multi-lead metal can, through-board. |
| **DC** | DILMON | Dual-in-line, multi-layer ceramic, sidebrazed leads, metal sealed lid, through board. |
| **DG** | CERDIP | Dual-in-line, ceramic body, Alloy 42 leadframe, glass sealed, through board. |
| **DP** | PLASDIP | Dual-in-line, copper or Alloy 42 leadframe, plastic moulded, through board. |
| **HG** | Quad Cerpack | Glass sealed ceramic chip carrier, J-formed leads on four sides, surface mount. |
| **HP** | PLCC | Plastic moulded chip carrier, J-formed leads on four sides, surface mount. |
| **LC** | Leadless Chip Carrier | Four sided, leadless, multi-layer ceramic, metal sealed lid, surface mount. |
| **MP** | Small Outline | Dual-in-line, plastic moulded, 'Gullwing' formed leads, metal sealed lid, surface mount. |
| **SOT-23** | Small Outline | 3-lead miniature plastic , 'Gullwing' formed leads, surface mount. |
| **TO-92** | | 3-lead plastic through-board. |

# Section 1
## Data Converters

PRELIMINARY INFORMATION
C11201PDS-1.2

# MA6560

## HIGH SPEED 8-BIT HALF FLASH ANALOG-TO-DIGITAL CONVERTER

The MA6560 is a high speed CMOS analog-to-digital converter with integral sample and hold which uses a half-flash pipelined architecture to provide high conversion rates with low input capacitance and low power consumption. This device is pin compatible with the RCA part CA3318.

The overflow bit makes possible the connection of two converters in series. This produces a 9-bit high speed converter increasing the resolution of the conversion system. The tri-state data outputs allow two MA6560 devices to be connected in parallel so that the sample rate can be doubled by taking samples from alternate devices.

The MA6560 operates with input voltages between 0V and 5V and a full scale range between 0.5V and 5V. The power consumption depends on the frequency and is typically 200mW with a 2V input voltage range at a conversion rate of 20 MSamples/s.

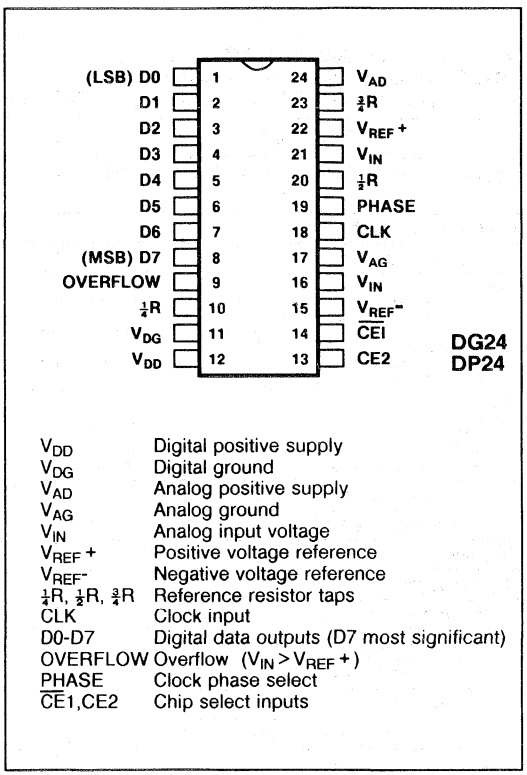
The integral sample and hold feature extends the analog input bandwidth to well beyond that offered by other CMOS flash analog-to-digital converters. This ensures that signals are digitised accurately up to the Nyquist rate without the extra system complexity of an external sample and hold. Other advantages include the ability to code signals above the Nyquist rate in sub-sampled systems; for example, direct RF down-conversion.

### FEATURES

- 20MS/s sample rate
- Integral Sample & Hold ensures High Analog Bandwidth
- 8-bit Tristate Data Output with Overflow Bit
- Low Power Dissipation
- ±0.5 LSB Accuracy Typical
- Single 5V Supply
- 2 Devices Cascadable for 9-bit Output
- 2 Devices Paralleled for Double Sample Rate

### APPLICATIONS

- Video Signal Digitising
- High Speed Digitising Oscilloscopes
- High Speed Digital Signal Processing
- High Performance Hybrid ADC Systems




| | |
|---|---|
| $V_{DD}$ | Digital positive supply |
| $V_{DG}$ | Digital ground |
| $V_{AD}$ | Analog positive supply |
| $V_{AG}$ | Analog ground |
| $V_{IN}$ | Analog input voltage |
| $V_{REF}+$ | Positive voltage reference |
| $V_{REF}-$ | Negative voltage reference |
| ¼R, ½R, ¾R | Reference resistor taps |
| CLK | Clock input |
| D0-D7 | Digital data outputs (D7 most significant) |
| OVERFLOW | Overflow ($V_{IN} > V_{REF}+$) |
| PHASE | Clock phase select |
| $\overline{CE}1$,CE2 | Chip select inputs |

*Fig.1 Pin connections - top view*

### ORDERING INFORMATION

**MA6560PLF** – Plastic DIL (DP), –40°C to +85°C

The following devices are supplied non-standard; contact your local GEC Semiconductors Sales Outlet for details:

**MA6560CCC** – Ceramic DIL (DG), –55°C to +125°C
**MA6560CGC** – Rel 0 Hermetic DIL (DG), –55°C to +125°C

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Supply Voltage $V_{DD}$-$V_{DG}$, $V_{AD}$-$V_{AG}$ | -0.3 | 7 | V |
| Digital input Voltage | $V_{DG}$-0.3 | $V_{DD}$+0.3 | V |
| Operating Temperature (Note 1) | -40 | 85 | °C |
| Storage temperature | -55 | 150 | °C |

*Stresses above those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1:Devices are supplied to the industrial temperature range, -40°C to +85°C, as standard. Devices can also be supplied to the military temperature range, -55°C to +125°C; contact your local GEC Semiconductors Sales Outlet for details.

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$V_{DD}$ = 5V, $V_{AD}$ = 5V, $V_{REF}$+ = 3.5V;$V_{REF}$- = 1.5V;$V_{IN}$ source resistance = 50Ω

| Characteristic | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Operating Supply Voltage (over full temperature range) | 4.5 | 5.0 | 5.5 | V |
| DC Power Dissipation | 70 | 100 | 140 | mW |
| AC Power Dissipation | 3.5 | 5.0 | 7.5 | mW/MHz |
| Resolution | - | 8 | - | Bits |
| Integral Linearity (See note 1) | - | ±0.5 | ±1.0 | LSB |
| Differential Linearity ($f_{CLK}$ = 15MHz) | - | ±0.4 | ±0.5 | LSB |
| Bandwidth (See note 2) | 5 | 7 | 10 | MHz |
| Offset Error | -20 | - | 20 | mV |
| Gain Error | -4 | -5 | -6 | LSB |
| Full Scale Range, [$V_{REF}$+] – [$V_{REF}$-] (See note 3) | 0.5 | 2.0 | 5.0 | V |
| Input Voltage Range | 0 | 2.0 | 5.0 | V |
| Positive Reference Voltage, $V_{REF}$+ | 0.5 | 3.5 | 5.0 | V |
| Negative Reference Voltage, $V_{REF}$- | 0.0 | 1.5 | 4.5 | V |
| $V_{IN}$ Capacitance | 18 | 20 | 22 | pF |
| $V_{IN}$ Source Resistance | 0 | 50 | 100 | Ω |
| Reference resistor ladder Impedance | 400 | 500 | 700 | Ω |
| Conversion Rate (See note 4) | 20 | 25 | 30 | MSamples/s |
| Minimum Clock High or Clock Low Time | - | 5 | - | ns |
| Minimum Clock Frequency (See note 5) | - | 0.1 | 100 | kHz |
| Input High Voltage, $V_{IH}$ | 3.5 | - | - | V |
| Input Low Voltage, $V_{IL}$ | - | - | 1.5 | V |
| Output High Voltage, $V_{OH}$ ($I_{OH}$ = 1mA) | 2.4 | - | - | V |
| Output Low Voltage, $V_{OL}$ ($I_{OL}$ = -2mA) | - | - | 0.4 | V |
| Tristate Leakage Current | - | - | 10 | μA |

NOTES

1. Without external midpoint trim. Integral linearity is ±0.5 LSB maximum with trim.
2. For 0.5 LSB maximum additional error on a full scale input sinewave. 3dB point is typically 70MHz.
3. Maximum bandwidth and sampling rate depend on full scale range.
4. 50% clock duty cycle.
5. Typical at 25°C - Maximum is worst case at 85°C.

## OPERATING NOTES

The MA6560 analog-to-digital converter is based on a pipelined half-flash technique with multiple conversion cores which results in high performance with low power consumption.

Fig. 2 shows the block diagram of the MA6560. The comparator array consists of two comparator cores with integral sample and hold functions. To achieve fast operation, the two cores are clocked alternately. Each core operates at half the system clock rate.

With the PHASE input low, the analog input voltage is sampled on the falling edge of the clock. The comparator array tests the sampled voltage in two stages. First, the four most significant bits are generated and latched, and then the four least significant bits are generated and the final result is decoded to an 8 bit binary word and latched. The pipelining used to maximise throughput results in a sample-to-data out delay of four clock periods as shown in Fig. 3.

An on-chip reference resistor string is used to establish reference voltages for the comparator array. Both ends of the reference string should be driven by external voltage references to define the converter zero and full scale levels. The reference resistor ladder is tapped at three points to allow decoupling and external trimming to maximise integral linearity.

The tri-state data outputs are controlled by chip enable inputs. For D0 to D7 to be enabled, $\overline{CE1}$ must be low and CE2 must be high. The OVERFLOW output only requires CE2 to be high to be enabled. This scheme is used to facilitate the cascading of devices.

The PHASE input is provided to allow the operation of the converter to be defined by the rising or the falling edge of the clock. This facility is incorporated to allow two MA6560s to be operated in parallel on different clock phases for double speed operation.

The OVERFLOW output goes high when the analog input voltage exceeds the $V_{REF}+$ level. This can be used as an error signal or to enable a second MA6560 and generate a ninth bit when two MA6560s are cascaded for 9 bit operation.

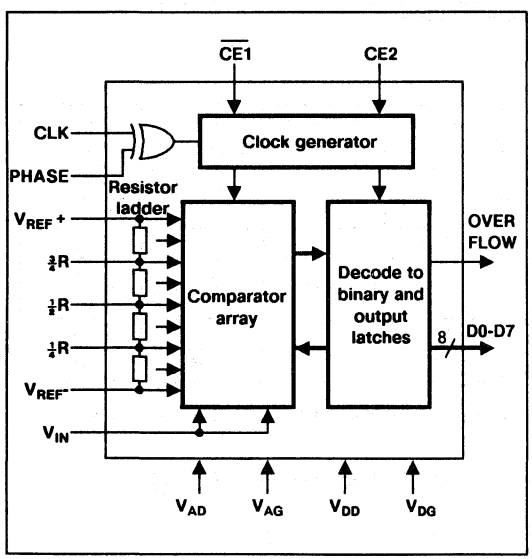



*Fig.2 Block daigram*

## PIN DESCRIPTIONS

**CLK**
Clock input. With the PHASE input logic low, the falling edge of the clock defines the point at which the analog input level is sampled.

**PHASE**
Clock phase input. The CLK input is Exclusive-ORed with the PHASE input to allow the converter operation to be defined by either the rising or falling edge of the clock. With PHASE logic low, the analog input is sampled on the falling edge of the clock.

**D0-D7**
Digital data outputs - D0 is the least significant bit with D7 the most significant bit. The data outputs are tri-state and are enabled with $\overline{CE1}$ logic low and CE2 logic high. Valid data for a specific sample is available four full clock cycles after the analog value was sampled.

**OVERFLOW**
The OVERFLOW output goes high when the analog input voltage exceeds the $V_{REF}+$ level.

**$\overline{CE1}$, CE2**
Chip enable inputs. D0-D7 and OVERFLOW outputs are enabled as shown in Table 1:

| $\overline{CE1}$ | CE2 | D0-D7 | OVERFLOW |
|---|---|---|---|
| 0 | 0 | Hi-Z | Hi-Z |
| 0 | 1 | Outputs | Output |
| 1 | 0 | Outputs | Illegal output |
| 1 | 1 | Hi-Z | Output |

*Table1*

**$V_{IN}$**
Analog inputs. The analog inputs are sampled on each clock cycle and converted to an 8 bit value which is available at the data outputs after four full clock cycles.
To achieve high accuracy at high speed, $V_{IN}$ must be driven by a low impedance to ensure that the sample and hold settles to within one least significant bit between conversions. The input capacitance is typically 20pF and settling to 1 lsb in 8 bits requires that the input signal is available to the sample and hold for at least 5.6 $R_{source} \times C_{in}$ time constants. The two analog inputs should be tied together externally.

**$V_{REF}+$**
Positive voltage reference input, used to define the full scale analog input level.

**$V_{REF}-$**
Negative voltage reference input, used to define the zero analog input level. In many applications, $V_{REF}-$ may be connected to analog ground.

**$\frac{3}{4}R$, $\frac{1}{2}R$, $\frac{1}{4}R$**
Reference resistor ladder taps which are pinned out for decoupling. They can also be driven by external reference drivers to improve the integral linearity of the converter.

**$V_{AD}$**
Analog positive supply.

**$V_{AG}$**
Analog ground.

**$V_{DD}$**
Digital positive supply.

**$V_{DG}$**
Digital ground.

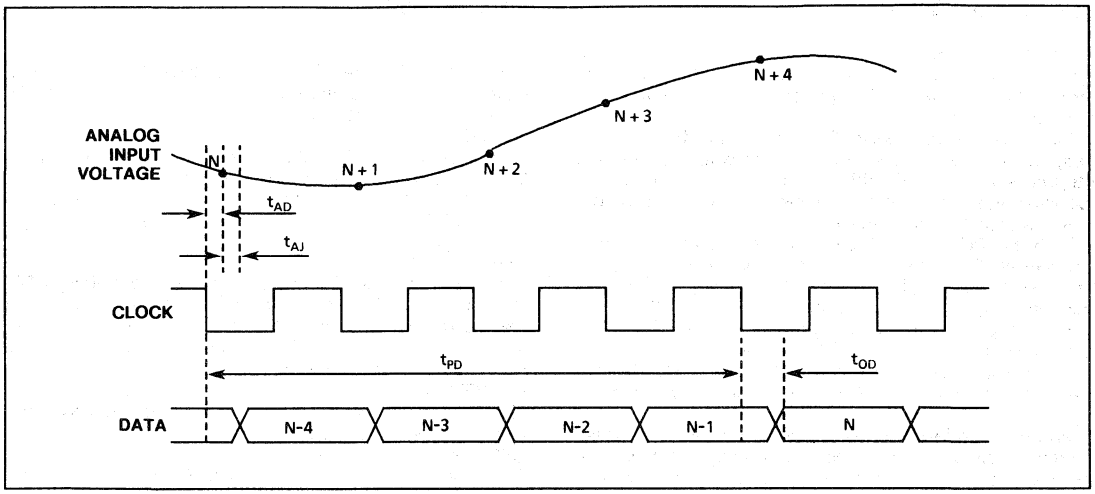



*Fig. 3: General timing diagram (PHASE = 0)*

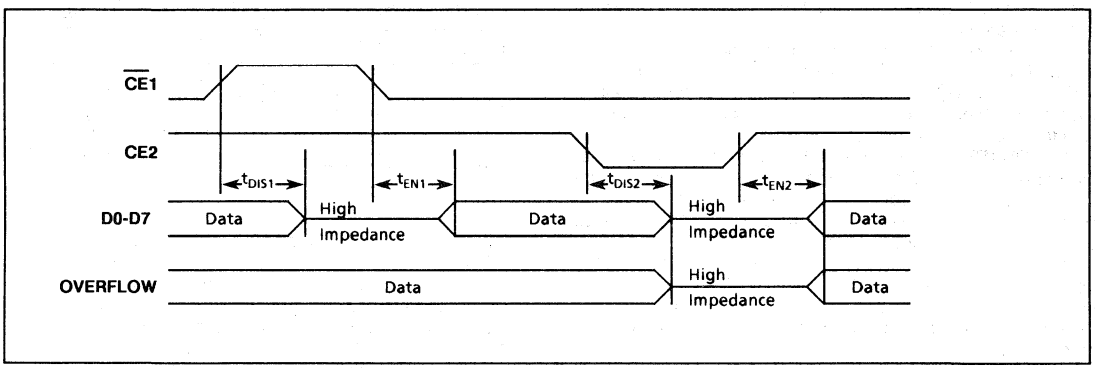



*Fig. 4: Output enable timing diagram*

## DYNAMIC CHARACTERISTICS

| Characteristic | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| $V_{IN}$ Aperture delay, $t_{AD}$ | 10 | 25 | 57 | ns |
| $V_{IN}$ Aperture jitter, $t_{AJ}$ | | | 25 | ps |
| Data/overflow pipeline delay, $t_{PD}$ | | 4 | | Clock cycles |
| Data/overflow output delay (2) (to valid logic threshold) $t_{OD}$ | 13 | 33 | 75 | ns |
| $\overline{CE1}$ to data disable, $t_{DIS1}$ | 11 | 28 | 64 | ns |
| $\overline{CE1}$ to data enable, $t_{EN1}$ (2) (to valid logic threshhold) | 13 | 32 | 73 | ns |
| CE2 to data/overflow disable, $t_{DIS2}$ | 14 | 34 | 77 | ns |
| CE2 to data/overflow enable, $t_{EN2}$ (2) (to valid logic threshhold) | 12 | 30 | 68 | ns |

NOTES
1. Typical figures are for operation with $V_{DD}$, $V_{AD}$ = 5V, 25°C. Min. and Max. figures are over full supply voltage and temperature ranges
2. $C_{LOAD}$ = 10pF
3. Timings measured from CE1 and CE2 = $V_{DD}/2$ to 10% change in data output voltage with 1kΩ // 10pF load

## APPLICATION NOTES

### Grounding / Decoupling

The analog and digital grounds of the system should be kept separate and only connected at the converter. The use of ground planes is recommended to ensure that the analog data to be converted is free of digital ground noise.

Reference drivers, input amplifiers, reference taps, and the $V_{AD}$ supply should be decoupled at the converter to analog ground. All capacitors should be low impedance 100nF ceramics in parallel with 4.7$\mu$F tantalum capacitors to ensure effective decoupling and should be mounted as close to the converter as possible.

If $V_{AD}$ is derived from $V_{DD}$, a small inductor should be used to reduce digital noise on the analog supply.

### Application circuit

Fig. 5 shows a typical application with the MA6560 functioning as a high performance 8 bit 20MS/s data acquisition front-end. $V_{REF}+$ and $V_{REF}-$ are derived from a single 2.5V voltage reference. Emitter followers driving the $V_{REF}$ inputs ensure that current is available for a large full scale range. The reference driver circuitry can be simplified if the input signal is referenced to analog ground, in which case $V_{REF}-$ should be connected to analog ground. Decoupling of the supplies, voltage reference inputs and reference resistor ladder is important to achieve full 8 bit performance at 20MS/s.

### Offset and gain trims

Offset correction should be carried out in the pre-amp circuitry by introducing a DC shift to $V_{IN}$ or by adjusting the op-amp offset trim. The trim should be carried out by applying the input voltage that corresponds to the first code transition and trimming until the transition is observed.

The gain trim should also be carried out in the pre-amp circuitry by introducing a gain adjustment. When this is not possible, an adjustment to the reference voltage should be made.

To achieve gain trim, first adjust offset trim as above and then set $V_{IN}$ to full scale. Following this, adjust the pre-amp gain or $V_{REF}+$ until the OVERFLOW output goes high.

### Quarter point trims

The quarter points should be decoupled with 100nF low inductance ceramic (chip capacitors are recommended) and 4.7$\mu$F tantalum capacitors. Decoupling is required to reduce the dynamic impedance of the resistor ladder and becomes more important as the sample rate is increased.

The quarter points can also be driven by reference drivers connected between $V_{REF}+$ and $V_{REF}-$ as shown in Fig. 6. The reference drivers should be adjusted to compensate for non-linearities introduced by inaccuracies in the on-chip reference resistors. The adjustment must be carried out with the ADC operating at the required clock rate and are made by applying values of $V_{IN}$ that correspond to $\frac{1}{4}$, $\frac{1}{2}$, and $\frac{3}{4}$ full scale and adjusting the reference drivers until the correct output code transitions are observed. Note that the adjustments are interactive, so more than one pass will be required.

At clock rates upto 5MHz, trimming the $\frac{1}{2}$R input should be sufficient to achieve good linearity performance. Above 5MHz, trim all the quarter points for optimum linearity performance.

### 9- bit resolution

To achieve 9-bit resolution, the reference resistor ladders of two MA6560 devices should be totem-poled as shown in Fig. 7. The aim is to split the 9-bit transfer function between two MA6560 converters. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The data outputs of the two devices (D0-D7) should be connected together. The OVERFLOW output of the lower MA6560 is used as the ninth bit, and to select which of the two MA6560 converters supplies the lower 8 bits of data. When the OVERFLOW output goes high, data must come from the upper device. When it goes low, data must come from the lower device. This is done by simply connecting the lower overflow signal to the $\overline{CE1}$ control of the lower device and the CE2 control of the upper device.

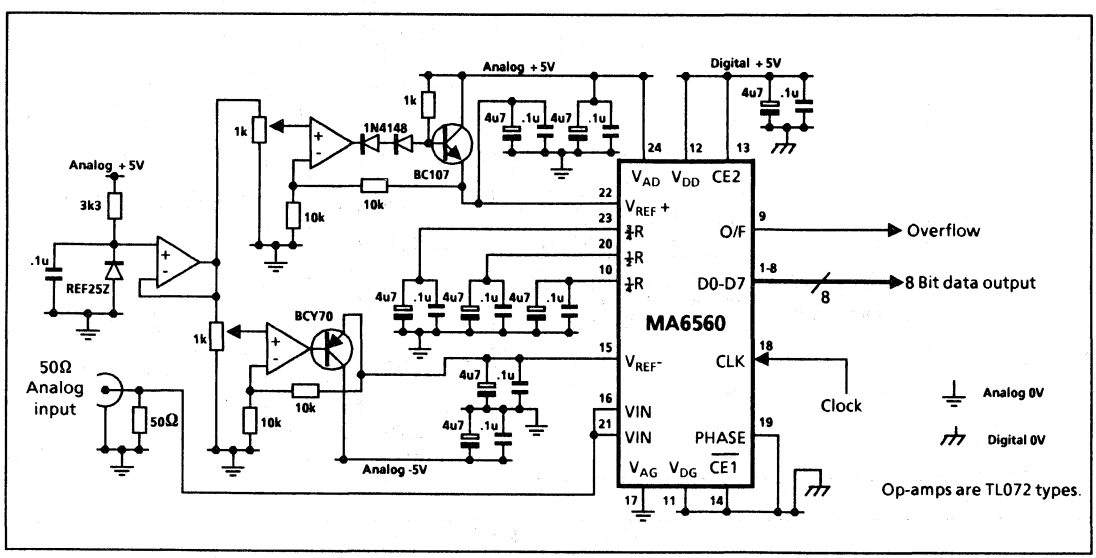



*Fig.5 Typical application*

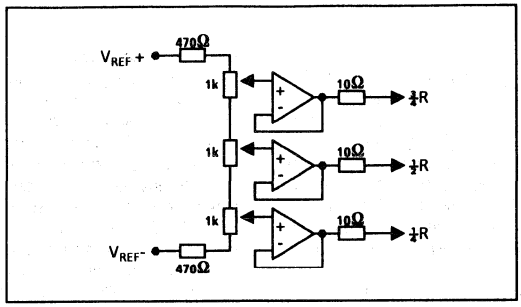



*Fig.6 Reference driver circuit*

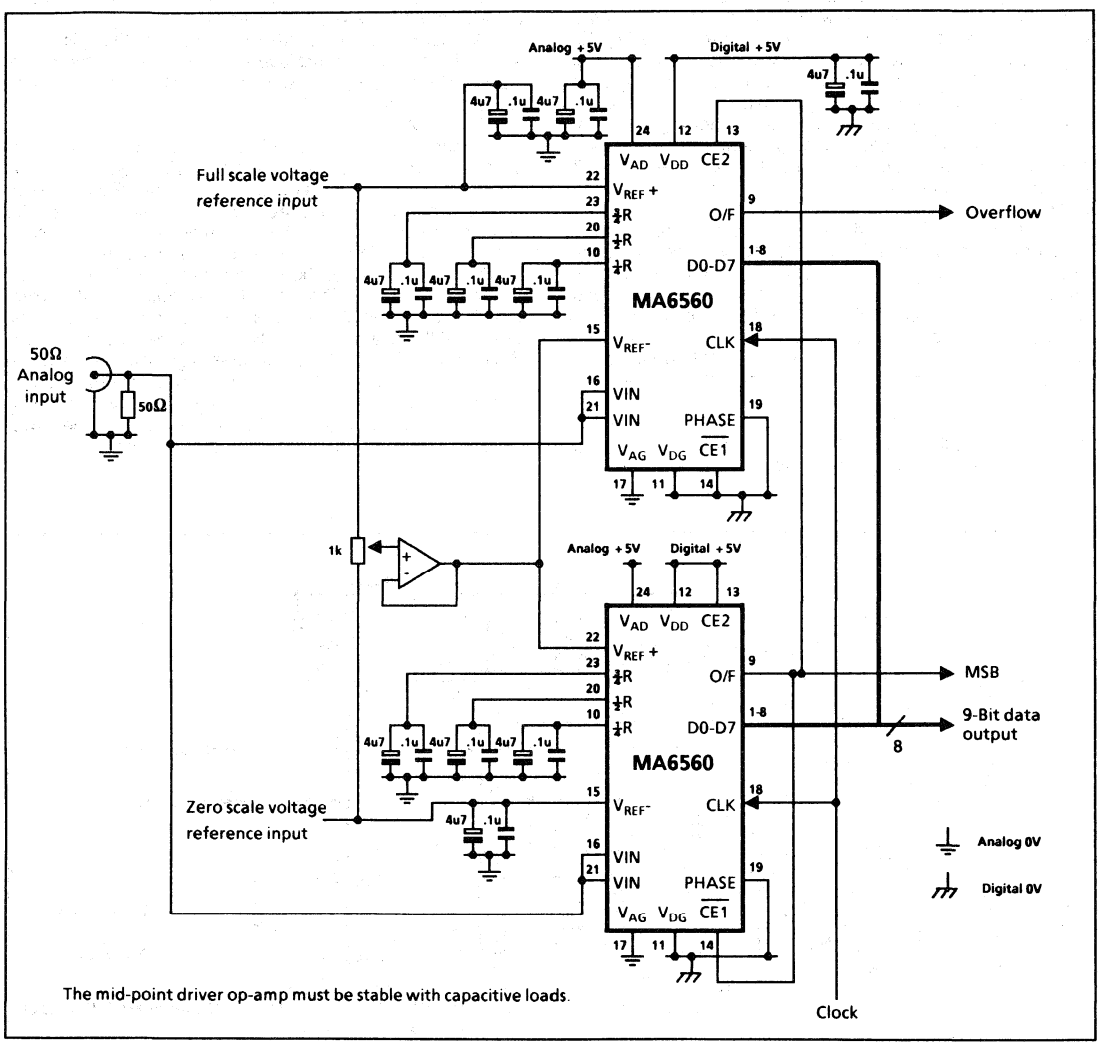



*Fig.7 Expansion to 9 bits*

# MA6561

## HIGH SPEED 8-BIT FLASH ANALOG-TO-DIGITAL CONVERTER

The MA6561 is a high speed CMOS SOS analog-to-digital converter which uses a half-flash pipelined architecture to provide high conversion rates with low input capacitance. This device is functionally compatible with the RCA part CA3318.

The overflow bit makes possible the connection of two converters in series. This produces a 9-bit high speed converter, increasing the resolution of the conversion system. The tri-state data outputs allow two MA6561 devices to be connected in parallel so that the sample rate can be doubled by taking samples from alternate devices.

The MA6561 operates with input voltages between 0V and 5V and a full scale range between 1V and 1V. The power consumption depends on the frequency and is typically 845mW with a 2V input voltage range at a conversion rate of 50 MSamples/s.

### FEATURES

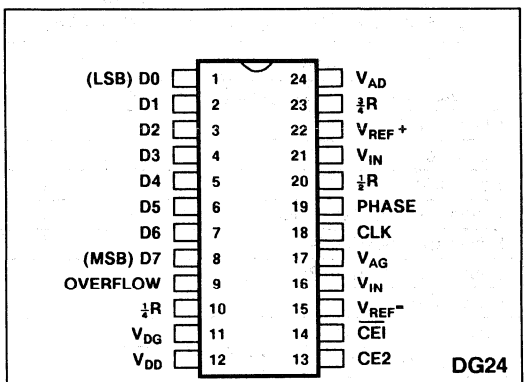
- CMOS Silicon-on Sapphire
- 20MS/s sample rate
- Low Input Capacitance
- 8-bit Tristate Data Output with Overflow Bit
- ±0.5 LSB Accuracy Typical
- Single 5V Supply
- 2 Devices Cascadable for 9-bit Output
- 2 Devices Paralleled for Double Sample Rate

### APPLICATIONS

- Video Signal Digitising
- High Speed Digitising Oscilloscopes
- High Speed Digital Signal Processing
- High Performance Hybrid ADC Systems

### ORDERING INFORMATION

**MA6561CCC** – Ceramic DIL (DG), –55°C to +125°C




| | |
|---|---|
| $V_{DD}$ | Digital positive supply |
| $V_{DG}$ | Digital ground |
| $V_{AD}$ | Analog positive supply |
| $V_{AG}$ | Analog ground |
| $V_{IN}$ | Analog input voltage |
| $V_{REF}+$ | Positive voltage reference |
| $V_{REF}-$ | Negative voltage reference |
| $\frac{1}{4}R$, $\frac{1}{2}R$, $\frac{3}{4}R$ | Reference resistor taps |
| CLK | Clock input |
| D0-D7 | Digital data outputs (D7 most significant) |
| OVERFLOW | Overflow ($V_{IN} > V_{REF}+$) |
| PHASE | Clock phase select |
| $\overline{CE1}$,CE2 | Chip select inputs |

*Fig.1 Pin connections - top view*

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Analog supply voltage $V_{AD}$-$V_{AG}$ | -0.3 | 7 | V |
| Digital supply voltage $V_{DD}$-$V_{DG}$ | -0.3 | 7 | V |
| Digital input voltage | $V_{DG}$-0.3 | $V_{DD}$+0.3 | V |
| Operating temperature | -55 | 125 | °C |
| Storage temperature | -55 | 150 | °C |

*Stresses above those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{AMB}$ = 25°C; $V_{DD}$ = 5V; $V_{AD}$ = 5V; $V_{REF}$+ = 3.5V; $V_{REF}$- = 1.5V; $V_{IN}$ source resistance = 50Ω; $f_{CLK}$ = 10MHz, 50% duty cycle.

| Characteristic | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Operating supply voltage (over full temp. range) | 4.5 | 5.0 | 5.5 | V |
| DC power dissipation | - | 325 | - | mW |
| AC power dissipation | 3.5 | 10.4 | 7.5 | mW/MHz |
| Resolution | - | 8 | - | Bits |
| Integral linearity (see note 1) | - | ±0.5 | ±1.0 | LSB |
| Differential linearity ($f_{CLK}$ = 15MHz) | - | ±0.25 | ±0.5 | LSB |
| Bandwidth (see note 2) | - | 6.6 | - | MHz |
| Offset error | -10 | - | 10 | mV |
| Gain error | - | 1.5 | - | LSB |
| Full scale range, [$V_{REF}$+] – [$V_{REF}$-] (see note 3) | 1.0 | 2.0 | 3.0 | V |
| Input voltage range | 0 | 2.0 | 5.0 | V |
| Positive reference voltage, $V_{REF}$+ | 1.0 | 3.5 | 5.0 | V |
| Negative reference voltage, $V_{REF}$- | 0.0 | 1.5 | 4.0 | V |
| $V_{IN}$ capacitance | - | 14 | - | pF |
| $V_{IN}$ source resistance | 0 | 25 | 50 | Ω |
| Reference resistor ladder impedance | - | 268 | - | Ω |
| Conversion rate | 40 | 50 | 60 | MSamples/s |
| Minimum clock high or clock low time | - | 7 | - | ns |
| Minimum clock frequency (see note 4) | - | 0.5 | 10 | MHz |

NOTES

1. Without external midpoint trim. integral linearity is ±0.5 LSB maximum with trim.
2. For 0.5 LSB maximum additional error on a full scale input sinewave. 3dB point is typically 85MHz. The typical figure quoted is for $CLK_{HIGH}$ = 10ns and $CLK_{LOW}$ = 90ns.
3. Maximum bandwidth and sampling rate depend on full scale range.
4. The typical value is at 25°C. The maximum value of 10MHz clock frequency is for operation at 75°C. Full characterisation above this temperature had not been completed at the time of printing this handbook. Please contact your local GEC Semiconductors Sales Outlet for latest information.

## OPERATING NOTES

The MA6561 analog-to-digital converter is based on a pipelined full-flash technique which results in very high speed performance.

Fig. 2 shows the block diagram of the MA6561. The comparator array effectively consists of 256 comparators which simultaneously compare the input voltage with 256 reference levels which are generated by an on-chip resistor ladder.

With the PHASE input low, the analog input voltage is compared with the 256 reference levels on the falling edge of the clock. A 256 level thermometer code is generated and the final result is decoded to an 8 bit binary word and latched. The pipelining used to maximise throughput results in a sample-to-data out delay of five clock periods as shown in Fig. 3.

Both ends of the reference string should be driven by external voltage references to define the converter zero and full scale levels. The reference resistor ladder is tapped at three points to allow decoupling and external trimming to maximise integral linearity.

The tri-state data outputs are controlled by chip enable inputs. For D0 to D7 to be enabled, $\overline{CE1}$ must be low and CE2 must be high. The OVERFLOW output only requires CE2 to be high to be enabled. This scheme is used to facilitate the cascading of devices.

The PHASE input is provided to allow the operation of the converter to be defined by the rising or the falling edge of the clock. This facility is incorporated to allow two MA6561s to be operated in parallel on different clock phases for double speed operation.

The OVERFLOW output goes high when the analog input voltage exceeds the $V_{REF}+$ level. This can be used as an error signal or to enable a second MA6561 and generate a ninth bit when two MA6561s are cascaded for 9-bit operation.

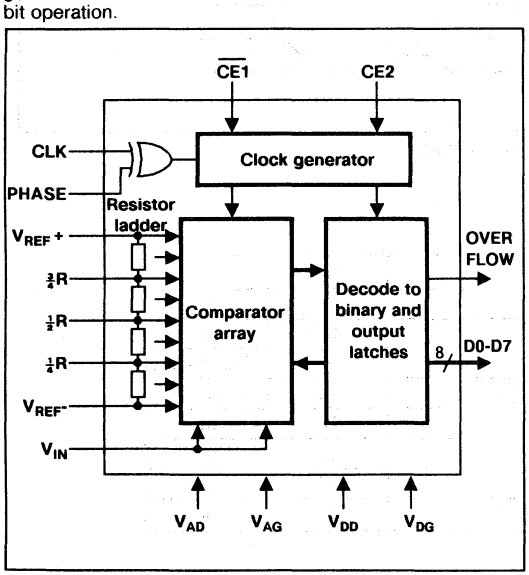



*Fig.2 Block diagram*

## PIN DESCRIPTIONS

**CLK**
Clock input. With the PHASE input logic low, the falling edge of the clock defines the point at which the analog input level is sampled.

**PHASE**
Clock phase input. The CLK input is Exclusive-ORed with the PHASE input to allow the converter operation to be defined by either the rising or falling edge of the clock. With PHASE logic low, the analog input is sampled on the falling edge of the clock.

**D0-D7**
Digital data outputs - D0 is the least significant bit with D7 the most significant bit. The data outputs are tri-state and are enabled with $\overline{CE1}$ logic low and CE2 logic high. Valid data for a specific sample is available four full clock cycles after the analog value was sampled.

**OVERFLOW**
The OVERFLOW output goes high when the analog input voltage exceeds the $V_{REF}+$ level.

**$\overline{CE1}$, CE2**
Chip enable inputs. D0-D7 and OVERFLOW outputs are enabled as shown in Table 1:

| $\overline{CE1}$ | CE2 | D0-D7 | OVERFLOW |
|---|---|---|---|
| 0 | 0 | Hi-Z | Hi-Z |
| 0 | 1 | Outputs | Output |
| 1 | 0 | Outputs | Illegal output |
| 1 | 1 | Hi-Z | Output |

*Table1*

**$V_{IN}$**
Analog inputs. The analog inputs are sampled on each clock cycle and converted to an 8-bit value which is available at the data outputs after five full clock cycles.

To achieve high accuracy at high speed, $V_{IN}$ must be driven by a low impedance to ensure that the input settles to within one least significant bit between conversions. The two analog inputs should be tied together externally.

**$V_{REF}+$**
Positive voltage reference input, used to define the full scale analog input level.

**$V_{REF}-$**
Negative voltage reference input, used to define the zero analog input level. In many applications, $V_{REF}-$ may be connected to analog ground.

**$\frac{3}{4}R$, $\frac{1}{2}R$, $\frac{1}{4}R$**
Reference resistor ladder taps which are pinned out for decoupling. They can also be driven by external reference drivers to improve the integral linearity of the converter.

**$V_{AD}$**
Analog positive supply.

**$V_{AG}$**
Analog ground.

**$V_{DD}$**
Digital positive supply.

**$V_{DG}$**
Digital ground.

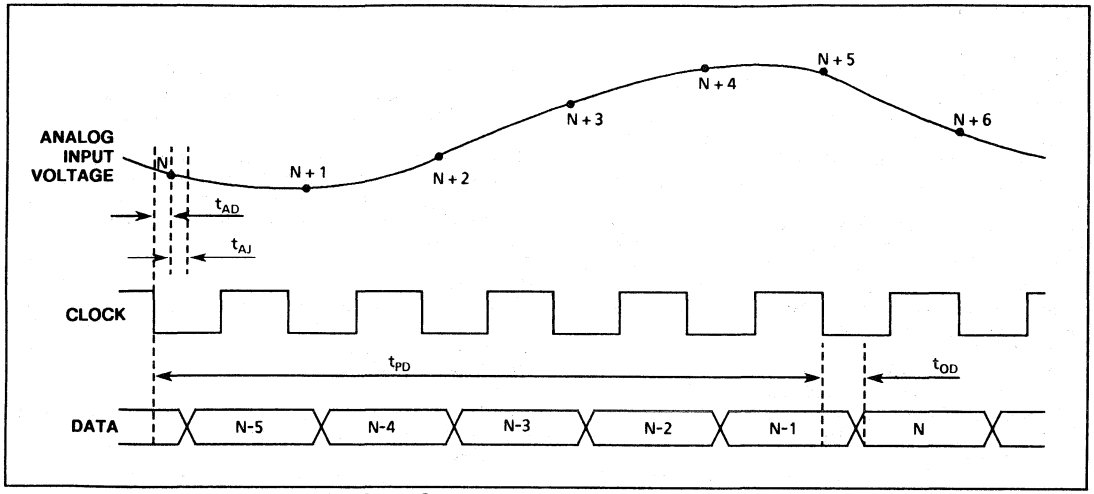



*Fig. 3: General timing diagram (PHASE = 0)*

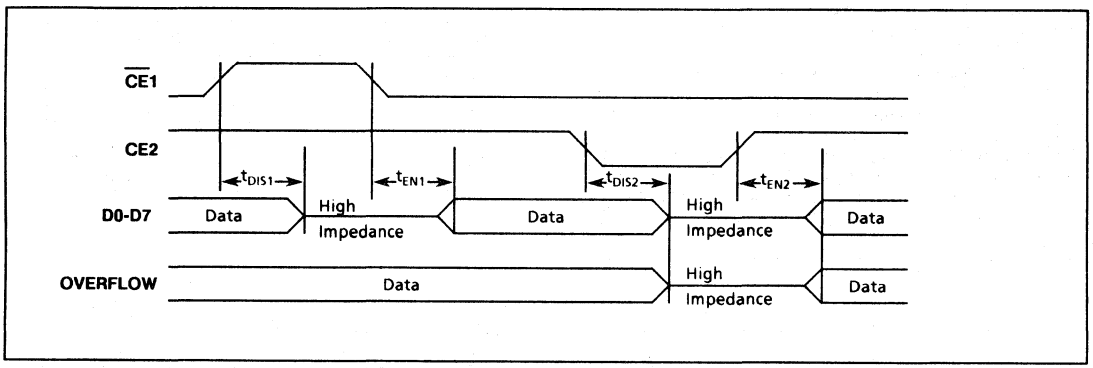



*Fig. 4: Output enable timing diagram*

## DYNAMIC CHARACTERISTICS

| Characteristic | Typ. | Units |
|---|---|---|
| $V_{IN}$ Aperture delay, $t_{AD}$ | 12.2 | ns |
| $V_{IN}$ Aperture jitter, $t_{AJ}$ | < 24 | ps |
| Data/overflow pipeline delay, $t_{PD}$ | 5 | Clock cycles |
| Data/overflow output delay (to valid logic threshold) $t_{OD}$ | 38 | ns |
| $\overline{CE1}$ to data disable, $t_{DIS1}$ | 25 | ns |
| $\overline{CE1}$ to data enable, $t_{EN1}$ (to valid logic threshhold) | 25 | ns |
| CE2 to data/overflow disable, $t_{DIS2}$ | 32 | ns |
| CE2 to data/overflow enable, $t_{EN2}$ (to valid logic threshhold) | 33 | ns |

## APPLICATION NOTES

### Grounding / Decoupling

The analog and digital grounds of the system should be kept separate and only connected at the converter. The use of ground planes is recommended to ensure that the analog data to be converted is free of digital ground noise.

Reference drivers, input amplifiers, reference taps, and the $V_{AD}$ supply should be decoupled at the converter to analog ground. All capacitors should be low impedance 100nF ceramics in parallel with 4.7µF tantalum capacitors to ensure effective decoupling and should be mounted as close to the converter as possible.

If $V_{AD}$ is derived from $V_{DD}$, a small inductor should be used to reduce digital noise on the analog supply.

### Application circuit

Fig. 5 shows a typical application with the MA6561 functioning as a high performance 8-bit high speed data acquisition front-end. $V_{REF}+$ and $V_{REF}-$ are derived from a single 2.5V voltage reference. Emitter followers driving the $V_{REF}$ inputs ensure that current is available for a large full scale range. The reference driver circuitry can be simplified if the input signal is referenced to analog ground, in which case $V_{REF}-$ should be connected to analog ground. Decoupling of the supplies, voltage reference inputs and reference resistor ladder is important to achieve full 8-bit performance at high speed.

### Offset and gain trims

Offset correction should be carried out in the pre-amp circuitry by introducing a DC shift to $V_{IN}$ or by adjusting the op-amp offset trim. The trim should be carried out by applying the input voltage that corresponds to the first code transition and trimming until the transition is observed.

The gain trim should also be carried out in the pre-amp circuitry by introducing a gain adjustment. When this is not possible, an adjustment to the reference voltage should be made.

To achieve gain trim, first adjust offset trim as above and then set $V_{IN}$ to full scale. Following this, adjust the pre-amp gain or $V_{REF}+$ until the OVERFLOW output goes high.

### Quarter point trims

The quarter points should be decoupled with 100nF low inductance ceramic (chip capacitors are recommended) and 4.7µF tantalum capacitors. Decoupling is required to reduce the dynamic impedance of the resistor ladder and becomes more important as the sample rate is increased.

The quarter points can also be driven by reference drivers connected between $V_{REF}+$ and $V_{REF}-$ as shown in Fig. 6. The reference drivers should be adjusted to compensate for non-linearities introduced by inaccuracies in the on-chip reference resistors. The adjustment must be carried out with the ADC operating at the required clock rate and are made by applying values of $V_{IN}$ that correspond to $\frac{1}{4}$, $\frac{1}{2}$, and $\frac{3}{4}$ full scale and adjusting the reference drivers until the correct output code transitions are observed. Note that the adjustments are interactive, so more than one pass will be required.

### 9- bit resolution

To achieve 9-bit resolution, the reference resistor ladders of two MA6561 devices should be totem-poled as shown in Fig. 7. The aim is to split the 9-bit transfer function between two MA6561 converters. Since the absolute resistance value of each ladder may vary, external trim of the mid-reference voltage may be required.

The data outputs of the two devices (D0-D7) should be connected together. The OVERFLOW output of the lower MA6561 is used as the ninth bit, and to select which of the two MA6561 converters supplies the lower 8 bits of data. When the OVERFLOW output goes high, data must come from the upper device. When it goes low, data must come from the lower device. This is done by simply connecting the lower overflow signal to the $\overline{CE1}$ control of the lower device and the CE2 control of the upper device.

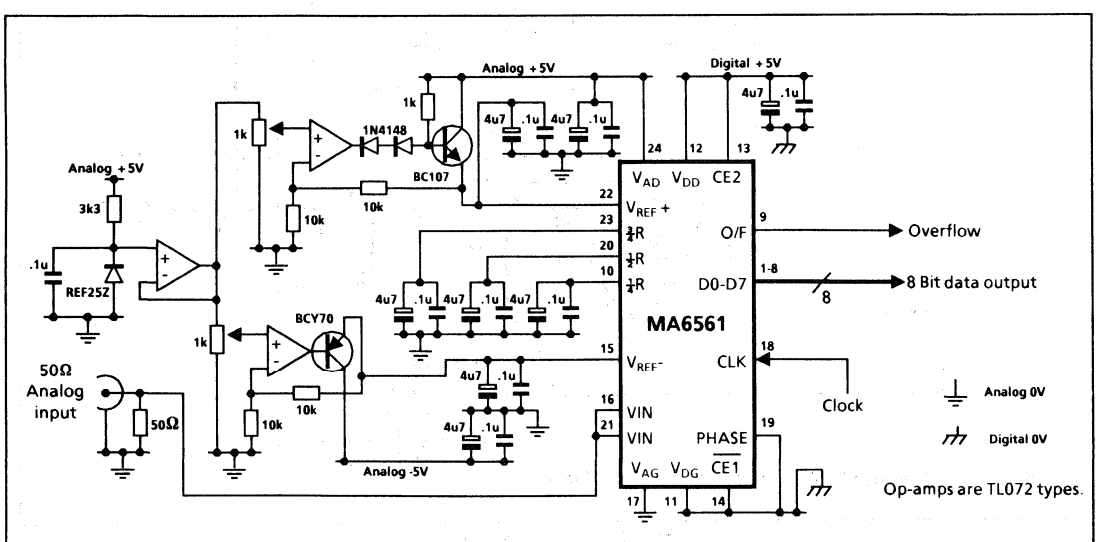



*Fig.5 Typical application*

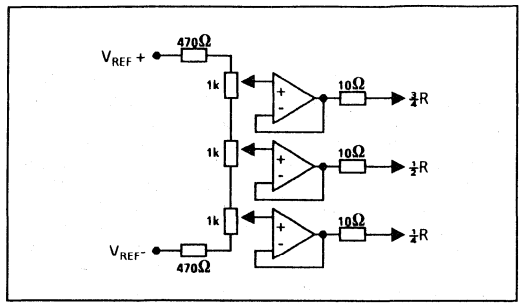



*Fig.6 Reference driver circuit*

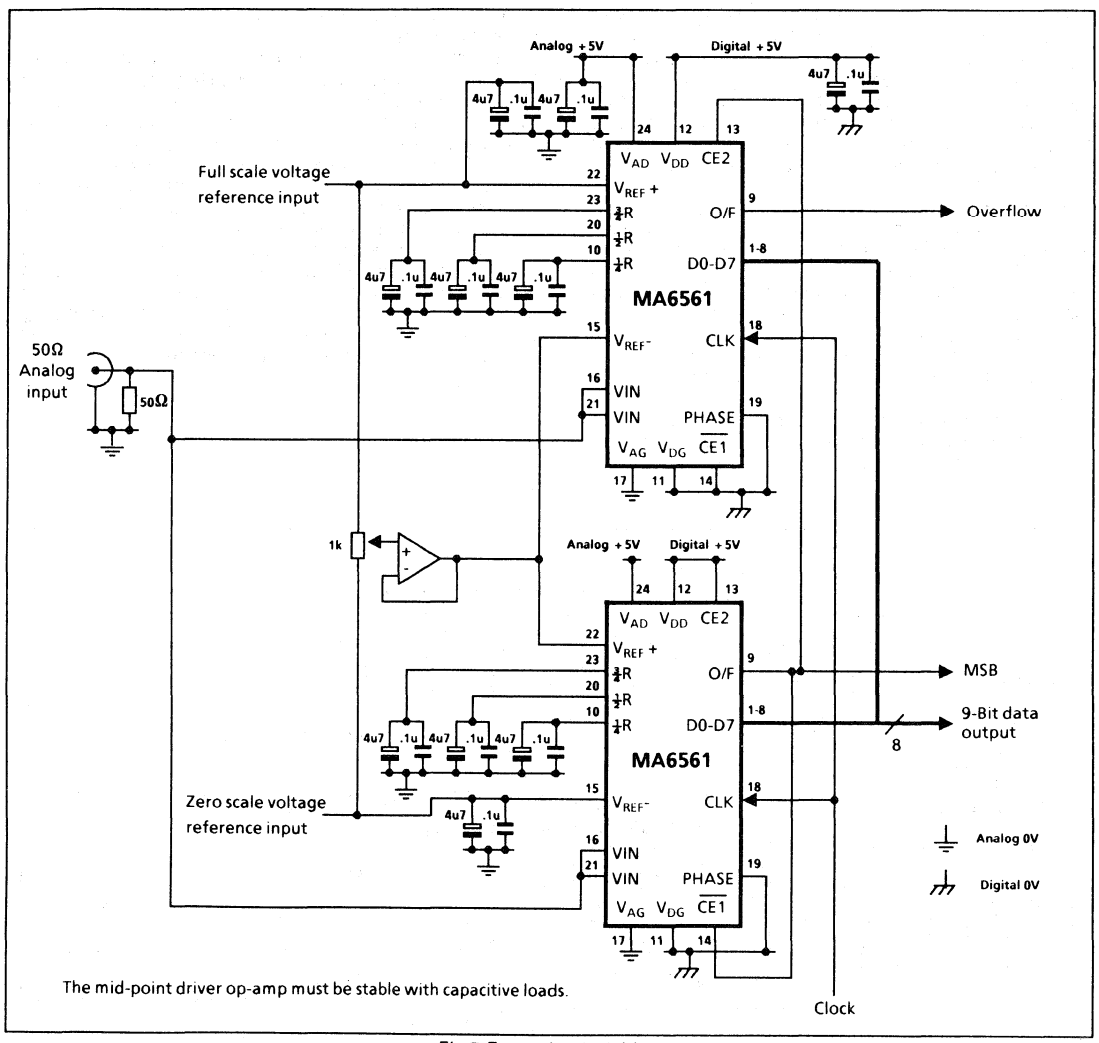



*Fig.7 Expansion to 9 bits*

# MA6670

## HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

The MA6670 is a high speed CMOS digital-to-analog converter with complementary current outputs. The architecture has been optimised to drive doubly terminated 50Ω and 75Ω loads with 1V levels for maximum speed and minimum settling time.

The MA6670 incorporates separate analog and digital power supplies to minimise noise on the analog outputs. The pin placing facilitates the design of low noise printed circuit boards with ground planes, for maximum performance.

A single clock pulse is required to latch the digital input data and update the analog output, allowing single shot or continuous operation.

The MA6670 can be switched to a powered down state.

### FEATURES

- 8-bit Monotonicity
- ±0.3 LSB Typical Differential Non-linearity
- ±1.0 LSB Integral Non-linearity
- 25Ω Drive Capability
- 35MHz Update Rate
- Single Shot or Clocked Operation
- Single 5V Supply
- Output Switchable to High-Z / Power Down

### APPLICATIONS

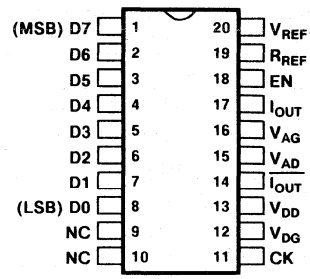
- High Speed DSP
- Video Signal Reconstruction
- High Speed Waveform Synthesis
- Analog Reconstruction in Subranging or Residue Analog-to-Digital Converters

### ORDERING INFORMATION

**MA6670PLF** – Plastic DIL (DP), –40°C to +85°C

The following device is supplied non-standard; contact your local GEC Semiconductors Sales Outlet for details:

**MA6670CCC** – Ceramic DIL (DG), –55°C to +125°C




**DG20**
**DP20**

| | |
|---|---|
| $V_{DD}$ | Digital positive supply |
| $V_{DG}$ | Digital ground |
| $V_{AD}$ | Analog positive supply |
| $V_{AG}$ | Analog ground |
| $I_{OUT}$ | Current output |
| $\overline{I_{OUT}}$ | Complementary current output |
| $V_{REF}$ | Voltage reference input |
| $R_{REF}$ | Reference resistor |
| CK | Clock input |
| D0-D7 | Digital data inputs (D7 most significant) |
| EN | Enable input, active high |

*Fig.1 Pin connections - top view*

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Supply Voltage $V_{DD}$-$V_{DG}$, $V_{AD}$-$V_{AG}$ | -0.3 | 11 | V |
| Digital input Voltage | $V_{DG}$-0.3 | $V_{DD}$ + 0.3 | V |
| Operating Temperature (Note 1) | -40 | 85 | °C |
| Storage temperature | -55 | 150 | °C |

*Stresses above those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1:Devices are supplied to the industrial temperature range, -40°C to +85°C, as standard. Devices can also be supplied to the military temperature range, -55°C to +125°C; contact your local GEC Semiconductors Sales Outlet for details.

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$V_{DD}$ = 5V, $V_{AD}$ = 5V, $V_{REF}$ = 1.0V, $I_{REF}$ = 625μA, $R_{REF}$ = 1.6kΩ, $R_{LOAD}$ = 25Ω, $C_{LOAD}$ = 10pF

| Characteristic | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Supply voltage $V_{DD}$-$V_{DG}$, $V_{AD}$-$V_{AG}$ (Operating) | 4.5 | 5.0 | 5.5 | V |
| Maximum reference current, $I_{REF}$ (See note 1) | 625 | 780 | | μA |
| Maximum output current (See note 1) | 40 | 50 | | mA |
| Reference amplifier input range, $V_{REF}$ | 0.1 | 1.0 | 3.0 | V |
| DC power dissipation (See note 1) | | 200 | | mW |
| Minimum clock rate (See note 2) | | 1 | 10 | kHz |
| Maximum clock rate | 35 | 50 | | MHz |
| Integral nonlinearity | | | ±1.0 | LSB |
| Differential nonlinearity | | ±0.3 | ±0.5 | LSB |
| Full scale error (untrimmed) | | 1.0 | 3.0 | % |
| Output compliance (See note 3) | 1.0 | 1.3 | | V |
| Settling time to - 8 bits (See note 4)<br>7 bits | | 35<br>25 | | ns |
| Rise time | | 1.6 | 2.5 | ns |
| Fall time | | 3.1 | 4.1 | ns |
| Input High Voltage, $V_{IH}$ (Pull Down) | 2.4 | | | V |
| Input Low Voltage, $V_{IL}$ (Pull Down) | | | 1.5 | V |

NOTES:

1. Application dependent: $I_{OUT}max = 64 \times I_{REF}$, where $I_{REF} = V_{REF} / R_{REF}$; DC power = $64 \times I_{REF} \times (V_{AD}-V_{OUT})$
2. At +125°C 50/50 mark/space ratio clock, not production tested. For single shot operation, the MA6670 can be clocked below this rate provided that the CK input is not held high for more than 500μs.
3. For 0.1% change in output current (Compliance is independent of full scale current).
4. To +1 LSB for full scale transition, $R_{LOAD}$ double terminated 50Ω, $f_{CK}$ = 1.6MHz, not production tested.

## TYPICAL OPERATING CONDITIONS

The full scale output current is related to the reference current as follows:

$$I_{OUT}max = 64 \times I_{REF}$$

where $I_{REF} = V_{REF} / R_{REF}$

Table 1 shows typical operating conditions for $V_{REF}$ = 1V

| $I_{OUT}$ load resistor | $I_{OUT}$ max | $R_{REF}$ | $I_{REF}$ |
|---|---|---|---|
| 25Ω | 40.0mA | 1.6kΩ | 625μA |
| 37.5Ω | 26.7mA | 2.4kΩ | 417μA |
| 50Ω | 20.0mA | 3.2kΩ | 313μA |
| 75Ω | 13.3mA | 4.8kΩ | 208μA |

*Table 1. Typical operating conditions for $V_{REF}$ = 1V*

## OPERATING NOTES

The MA6670 uses a current source array to drive 1 volt full scale into loads ranging from 25Ω to 75Ω. Current is switched between complementary outputs by the digital input word.

Input data is latched on the rising edge of the clock and decoded. The decoded data is latched into the current source array on the falling edge of the clock and the analog value is output.

The full scale current output is programmed by applying a voltage reference. A reference amplifier is used to establish the reference current through a reference resistor.

An enable line is provided which switches off the internal current reference when taken logic low and so disables the output. This powers down the DAC which then only consumes power associated with the digital circuitry switching.

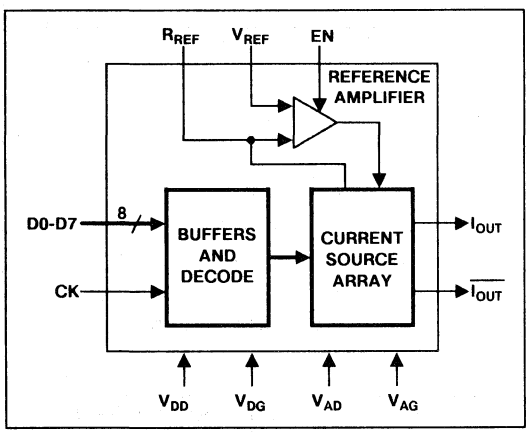



*Fig. 2 Block Diagram*

## PIN DESCRIPTIONS

**D0-D7** Digital data inputs - D0 is the least significant bit with D7 the most significant bit.

**CK** Clock input - Data is latched on the rising edge of the clock and the analog output is updated on the falling edge of the clock.

**$I_{OUT}$** Current output - With D0-D7 logic high, full scale current is output and with D0-D7 logic low, no current is output.

**$\overline{I_{OUT}}$** Complementary current output - With D0-D7 logic high, no current is output and with D0-D7 logic low, full scale current is output.

**$V_{REF}$** Voltage reference input - Used to establish the full scale analog output.

**$R_{REF}$** Reference resistor connection - Used to sense the reference current generated by the current source array in establishing the full scale analog output.

**EN** Reference amplifier enable input - For normal operation, EN should be held at $V_{AD}$. With EN held at $V_{AG}$, the reference amplifier powers down and the analog outputs source no current. Note that this input disables the DAC by powering down the reference amplifier and so should not be used if a fast response is required.

**$V_{AD}$** Analog positive supply.

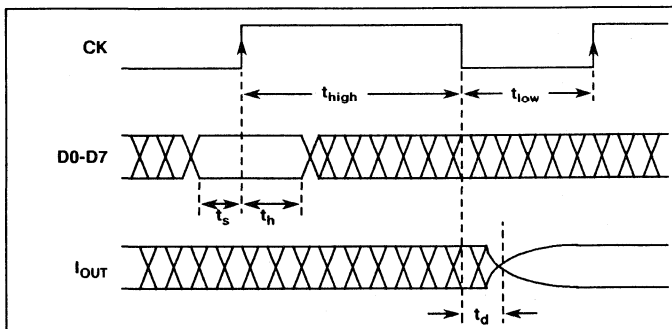
**$V_{AG}$** Analog ground.

**$V_{DD}$** Digital positive supply.

**$V_{DG}$** Digital ground.

## DYNAMIC CHARACTERISTICS

| Parameter | Typ. | Units |
|---|---|---|
| Data set-up, $t_s$ | 1.0 | ns |
| Data hold, $t_h$ | 4.5 | ns |
| Minimum clock pulse width, $t_{high}$ | 5.0 | ns |
| Minimum clock pulse separation, $t_{low}$ | 5.0 | ns |
| Output propagation delay, $t_d$ | 13.5 | ns |




Input data is latched on the rising edge of the clock and the digital-to-analog conversion takes place on the falling edge of the clock. This scheme allows the converter to be used in a one-shot mode.

*Fig. 3 General timing Diagram*

## APPLICATION NOTES

Fig. 4 shows the circuitry required to configure the MA6670 as an 8-bit DAC with a 50Ω output impedance and capable of driving a 50 ohmΩ terminated load with 1.0V peak.

Double termination is recommended because it allows each end of a transmission line to be correctly terminated resulting in minimum reflection and good signal accuracy. Also, the low impedance results in a fast signal fall time which is governed by the RC time constant of the load.

Both analog outputs, whether used or not, should drive matched loads.

Analog and digital supplies are separated to reduce digital noise from appearing on the analog outputs. Printed circuit board layout with ground and power planes is recommended for maximum performance, as is the use of chip capacitors mounted as close to the device as possible for decoupling.

The $R_{REF}$ pin is a relatively high impedance point which should be shielded from any noise source (data inputs, random logic, analog outputs) to ensure stable current source operation.

Any suitable voltage reference upto 3V can be used. The full scale output current can be trimmed by setting the logic inputs to full scale and adjusting $R_{REF}$ until $I_{OUT}$ reaches full scale.

The analog output is updated on the falling edge of the clock. The output will settle to the required accuracy in the settling time specified in the table of Electrical Characteristics. In high accuracy applications, attention must be paid to digital feedthrough to the analog outputs on the rising edge of the clock caused by non-ideal analog-digital isolation. The resulting breakthrough may not be a problem.

In many applications such as video signal reconstruction or waveform synthesis, the analog output will be low pass filtered with cut-off below the Nyquist frequency. This should eliminate digital feedthrough.

In applications such as analog-to-digital conversion, a high speed DAC may be used to reconstruct an analog conversion in a half-flash or successive approximation ADC. Full accuracy may be achieved by ensuring that the DAC output is sampled after the specified settling time and before the rising edge of the DAC clock.

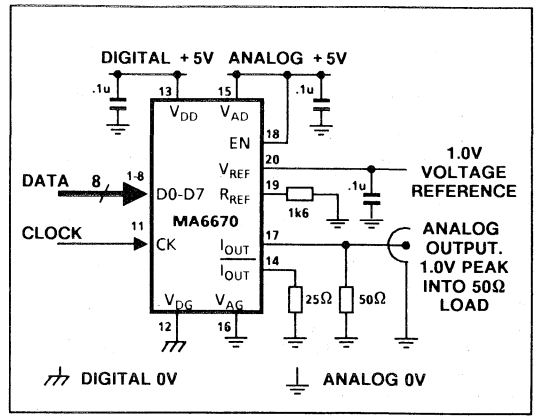



*Fig. 4 Typical application*

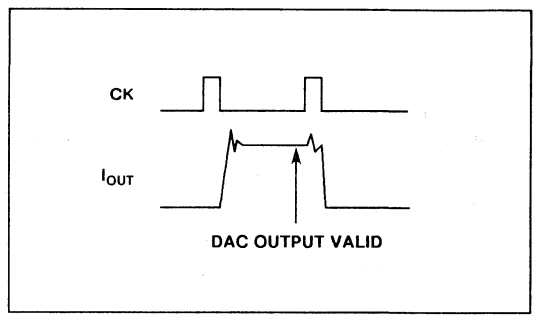



*Fig. 5 $I_{OUT}$ clocking for high speed operation*

The DAC clocking is very flexible in that the clock can be high or low for less than 10ns and so digital feedthrough can be positioned in time relative to the transitions of the analog output. Fig. 5 illustrates how maximum speed and accuracy is achieved by using an unequal mark-space ratio clock.

# MA6672

## HIGH SPEED 10-BIT DIGITAL-TO-ANALOG CONVERTER

The MA6672 is a high speed CMOS digital-to-analog converter with complementary current outputs. The architecture has been optimised to drive doubly terminated 50Ω and 75Ω loads with 1V levels for maximum speed and minimum settling time.

The MA6672 incorporates separate analog and digital power supplies to minimise noise on the analog outputs. The pin placing facilitates the design of low noise printed circuit boards with ground planes, for maximum performance.

A single clock pulse is required to latch the digital input data and update the analog output, allowing single shot or continuous operation.

The MA6672 can be switched to a powered down state.

### FEATURES

- 10-bit Monotonicity
- ±0.3 LSB Typical Differential Non-linearity
- ±1.0 LSB Integral Non-linearity
- 25Ω Drive Capability
- 35MHz Update Rate
- Single Shot or Clocked Operation
- Single 5V Supply
- Output Switchable to High-Z / Power Down

### APPLICATIONS

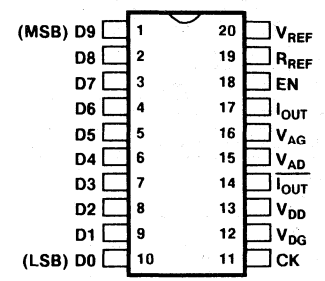
- High Speed DSP
- Video Signal Reconstruction
- High Accuracy, High Speed Waveform Synthesis
- Analog Reconstruction in High Performance Subranging or Residue Analog-to-Digital Converters

### ORDERING INFORMATION

**MA6672PLF** – Plastic DIL (DP), –40°C to +85°C

The following device is supplied non-standard; contact your local GEC Semiconductors Sales Outlet for details:

**MA6672CCC** – Ceramic DIL (DG), –55°C to +125°C




**DG20**
**DP20**

| | |
|---|---|
| $V_{DD}$ | Digital positive supply |
| $V_{DG}$ | Digital ground |
| $V_{AD}$ | Analog positive supply |
| $V_{AG}$ | Analog ground |
| $I_{OUT}$ | Current output |
| $\overline{I_{OUT}}$ | Complementary current output |
| $V_{REF}$ | Voltage reference input |
| $R_{REF}$ | Reference resistor |
| CK | Clock input |
| D0-D9 | Digital data inputs (D9 most significant) |
| EN | Enable input, active high |

*Fig.1 Pin connections - top view*

## ABSOLUTE MAXIMUM RATINGS

| Parameter | Min. | Max. | Units |
|---|---|---|---|
| Supply Voltage $V_{DD}$-$V_{DG}$, $V_{AD}$-$V_{AG}$ | -0.3 | 11 | V |
| Digital input Voltage | $V_{DG}$-0.3 | $V_{DD}$+0.3 | V |
| Operating Temperature (Note 1) | -40 | 85 | °C |
| Storage temperature | -55 | 150 | °C |

*Stresses above those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions, or at any other condition above those indicated in the operations section of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

NOTE 1:Devices are supplied to the industrial temperature range, -40°C to +85°C, as standard. Devices can also be supplied to the military temperature range, -55°C to +125°C; contact your local GEC Semiconductors Sales Outlet for details.

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$V_{DD}$ = 5V, $V_{AD}$ = 5V, $V_{REF}$ = 1.0V, $I_{REF}$ = 625μA, $R_{REF}$ = 1.6kΩ, $R_{LOAD}$ = 25Ω, $C_{LOAD}$ = 10pF

| Characteristic | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| Supply voltage $V_{DD}$-$V_{DG}$, $V_{AD}$-$V_{AG}$ (Operating) | 4.5 | 5.0 | 5.5 | V |
| Maximum reference current, $I_{REF}$ (See note 1) | 625 | 780 | | μA |
| Maximum output current (See note 1) | 40 | 50 | | mA |
| Reference amplifier input range, $V_{REF}$ | 0.1 | 1.0 | 3.0 | V |
| DC power dissipation (See note 1) | | 200 | | mW |
| Minimum clock rate (See note 2) | | 1 | 10 | kHz |
| Maximum clock rate | 35 | 50 | | MHz |
| Integral nonlinearity | | | ±1.0 | LSB |
| Differential nonlinearity | | ±0.3 | ±0.5 | LSB |
| Full scale error (untrimmed) | | 1.0 | 3.0 | % |
| Output compliance (See note 3) | 1.0 | 1.3 | | V |
| Settling time to - 10 bits (See note 4)<br>9 bits<br>8 bits<br>7 bits | | 80<br>45<br>35<br>25 | | ns |
| Rise time | | 1.6 | 2.5 | ns |
| Fall time | | 3.1 | 4.1 | ns |
| Input High Voltage, $V_{IH}$ (Pull Down) | 2.4 | | | V |
| Input Low Voltage, $V_{IL}$ (Pull Down) | | | 1.5 | V |

NOTES:

1. Application dependent: $I_{OUT}max = 64 \times I_{REF}$, where $I_{REF} = V_{REF} / R_{REF}$; DC power = $64 \times I_{REF} \times (V_{AD}-V_{OUT})$
2. At +125°C 50/50 mark/space ratio clock, not production tested. For single shot operation, the MA6670 can be clocked below this rate provided that the CK input is not held high for more than 500μs.
3. For 0.1% change in output current (Compliance is independent of full scale current).
4. To +1 LSB for full scale transition, $R_{LOAD}$ double terminated 50Ω, $f_{CK}$ = 1.6MHz, not production tested.

## TYPICAL OPERATING CONDITIONS

The full scale output current is related to the reference current as follows:

$$I_{OUT}max = 64 \times I_{REF}$$

where $I_{REF} = V_{REF} / R_{REF}$

Table 1 shows typical operating conditions for $V_{REF}$ = 1V

| $I_{OUT}$ load resistor | $I_{OUT}$ max | $R_{REF}$ | $I_{REF}$ |
|---|---|---|---|
| 25Ω | 40.0mA | 1.6kΩ | 625μA |
| 37.5Ω | 26.7mA | 2.4kΩ | 417μA |
| 50Ω | 20.0mA | 3.2kΩ | 313μA |
| 75Ω | 13.3mA | 4.8kΩ | 208μA |

*Table 1. Typical operating conditions for $V_{REF}$ = 1V*

## OPERATING NOTES

The MA6672 uses a current source array to drive 1 volt full scale into loads ranging from 25Ω to 75Ω. Current is switched between complementary outputs by the digital input word.

Input data is latched on the rising edge of the clock and decoded. The decoded data is latched into the current source array on the falling edge of the clock and the analog value is output.

The full scale current output is programmed by applying a voltage reference. A reference amplifier is used to establish the reference current through a reference resistor.

An enable line is provided which switches off the internal current reference when taken logic low and so disables the output. This powers down the DAC which then only consumes power associated with the digital circuitry switching.

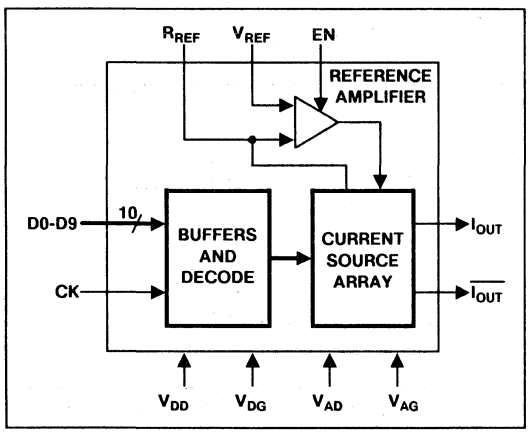



*Fig. 2 Block Diagram*

## PIN DESCRIPTIONS

**D0-D9** Digital data inputs - D0 is the least significant bit with D9 the most significant bit.

**CK** Clock input - Data is latched on the rising edge of the clock and the analog output is updated on the falling edge of the clock.

**$I_{OUT}$** Current output - With D0-D9 logic high, full scale current is output and with D0-D9 logic low, no current is output.

**$\overline{I_{OUT}}$** Complementary current output - With D0-D9 logic high, no current is output and with D0-D9 logic low, full scale current is output.

**$V_{REF}$** Voltage reference input - Used to establish the full scale analog output.

**$R_{REF}$** Reference resistor connection - Used to sense the reference current generated by the current source array in establishing the full scale analog output.

**EN** Reference amplifier enable input - For normal operation, EN should be held at $V_{AD}$. With EN held at $V_{AG}$, the reference amplifier powers down and the analog outputs source no current. Note that this input disables the DAC by powering down the reference amplifier and so should not be used if a fast response is required.

**$V_{AD}$** Analog positive supply.

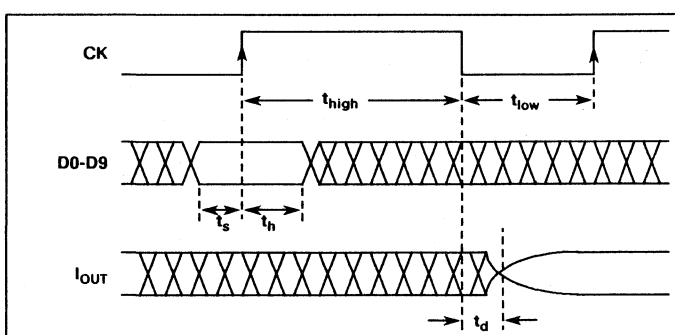
**$V_{AG}$** Analog ground.

**$V_{DD}$** Digital positive supply.

**$V_{DG}$** Digital ground.

## DYNAMIC CHARACTERISTICS

| Parameter | Typ. | Units |
|---|---|---|
| Data set-up, $t_s$ | 1.0 | ns |
| Data hold, $t_h$ | 4.5 | ns |
| Minimum clock pulse width, $t_{high}$ | 5.0 | ns |
| Minimum clock pulse separation, $t_{low}$ | 5.0 | ns |
| Output propagation delay, $t_d$ | 13.5 | ns |




Input data is latched on the rising edge of the clock and the digital-to-analog conversion takes place on the falling edge of the clock. This scheme allows the converter to be used in a one-shot mode.

*Fig. 3 General timing Diagram*

## APPLICATION NOTES

Fig. 4 shows the circuitry required to configure the MA6672 as a 10-bit DAC with a 50Ω output impedance and capable of driving a 50 ohmΩ terminated load with 1.0V peak.

Double termination is recommended because it allows each end of a transmission line to be correctly terminated resulting in minimum reflection and good signal accuracy. Also, the low impedance results in a fast signal fall time which is governed by the RC time constant of the load.

Both analog outputs, whether used or not, should drive matched loads.

Analog and digital supplies are separated to reduce digital noise from appearing on the analog outputs. Printed circuit board layout with ground and power planes is recommended for maximum performance, as is the use of chip capacitors mounted as close to the device as possible for decoupling.

The $R_{REF}$ pin is a relatively high impedance point which should be shielded from any noise source (data inputs, random logic, analog outputs) to ensure stable current source operation.

Any suitable voltage reference upto 3V can be used. The full scale output current can be trimmed by setting the logic inputs to full scale and adjusting $R_{REF}$ until $I_{OUT}$ reaches full scale.

The analog output is updated on the falling edge of the clock. The output will settle to the required accuracy in the settling time specified in the table of Electrical Characteristics. In high accuracy applications, attention must be paid to digital feedthrough to the analog outputs on the rising edge of the clock caused by non-ideal analog-digital isolation. The resulting breakthrough may not be a problem.

In many applications such as video signal reconstruction or waveform synthesis, the analog output will be low pass filtered with cut-off below the Nyquist frequency. This should eliminate digital feedthrough.

In applications such as analog-to-digital conversion, a high speed DAC may be used to reconstruct an analog conversion in a half-flash or successive approximation ADC. Full accuracy may be achieved by ensuring that the DAC output is sampled after the specified settling time and before the rising edge of the DAC clock.

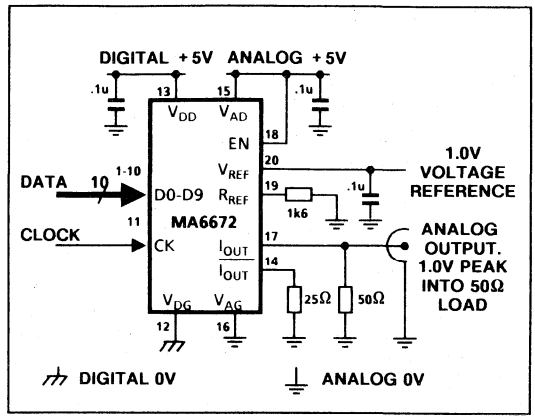



*Fig. 4 Typical application*

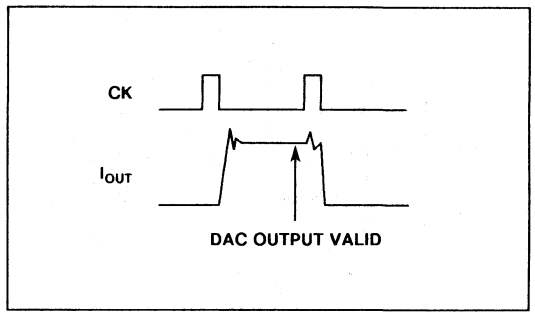



*Fig. 5 $I_{OUT}$ clocking for high speed operation*

The DAC clocking is very flexible in that the clock can be high or low for less than 10ns and so digital feedthrough can be positioned in time relative to the transitions of the analog output. Fig. 5 illustrates how maximum speed and accuracy is achieved by using an unequal mark-space ratio clock.

# MV95308

## 30MHz 8-BIT CMOS VIDEO DAC

The MV95308 is a CMOS 8-bit, 30MHz Digital to Analog converter, designed for use in both video graphics and general digital television applications.

A very low external component count has been achieved by including the loop amplifer and reference voltage source on chip.

The device contains a data input register and registered video controls ($\overline{\text{BLANK}}$, $\overline{\text{REFWHITE}}$, $\overline{\text{OVERBRT}}$ and $\overline{\text{SYNC}}$). These control inputs and associated internal circuitry allows the MV95308 to be used in video graphics systems by providing the necessary video pedestal levels. The $\overline{\text{STRDAC}}$ input allows the video pedestals to be disabled in conventional DAC applications.

This device is capable of directly driving 75Ω lines with standard RS-343A or RS-170 video levels, using the appropriate $R_{SET}$ external resistor.

Pull up resistors have been added to tie all unused control inputs into their inactive (High) states.

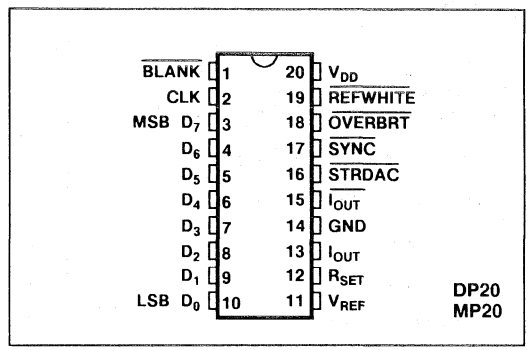



*Fig.1 Pin connections - top view*

### FEATURES

- Low Power Consumption(180mW Typ)
- 30MHz Pipeline Operation
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Levels
- On Chip Reference Voltage Source
- Guaranteed Monotonic
- Drives 75Ω Loads Directly
- Single 5V Power Supply

### APPLICATIONS

- Data Conversion (general)
- Computer Graphics
- Waveform Synthesis
- Consumer TV
- Instrumentation

### ORDERING INFORMATION

**MV95308 CDP** (Commercial - Plastic DIL Package)
**MV95308 CMP** (Commercial - Miniature Plastic DIL Package)

### ABSOLUTE MAXIMUM RATINGS (Reference to GND)

| | |
|---|---|
| DC Supply Voltage, $V_{DD}$ | -0.3V to +7V |
| Digital Input Voltage | -0.3V to $V_{DD}$ + 0.3V |
| Analog Output Short Circuit Duration | Indefinite |
| Ambient Operating Temperature | 0°C to +70°C |
| Storage Temperature Range | -55°C to +125°C |

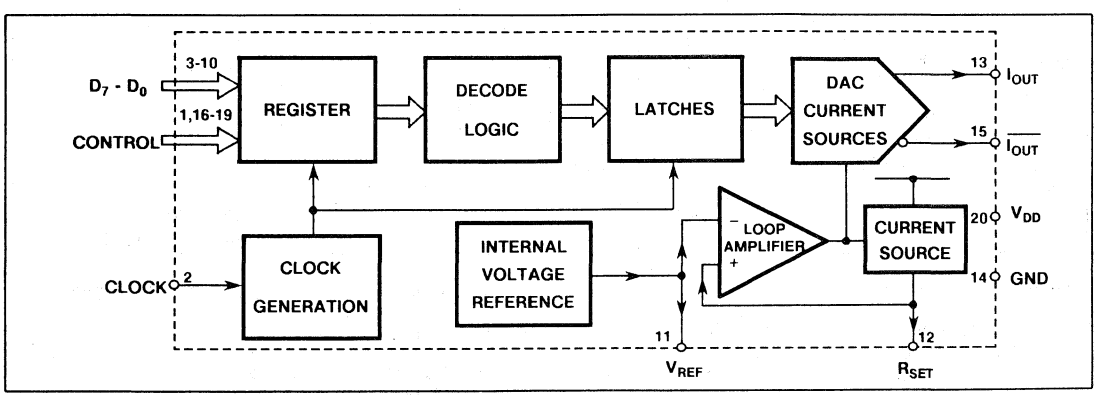



*Fig.2 Block diagram of MV95308*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
As specified in recommended operating conditions. Full temperature range = 0 to 70°C

### DC CHARACTERISTICS

| Parameter | Symbol | Temp (°C) | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | | Full | 8 | | | Bits | |
| Integral Linearity Error | INL | 25 | | ±0.5 | | LSB | |
| | | Full | | | ±1 | LSB | |
| Differential Linearity Error | DNL | 25 | | ±0.5 | | LSB | |
| | | Full | | | ±1 | LSB | |
| Gain Error | | 25 | | ±1% | ±5% | % | Of Full Scale |
| **Analog Output** | | | | | | | |
| Grey scale Current range | | 25 | | 8.8 | | mA | 75Ω Singly Terminated Load $R_{SET}$ = 1.8kΩ (Graphics Mode) |
| | | | | 255 | | LSB | |
| 10% Over Bright Level Relative to White Level | | 25 | 26 | 27 | 28 | LSB | |
| | | | | 10 | | IRE | |
| White Level Relative to Blank Level | | 25 | 275 | 276 | 277 | LSB | |
| | | | | 100 | | IRE | |
| Black Level Relative to Blank Level | | 25 | 20 | 21 | 22 | LSB | |
| | | | | 7.5 | | IRE | |
| White Level Relative to Black Level | | 25 | | 255 | | LSB | |
| | | | | 92.5 | | IRE | |
| Blank Level | | 25 | 107 | 111 | 115 | LSB | |
| | | | | 40 | | IRE | |
| Sync Level | | 25 | | 0 | | LSB | |
| LSB Size | LSB | 25 | | 2.58 | | mV | |
| Output Compliance | $V_{OC}$ | 25 | -0.3 | | +1.5 | V | |
| **DIGITAL INPUTS** | | | | | | | |
| High Level I/P Voltage | $V_{IH}$ | 25 | 3 | | $V_{DD}$ +0.3 | V | |
| Low Level I/P Voltage | $V_{IL}$ | 25 | GND -0.3 | | 1.2 | V | |
| High level I/P Current | $I_{IH}$ | 25 | | | +1 | µA | |
| Low Level I/P Current | $I_{IL}$ | 25 | | | -1 | µA | |
| Internal Voltage Reference ($V_{REF}$) | $V_{REF}$ | 25 | 0.95 | 1.0 | 1.05 | V | |
| | | Full | 0.90 | | 1.10 | V | |
| $V_{REF}$ Temperature Coefficient | | | | 40 | | ppm/°C | |

### AC CHARACTERISTICS (Refer to Fig. 3)

| Parameter | Symbol | Temp (°C) | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Max Clock Rate | $f_{MAX}$ | Full | 30 | | | MHz | Maximum Guaranteed Freq. |
| Clock High Time | $t_{CLKH}$ | 25 | 10 | | | ns | |
| Clock Low Time | $t_{CLKL}$ | 25 | 10 | | | ns | |
| Data and Control Setup Time | $t_{SU}$ | 25 | 8 | | | ns | |
| Data and Control hold Time | $t_H$ | 25 | 2 | | | ns | |
| Analog Output Delay | $t_{DLY}$ | 25 | | 10 | | ns | |
| Analog Output Rise/Fall Time | $t_{RF}$ | 25 | | 3 | 6 | ns | |
| Analog Output Settling Time | $t_S$ | 25 | | 15 | | ns | |
| Glitch Energy | | 25 | | 100 | | pV-sec | |
| $V_{DD}$ Supply Current | IDD | 25 | | 30 | | mA | fc = 15MHz |
| | | | | 36 | | mA | fc = 30MHz |

### THERMAL CHARACTERISTICS

| Thermal Resistance | DP | MP | |
|---|---|---|---|
| Chip to Case $\theta_{jc}$ | 20 | 30 | °C/W |
| Chip to Ambient $\theta_{jA}$ | 75 | 93 | °C/W |

### RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| $R_{LOAD}$ ($I_{OUT}$ and $I_{OUT}$) | 75Ω |
| $V_{DD}$ | 5.0V ±0.5V |
| $R_{SET}$ (Graphics Applications) | 1.8kΩ |
| $R_{SET}$ (Straight DAC Applications) | 1.2kΩ |

## CIRCUIT DESCRIPTION

As illustrated in the function block diagram, Fig. 2, the MV95308 contains an 8-bit D-to-A converter, input registers, a loop amplifier and a voltage reference.

On the falling edge of each clock cycle, as shown in Fig. 3, eight data bits are latched into the device and passed to the 8 bit D-to-A converter. Also latched on the falling edge of the clock signal, the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs add the necessary weighted currents to the analog outputs to produce the required output levels for use in video applications. Table 1 details how the $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, $\overline{\text{REFWHITE}}$ and $\overline{\text{OVERBRT}}$ inputs modify the DAC output levels.

To obtain a high data throughput rate, the decoding logic of the MV95308 is fully pipelined. This introduces a one clock cycle delay between the latching of the input data and the resultant DAC output.

It also ensures synchronisation of the internal data and a minimal output glitch energy.

The DAC employed by the MV95308 eliminates the need for precision component ratios by using a segmented architecture in which equal weight bit currents are either routed to $I_{OUT}$ or $\overline{I_{OUT}}$. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed.

The MV95308 eliminates the need for an external voltage reference by providing a nominally 1.0V reference on chip. An on-chip loop amplifier also provides stability of the full scale output current against power supply and temperature variations. The full scale output current is set by an external resistor $R_{SET}$. By adjustment of this value it is possible to implement RS-343A or RS-170 video levels as explained in the application notes.

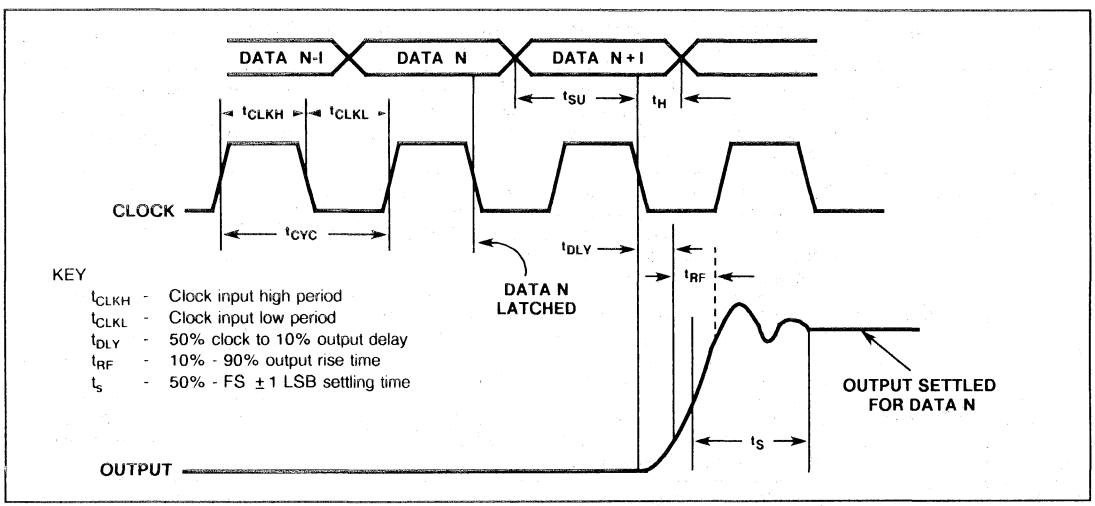



*Fig.3 Timing Diagram*

| Description | $\overline{\text{STRDAC}}$ | $\overline{\text{SYNC}}$ | $\overline{\text{BLANK}}$ | $\overline{\text{REFWHITE}}$ | $\overline{\text{OVERBRT}}$ | INPUT DATA | $I_{OUT}$ (LSB) |
|---|---|---|---|---|---|---|---|
| REFWHITE + 10% | 1 | 1 | 1 | 0 | 0 | × | 414 |
| REFWHITE | 1 | 1 | 1 | 0 | 1 | × | 387 |
| FULL WHITE | 1 | 1 | 1 | 1 | 1 | $FF | 387 |
| OVERBRIGHT | 1 | 1 | 1 | 1 | 0 | DATA | DATA + 132 + 27 |
| FULL BLACK | 1 | 1 | 1 | 1 | 1 | $00 | 132 |
| BLANK | 1 | 1 | 0 | × | × | × | 111 |
| DATA-SYNC | 1 | 0 | 1 | 1 | 1 | DATA | DATA + 21 |
| SYNC | 1 | 0 | 0 | × | × | × | 0 |
| STRDAC MODE | 0 | × | 1 | 1 | × | DATA | DATA |

*Table 1: Video Output Truth Table*

## PIN DESCRIPTIONS

| Pin | Name | Description |
|---|---|---|
| 2 | CLK | **The clock input.** The falling edge of the clock latches the $\overline{\text{DATA}}$, $\overline{\text{BLANK}}$, $\overline{\text{SYNC}}$, $\overline{\text{OVERBRT}}$ and $\overline{\text{REFWHITE}}$ inputs into the logic pipeline. The decoded data will be latched into the DAC output 1 clock cycle later. The clock frequency determines the update rate of the DAC output. |
| 3-10 | $D_7$-$D_0$ | **The data inputs.** $D_0$ is the least significant bit (LSB). The coding is in straight binary only. |
| 13,15 | $I_{OUT}$, $\overline{I_{OUT}}$ | **The current output and it's complement.** These are the high impedance current source outputs of the DAC capable of driving a 75Ω load up to a voltage of 1.5V. |
| 14 | GND | **Analog ground for the DAC.** |
| 20 | $V_{DD}$ | **Analog power for the DAC.** |
| 11 | $V_{REF}$ | **The output of the internal voltage reference generator.** This output is nominally 1V, and should be decoupled with a 10nF capacitor. |
| 12 | $R_{SET}$ | **The full scale adjust control.** The $R_{SET}$ resistor is connected from this pin to ground. An internal loop amplifier adjusts a reference current flowing through the $R_{SET}$ resistor so that the voltage across the resistor is equal to the $V_{REF}$ voltage. This reference current has a weighting equal to 16 LSB's. |
| 1 | $\overline{\text{BLANK}}$ | **The composite blank control input.** A logical zero on this input removes the Black pedestal from the $I_{OUT}$ output, whilst forcing the internal data to the DAC to $00. This input is latched on the clock falling edge and will override the $\overline{\text{REFWHITE}}$ and $\overline{\text{OVERBRT}}$ inputs. The Black pedestal is 7.5 IRE units (actually 21 LSB's). If left open circuit this input is internally tied high. |
| 17 | $\overline{\text{SYNC}}$ | **The composite sync control input.** A logical zero on this input removes the Blank pedestal from the $I_{OUT}$ output. The Blank pedestal is nominally 40 IRE units (actually 111 LSB's). The $\overline{\text{SYNC}}$ input does not override any of the other control lines. This input is latched on the clock falling edge. If left open circuit this input is internally tied high. |
| 19 | $\overline{\text{REFWHITE}}$ | **The reference white level control input.** A logical zero on this input overrides the input data, forcing the data to $FF. The $\overline{\text{BLANK}}$ input will override this input. If left open circuit this input is internally tied high. |
| 18 | $\overline{\text{OVERBRT}}$ | **The 10% overbright control input.** A logical zero on this input switches the Overbright pedestal into the $I_{OUT}$ output. The Overbright pedestal is 10 IRE units (actually 27 LSB's). This input does not override any other input. The $\overline{\text{BLANK}}$ input overrides this input. If left open circuit this input is internally tied high. |
| 16 | $\overline{\text{STRDAC}}$ | **The straight DAC control input.** A logical zero on this input causes the Black, Blank and Overbright pedestals to be disabled, removing them from both $I_{OUT}$ and $\overline{I_{OUT}}$. This allows the DAC contribution to the output to be extended to a full 1 Volt. To obtain this extra DAC range, it is necessary to reduce the $R_{SET}$ resistor value, see application notes. The $\overline{\text{BLANK}}$ and $\overline{\text{REFWHITE}}$ inputs may still be used to force the input data to $00 or $FF respectively. With the $\overline{\text{STRDAC}}$ pin held low the output current can be calculated from:<br><br>Output current = Data × 1 LSB<br><br>Where 1 LSB = $\frac{V_{REF}}{16 \times R_{SET}}$<br><br>Full scale = 255 LSB<br>$V_{REF}$ = 1.0V typ.<br>The exact value of 1 LSB must be calculated from the full scale output.<br><br>If left open circuit this input is internally tied high and the device will be configured for video graphics. In this mode the output current can be calculated from:<br><br>Output current = (DATA + 21 + 111) × 1 LSB<br>$V_{REF}$ = 1.0V typ. |

## APPLICATIONS INFORMATION

### RS-343A and RS-170 Video Generation

For generation of RS-343A compatible video levels (see Fig. 4) it is recommended that a singly terminated 75Ω load be used with an $R_{SET}$ resistor value of approximately 1.82kΩ.

Similarly for the generation of RS-170 video levels a singly terminated 75Ω load should be used, but in association with an $R_{SET}$ value of approximately 1.29kΩ to provide the increased voltage range.

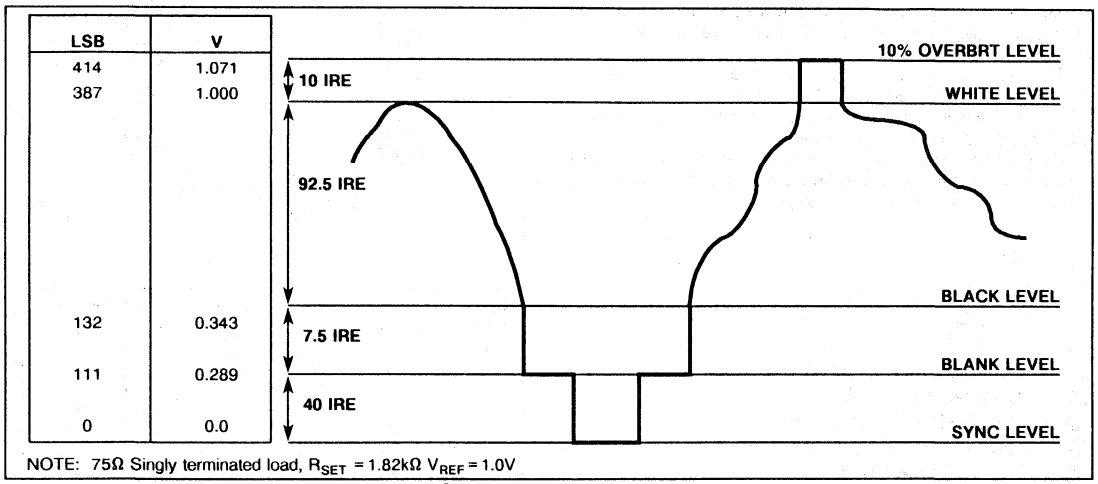
### Non-Video Applications

The MV95308 may be used in non video applications as explained in the pin description for $\overline{STRDAC}$ mode. The relationship between $R_{SET}$ and the full scale output current has been explained previously and for a singly terminated 75Ω load an $R_{SET}$ resistor value of approximately 1.19KΩ should be used.

## PCB LAYOUT CONSIDERATIONS

The PCB layout should provide low noise on the MV95308 power and ground lines by shielding the digital inputs and providing adequate decoupling. The PCB should utilise both power and ground planes for best performance, connecting both planes to their respective regular PCB planes through a ferrite bead located as close as possible to the device. For best performance, a 100nF capacitor should be used to decouple the reference and supply pins. Decoupling should take place as close to the device as possible to reduce lead inductance. The digital inputs to the device should be isolated as much as possible from the analog outputs and other analog circuitry and should not overlay the analog ground and power planes.

To reduce noise pickup, long clock lines to the device should be avoided. For best performance the analog output should have a 75Ω load connected to analog ground.




NOTE: 75Ω Singly terminated load, $R_{SET}$ = 1.82kΩ $V_{REF}$ = 1.0V

*Fig.4. Composite video output waveform*

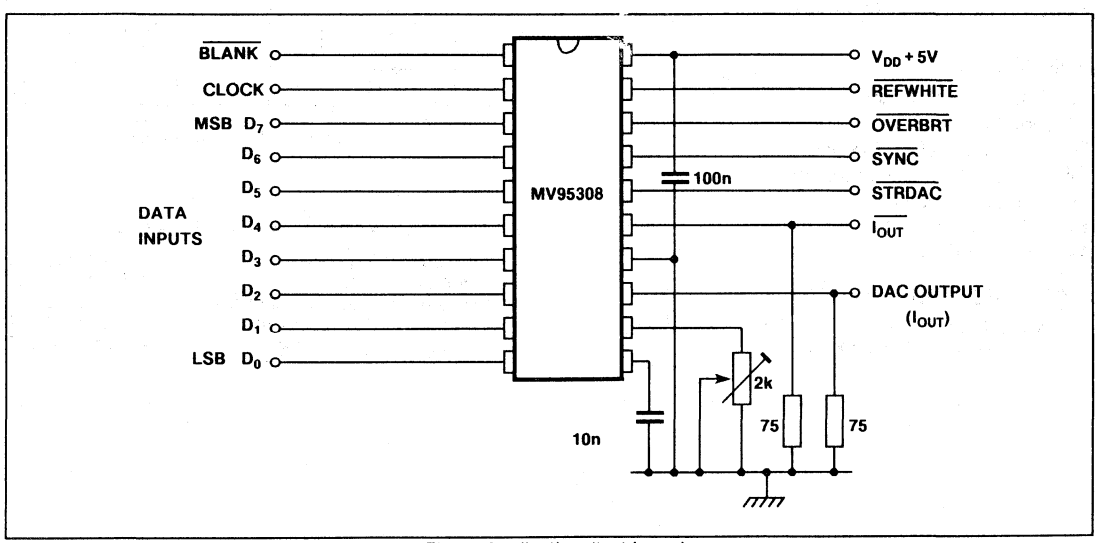



*Fig.5 Applications/test board*

# MV95338

## 30MHz TRIPLE 8-BIT CMOS VIDEO DAC

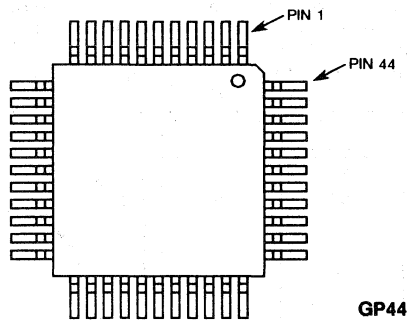
The MV95338 is a CMOS triple 8-bit video DAC designed for use in high resolution television and computer colour graphics.

The device uses video control inputs ($\overline{BLANK}$, $\overline{SYNC}$ and REF WHITE) to provide the MV95338 with the video pedestal levels required to generate RS-343A compatible video signals into a doubly-terminated 75Ω load, or alternatively to produce RS-170 video signals across a singly-terminated 75Ω load.

Data and control inputs are fully pipelined to maintain synchronisation between the DAC outputs.

The full scale output current is defined by an on-chip 1.2V reference and a single resistor.

Differential and integral linearity errors of the D-A converters are guaranteed to be a maximum of ±1LSB over the full operating temperature range.




| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | CLOCK | 16 | $V_{AA}$ | 31 | $R_5$ |
| 2 | $R_0$ | 17 | $V_{AA}$ | 32 | $R_4$ |
| 3 | $R_1$ | 18 | $I_{SYNC}$ | 33 | $B_7$ |
| 4 | $R_2$ | 19 | IOG | 34 | $B_6$ |
| 5 | $R_3$ | 20 | IOR | 35 | $B_5$ |
| 6 | $G_0$ | 21 | IOB | 36 | $B_4$ |
| 7 | $G_1$ | 22 | $\overline{AGND}$ | 37 | $V_{AA}$ |
| 8 | $G_2$ | 23 | $\overline{SYNC}$ | 38 | $V_{AA}$ |
| 9 | $G_3$ | 24 | $\overline{BLANK}$ | 39 | AGND |
| 10 | REF WHITE | 25 | $G_7$ | 40 | AGND |
| 11 | COMP | 26 | $G_6$ | 41 | $B_0$ |
| 12 | $V_{REF\ OUT}$ | 27 | $G_5$ | 42 | $B_1$ |
| 13 | FS ADJUST | 28 | $G_4$ | 43 | $B_2$ |
| 14 | AGND | 29 | $R_7$ | 44 | $B_3$ |
| 15 | AGND | 30 | $R_6$ | | |

*Fig.1 Pin connections - top view.*

### FEATURES

- 30MHz Pipeline Operation
- Triple 8-Bit D-A Converters
- ±1LSB Differential Linearity Error
- ±1LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170 Compatible Levels
- Drives Doubly-Terminated 75Ω Load
- Single 5V Power Supply
- Typical Power Dissipation 500mW
- On-Chip Voltage Reference

### APPLICATIONS

- DBS Broadcast Video
- High Resolution TV
- Computer Colour Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Picture-In-Picture

### ORDERING INFORMATION

**MV95338 C GP** (Commercial - Plastic Leaded Chip Carrier, Gullwing formed leads)

### ABSOLUTE MAXIMUM RATINGS (Referenced to AGND)

| | |
|---|---|
| DC supply voltage, $V_{AA}$ | -0.3V to +7V |
| Digital input voltage | -0.3V to $V_{AA}$ +0.3V |
| Analog output short circuit duration | Indefinite |
| Ambient operating temperature | 0°C to +70°C |
| Storage temperature range | -55°C to +125°C |

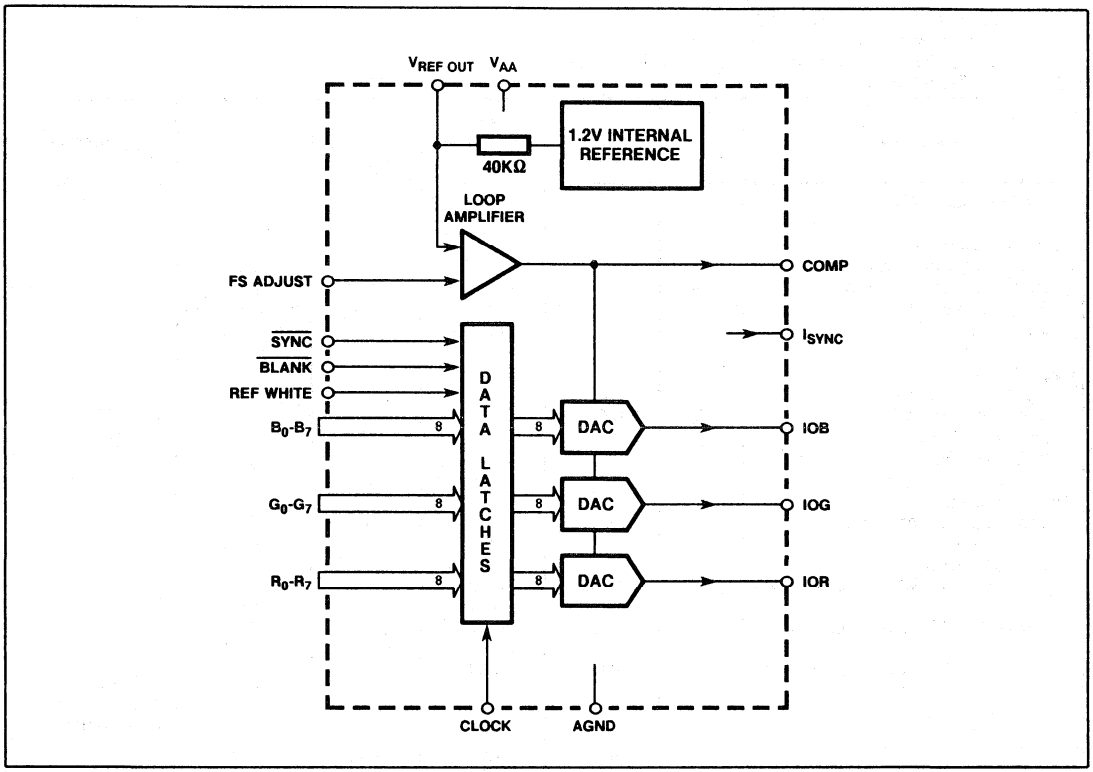



*Fig.2 Functional block diagram of MV95338*

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply voltage | $V_{AA}$ | 4.75 | 5.00 | 5.25 | V | |
| Ambient operating temperature | $T_{amb}$ | 0 | | +70 | °C | |
| Output load | $R_L$ | | 37.5 | | Ω | For RS-343A compatible output levels |
| FS ADJUST resistor | $R_{SET}$ | | 542 | | Ω | |

## THERMAL CHARACTERISTICS

| | GP |
|---|---|
| Thermal resistance, chip-to-case $\theta_{jc}$ | 17 °C/W |
| Thermal resistance, chip-to-ambient $\theta_{jA}$ | 50 °C/W |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
As specified in Recommended Operating Conditions

### DC CHARACTERISTICS

| Parameter | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Resolution (each DAC) | | 8 | | | Bits | |
| **Accuracy (each DAC)** | | | | | | |
| Integral linearity error | INL | | ±0.3 | ±1 | LSB | |
| Differential linearity error | DNL | | ±0.3 | ±1 | LSB | |
| Grey scale error | | | ±1 | ±5 | % grey scale | |
| Monotonicity | | | Guaranteed | | | |
| **Digital Inputs** | | | | | | |
| Input high voltage | $V_{IH}$ | 3.0 | | $V_{AA}$ + 0.3 | V | Binary coding |
| Input low voltage | $V_{IL}$ | AGND-0.3 | | 1.2 | V | |
| Input high current | $I_{IH}$ | | | 1 | μA | |
| Input low current | $I_{IL}$ | | | -1 | μA | |
| **Analog Outputs** | | | | | | |
| Grey scale current range | | 15 | | 20 | mA | |
| | | | 255 | | LSB | |
| **Output currents** | | | | | | |
| White level relative to blank level | | 17.69 | 19.06 | 20.40 | mA | RS-343A tolerances assumed |
| | | | 276 | | LSB | |
| White level relative to black level | | 16.74 | 17.62 | 18.50 | mA | |
| | | | 255 | | LSB | |
| Black level relative to blank level | | 0.95 | 1.44 | 1.90 | mA | |
| | | | 21 | | LSB | |
| Blank level on IOR, IOB | | 0 | 5 | 50 | μA | |
| | | | 0 | | LSB | |
| Blank level on IOG | | 6.29 | 7.62 | 8.96 | mA | |
| | | | 111 | | LSB | |
| Sync level on IOG | | 0 | 5 | 50 | μA | |
| | | | 0 | | LSB | |
| LSB size | | | 69.1 | | μA | |
| DAC to DAC matching | | | 2 | | % | |
| Output compliance | $V_{OC}$ | -0.5 | | +1.4 | V | |
| Reference voltage | $V_{REFOUT}$ | 1.14 | 1.20 | 1.26 | V | |
| Voltage reference temperature coeff. | | | 40 | | ppm/°C | |

### AC CHARACTERISTICS

| Parameter | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max clock rate | $f_{max}$ | 30 | | | MHz | |
| Data and control setup time | $t_{SU}$ | 8 | | | ns | |
| Data and control hold time | $t_H$ | 2 | | | ns | |
| Clock cycle time | $t_{CYC}$ | 33.3 | | | ns | |
| Clock pulse width high time | $t_{CLKH}$ | 10 | | | ns | |
| Clock pulse width low time | $t_{CLKL}$ | 10 | | | ns | |
| Analog output delay | $t_{DLY}$ | | 10 | | ns | |
| Analog output rise/fall time | $t_{VRF}$ | | 6 | 9 | ns | |
| Analog output settling time | $t_S$ | | 15 | | ns | |
| Glitch impulse | | | 100 | | pV-sec | |
| Analog output skew | | | 0 | 3 | ns | |
| Pipeline delay | | 1 | 1 | 1 | Clock | |
| $V_{AA}$ supply current | $I_{AA}$ | | 100 | 140 | mA | At $f_{max}$, $V_{AA}$ = 5V |

## CIRCUIT DESCRIPTION

As shown in Fig. 2, the MV95338 contains three 8-bit D-A converters, input latches, internal voltage reference and a loop amplifier.

On the rising edge of each clock cycle (see Fig. 4), 24 bits of colour information ($R_0$-$R_7$, $G_0$-$G_7$, and $B_0$-$B_7$) are latched into the device and presented to the three 8-bit D-A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, and will force the inputs of each D-A converter to $FF.

$\overline{SYNC}$ and $\overline{BLANK}$ are latched on the rising edge of the clock to maintain synchronisation with the colour data. These inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as shown in Fig. 3. Table 1 details how the $\overline{SYNC}$, $\overline{BLANK}$ and REF WHITE inputs modify the output levels.

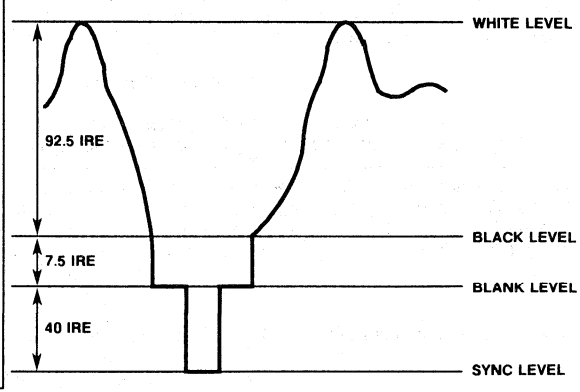
The $I_{SYNC}$ current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If $I_{SYNC}$ is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG and IOB outputs will have the same full scale output current.

Full Scale output current is set by an external resistor ($R_{SET}$) between the FS ADJUST pin and AGND. $R_{SET}$ has a typical value of 542Ω for generation of RS-343A video into a 37.5Ω load.

The D-A converters on the MV95338 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifer stabilizes the full scale output current against temperature and power supply variations.

The analog outputs of the MV95338 are capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω co-axial cable.

| Red/Blue | | Green | |
|---|---|---|---|
| mA | V | mA | V |
| 19.06 | 0.714 | 26.68 | 1.000 |
| 1.44 | 0.054 | 9.06 | 0.340 |
| 0.00 | 0.000 | 7.62 | 0.286 |
| | | 0.000 | 0.000 |




NOTE : 75Ω doubly terminated load, $R_{SET}$ = 542Ω, $V_{REF}$ = 1.2V, $I_{SYNC}$ connected to IOG, RS-343A levels assumed

*Fig.3 Composite video output waveform*

| Description | IOG (mA) | IOR/IOB (mA) | REF WHITE | $\overline{SYNC}$ | $\overline{BLANK}$ | DAC I/P Data |
|---|---|---|---|---|---|---|
| White Level | 26.68 | 19.06 | 1 | 1 | 1 | $XX |
| White Level | 26.68 | 19.06 | 0 | 1 | 1 | $FF |
| Data | Data + 9.06 | Data + 1.44 | 0 | 1 | 1 | Data |
| Data-Sync | Data + 1.44 | Data + 1.44 | 0 | 0 | 1 | Data |
| Black Level | 9.06 | 1.44 | 0 | 1 | 1 | $00 |
| Black-Sync | 1.44 | 1.44 | 0 | 0 | 1 | $00 |
| Blank Level | 7.62 | 0 | X | 1 | 0 | $XX |
| Sync Level | 0 | 0 | X | 0 | 0 | $XX |

NOTE : Typical with full scale IOG = 26.68mA, $R_{SET}$ = 542Ω, $V_{REF}$ = 1.2V, $I_{SYNC}$ connected to IOG

*Table 1 Video output truth table*

## PIN DESCRIPTIONS

| Pin name | Description |
|---|---|
| $\overline{\text{BLANK}}$ | Composite blank control input. A logic '0' forces the IOR, IOG and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logic zero, the $R_0$-$R_7$, $G_0$-$G_7$, $B_0$-$B_7$, and REF WHITE inputs are ignored. |
| $\overline{\text{SYNC}}$ | Composite sync control input. A logic '0' on this input switches off a 40 IRE current source on the $I_{SYNC}$ output. $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Table 1; therefore it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. |
| REF WHITE | Reference white control input. A logic '1' on this input forces the IOR, IOG, and IOB outputs to the white level, regardless of the $R_0$-$R_7$, $G_0$-$G_7$ and $B_0$-$B_7$ inputs. It is latched on the rising edge of CLOCK. See Table 1. |
| $R_0$-$R_7$<br>$G_0$-$G_7$<br>$B_0$-$B_7$ | Red, Green, and Blue data inputs. $R_0$, $G_0$, and $B_0$ are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane. |
| CLOCK | Clock input. The rising edge of CLOCK latches the $R_0$-$R_7$, $G_0$-$G_7$, $B_0$-$B_7$ $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated CMOS buffer. |
| IOR, IOG, IOB | Red, Green and Blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω co-axial cable. All outputs, whether used or not, should have the same output load. |
| $I_{SYNC}$ | Sync current output. Typically this current output is directly wired to the IOG output, and enables sync information to be encoded onto the green channel. A logic '0' on the $\overline{\text{SYNC}}$ input results in no current being output onto this pin, while a logic '1' results in the following current being output:<br>$I_{SYNC}\ (mA) = 3468 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 111$ LSBs<br>If sync information is not required on the green channel, this output may be connected to $V_{AA}$ and the $\overline{\text{SYNC}}$ input tied high, causing the $I_{SYNC}$ current source to be turned off, reducing the power consumption. |
| FS ADJUST | Full scale adjust control. A resistor ($R_{SET}$) connected between this pin and AGND controls the magnitude of the full video signal (Fig. 3). The current flowing in the $R_{SET}$ resistor is equal to 32 LSBs. Note that the IRE relationships in Fig. 3 are maintained, regardless of the full scale output current.<br>The relationship between $R_{SET}$ and the full scale current on IOG (assuming $I_{SYNC}$ is connected to IOG) is:<br>$IOG\ (mA) = 12082 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 387$ LSBs<br>The full scale output current on IOR and IOB for a given $R_{SET}$ is defined as:<br>$IOR, IOB\ (mA) = 8624 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)} \equiv 276$ LSBs |
| COMP | Compensation pin. This pin provides compensation for the internal loop amplifier. A 0.01μF ceramic capacitor must be connected between this pin and the nearest $V_{AA}$ pin. Connecting the capacitor to $V_{AA}$ rather than to AGND provides the highest possible power supply noise rejection. |
| $V_{REF\ OUT}$ | Voltage reference output. The output from an internal reference circuit, providing 1.2V (typical) reference. A 0.1μF ceramic capacitor must be used to decouple this output to $V_{AA}$. |
| AGND | Analog ground. All AGND pins must be connected. |
| $V_{AA}$ | Analog power. All $V_{AA}$ pins must be connected. |

## APPLICATION NOTES

### RS-343A and RS-170 Video Generation

For the generation of RS-343A compatible video levels it is recommended that a doubly terminated 75Ω load be used with an $R_{SET}$ resistor value of a approximately 542Ω.

Similarly for the generation of RS-170 compatible video, it is recommended that a singly terminated 75Ω load be used with an $R_{SET}$ value of about 774Ω. If the MV95338 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75Ω and singly terminated 75Ω loads

If driving a large capacitive load (load $RC > 1/20\Pi f_C$) it is recommended that an output buffer with an unloaded gain > 2 be used to drive a doubly terminated 75Ω load.

### COMP Resistor

To optimise the settling time of the MV95338, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

### Non- Video Applications

The MV95338 may be used in non-video applications by disabling the video specific control inputs. REF WHITE should be logic '0' while $\overline{BLANK}$ and $\overline{SYNC}$ should be a logic '1'. $I_{SYNC}$ should be connected to $V_{AA}$ or AGND. All three outputs will have the same full scale output current.

The relationship between $R_{SET}$ and full scale output current ($I_{out}$) in this configuration is as follows:

$$I_{out}\,(mA) = 7968 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} \equiv 255\ LSBs$$

$$\text{Note that } 1\ LSB \equiv \frac{V_{REF}\,(V)}{32 \times R_{SET}\,(\Omega)}$$

With the data inputs at $00, there is a DC offset current ($I_{min}$) defined as follows:

$$I_{min}\,(mA) = 656 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} \equiv 21\ LSBs$$

Therefore, the total full scale output current will be $I_{out} + I_{min}$. The REF WHITE input may optionally be used as a 'force to full scale' control.

## TIMING WAVEFORMS

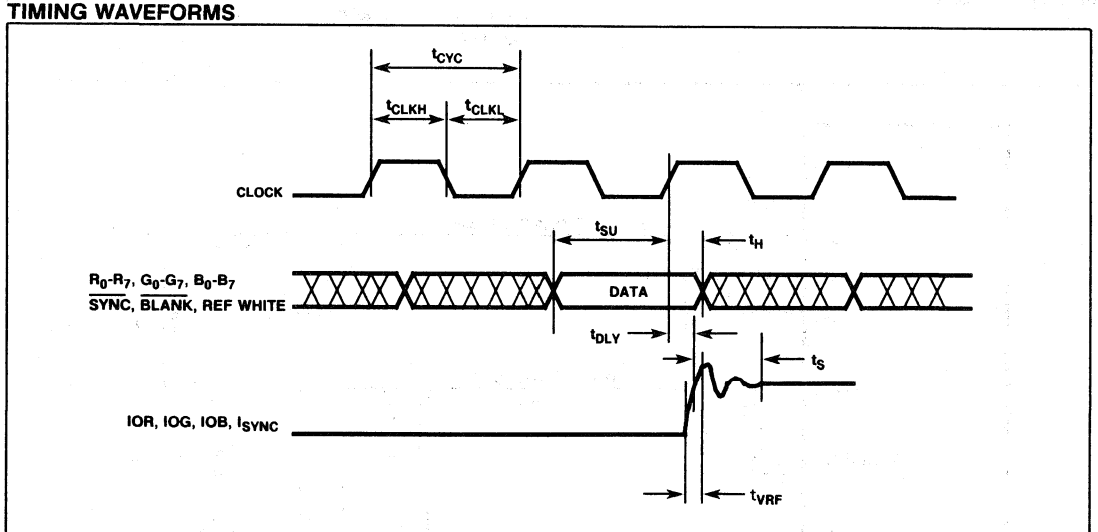



*Fig.4 Input/output timing*

NOTES

1. Output delay, $t_{DLY}$, measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
2. Settling time, $t_S$, measured from the 50% point of full scale transition to the output remaining within ±1 LSB.
3. Output rise/fall time , $t_{VRF}$, measured between the 10% and 90% points of full scale transition.

## PCB LAYOUT CONSIDERATIONS

To obtain the optimum performance from the MV95338 great care must be taken in the PCB layout to ensure low noise power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling.

### Power and Ground Planes

The MV95338 and its associated circuitry should have its own separate power/ground planes, which should be at a single point through ferrite bead. It is important that the regular PCB power and ground planes do not over lay portions of the analog power or ground planes to minimise plane-to-plane noise coupling.

### Digital Signal Interconnect

The digital signal lines to the MV95338 should be isolated as much as possible from the analog circuitry. Due to the high clock rates used, the clock lines to the MV95338 should be as short as possible to minimise noise pickup.

Any pull-up resistors used on the digital inputs should be connected to the regular PCB power plane, not to the analog power plane.

### Supply Decoupling

Noise on the analog power plane will be further reduced by the use of multiple decoupling capacitors (See Fig. 5.)

Optimum performance is obtained with 0.1µF chip ceramic capacitors placed as close as possible to the VAA pins, with the shortest leads possible to reduce lead inductance.

It should be noted that while the loop amplifier circuitry of the MV95338 will reject power supply noise, this rejection decreases with frequency. Any high frequency noise on the regular supply (such as produced by a switch mode power supplies) must be adequately suppressed, else the designer should consider using a three terminal regulator to supply the analog power plane.

### Analog Signal Interconnect

For optimum performance the analog output connectors and source termination resistors should be as close as possible to the MV95338 to minimise noise pickup and reflections due to impedance mismatch. The video output signals should overlay the ground plane and not the analog power plane, to maximise the high frequency power supply rejection.

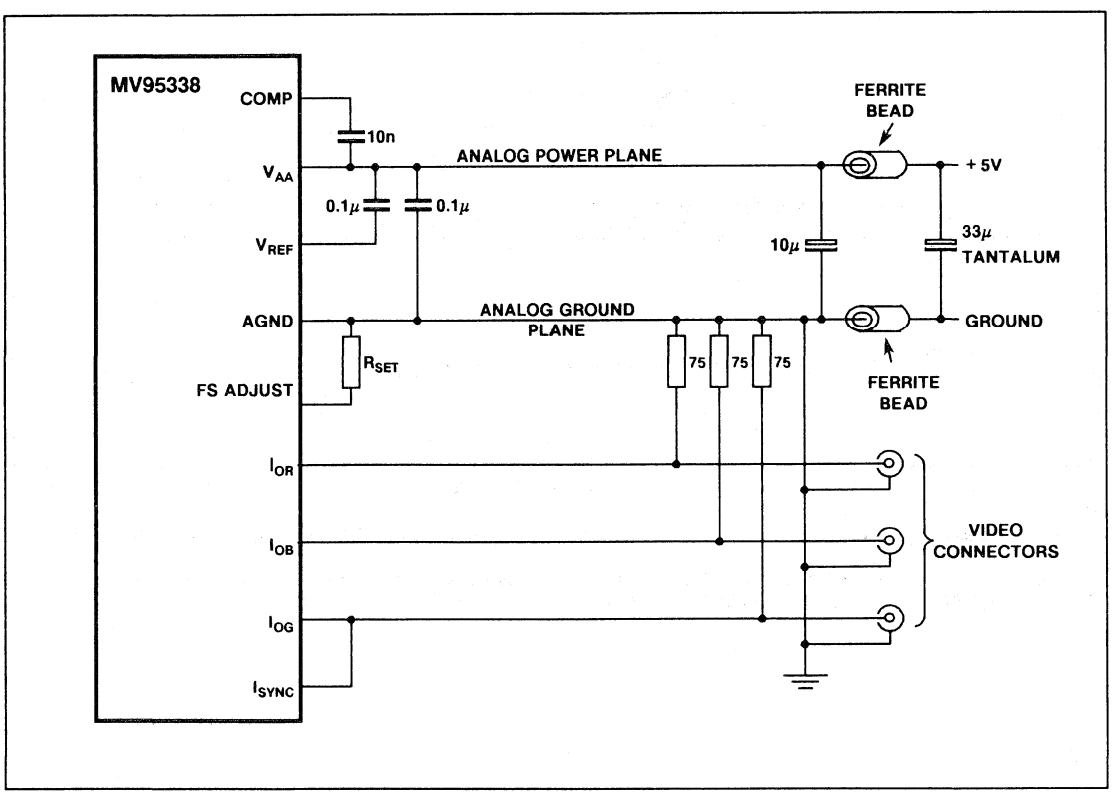



*Fig.5 MV95338 Typical Connections*

# MV95408

## 50MHz 8-BIT CMOS VIDEO DAC

The MV95408 is a CMOS 8-bit, 50MHz Digital to Analog converter, designed for use in both video graphics and general digital television applications.

A very low external component count has been achieved by including the loop amplifer and reference voltage source on chip.

The device contains a data input register and registered video controls ($\overline{\text{BLANK}}$, $\overline{\text{REFWHITE}}$, $\overline{\text{OVERBRT}}$ and $\overline{\text{SYNC}}$). These control inputs and associated internal circuitry allows the MV95408 to be used in video graphics systems by providing the necessary video pedestal levels. The $\overline{\text{STRDAC}}$ input allows the video pedestals to be disabled in conventional DAC applications.

This device is capable of directly driving 75Ω lines with standard RS-343A or RS-170 video levels, using the appropriate $R_{SET}$ external resistor.

Pull up resistors have been added to tie all unused control inputs into their inactive (High) states.

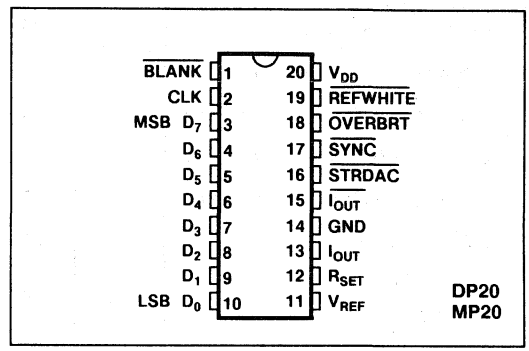



*Fig.1 Pin connections - top view*

### FEATURES

- Low Power Consumption(180mW Typ)
- 50MHz Pipeline Operation
- ±1 LSB Differential Linearity Error
- ±1 LSB Integral Linearity Error
- RS-343A/RS-170 Compatible Levels
- On Chip Reference Voltage Source
- Guaranteed Monotonic
- Drives 75Ω Loads Directly
- Single 5V Power Supply

### APPLICATIONS

- Data Conversion (general)
- Computer Graphics
- Waveform Synthesis
- Commercial TV
- Instrumentation

### ORDERING INFORMATION

**MV95408 BDP** (Commercial - Plastic DIL Package)
**MV95408 BMP** (Commercial - Miniature Plastic DIL Package)

### ABSOLUTE MAXIMUM RATINGS (Reference to GND)

| | |
|---|---|
| DC Supply Voltage, $V_{DD}$ | -0.3V to +7V |
| Digital Input Voltage | -0.3V to $V_{DD}$ +0.3V |
| Analog Output Short Circuit Duration | Indefinite |
| Ambient Operating Temperature | –40°C to +85°C |
| Storage Temperature Range | -55°C to +125°C |

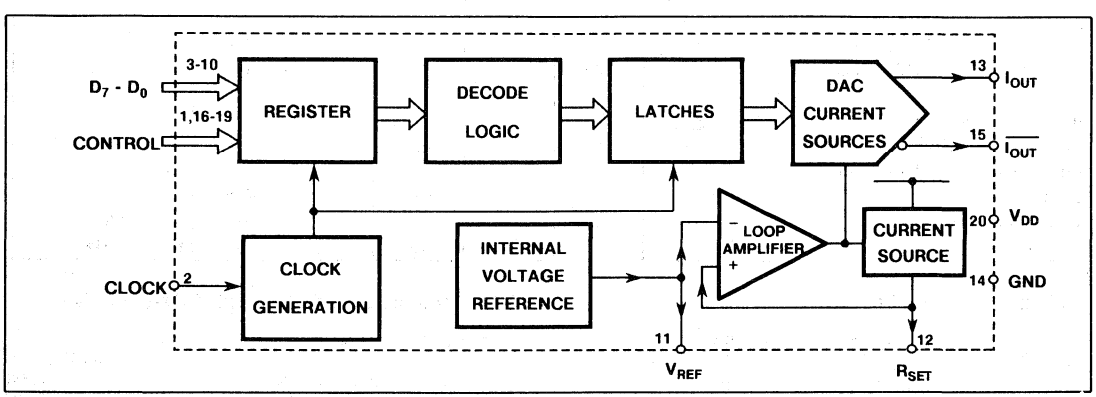



*Fig.2 Block diagram of MV95408*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
As specified in recommended operating conditions. Full temperature range = –40°C to + 85°C

### DC CHARACTERISTICS

| Parameter | Symbol | Temp (°C) | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | | Full | 8 | | | Bits | |
| Integral Linearity Error | INL | 25 | | ±0.5 | | LSB | |
| | | Full | | | ±1 | LSB | |
| Differential Linearity Error | DNL | 25 | | ±0.5 | | LSB | |
| | | Full | | | ±1 | LSB | |
| Gain Error | | 25 | | ±1% | ±5% | % | Of Full Scale |
| **Analog Output** | | | | | | | |
| Grey scale Current range | | 25 | | 8.8 | | mA | 75Ω Singly Terminated Load $R_{SET}$ = 1.8kΩ (Graphics Mode) |
| | | | | 255 | | LSB | |
| 10% Over Bright Level Relative to White Level | | 25 | 26 | 27 | 28 | LSB | |
| | | | | 10 | | IRE | |
| White Level Relative to Blank Level | | 25 | 275 | 276 | 277 | LSB | |
| | | | | 100 | | IRE | |
| Black Level Relative to Blank Level | | 25 | 20 | 21 | 22 | LSB | |
| | | | | 7.5 | | IRE | |
| White Level Relative to Black Level | | 25 | | 255 | | LSB | |
| | | | | 92.5 | | IRE | |
| Blank Level | | 25 | 107 | 111 | 115 | LSB | |
| | | | | 40 | | IRE | |
| Sync Level | | 25 | | 0 | | LSB | |
| LSB Size | LSB | 25 | | 2.58 | | mV | |
| Output Compliance | $V_{OC}$ | 25 | -0.3 | | +1.5 | V | |
| **DIGITAL INPUTS** | | | | | | | |
| High Level I/P Voltage | $V_{IH}$ | 25 | 3 | | $V_{DD}$ +0.3 | V | |
| Low Level I/P Voltage | $V_{IL}$ | 25 | GND -0.3 | | 1.2 | V | |
| High level I/P Current | $I_{IH}$ | 25 | | | +1 | µA | |
| Low Level I/P Current | $I_{IL}$ | 25 | | | -1 | µA | |
| Internal Voltage Reference ($V_{REF}$) | $V_{REF}$ | 25 | 0.95 | 1.0 | 1.05 | V | |
| | | Full | 0.90 | | 1.10 | V | |
| $V_{REF}$ Temperature Coefficient | | | | 40 | | ppm/°C | |

### AC CHARACTERISTICS (Refer to Fig. 3)

| Parameter | Symbol | Temp (°C) | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Max Clock Rate | $f_{MAX}$ | Full | 50 | | | MHz | Maximum Guaranteed Freq. |
| Clock High Time | $t_{CLKH}$ | 25 | 7 | | | ns | |
| Clock Low Time | $t_{CLKL}$ | 25 | 7 | | | ns | |
| Data and Control Setup Time | $t_{SU}$ | 25 | 6 | | | ns | |
| Data and Control hold Time | $t_H$ | 25 | 2 | | | ns | |
| Analog Output Delay | $t_{DLY}$ | 25 | | 10 | | ns | |
| Analog Output Rise/Fall Time | $t_{RF}$ | 25 | | 3 | 6 | ns | |
| Analog Output Settling Time | $t_S$ | 25 | | 15 | | ns | |
| Glitch Energy | | 25 | | 100 | | pV-sec | |
| $V_{DD}$ Supply Current | IDD | 25 | | 30 | | mA | fc = 15MHz |
| | | | | 42 | | mA | fc = 50MHz |

### THERMAL CHARACTERISTICS

| Thermal Resistance | DP | MP | |
|---|---|---|---|
| Chip to Case $\theta_{jc}$ | 20 | 30 | °C/W |
| Chip to Ambient $\theta_{jA}$ | 75 | 93 | °C/W |

### RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| $R_{LOAD}$ ($I_{OUT}$ and $I_{OUT}$) | 75Ω |
| $V_{DD}$ | 5.0V ±0.5V |
| $R_{SET}$ (Graphics Applications) | 1.8kΩ |
| $R_{SET}$ (Straight DAC Applications) | 1.2kΩ |

## CIRCUIT DESCRIPTION

As illustrated in the function block diagram, Fig. 2, the MV95408 contains an 8-bit D-to-A converter, input registers, a loop amplifier and a voltage reference.

On the falling edge of each clock cycle, as shown in Fig. 3, eight data bits are latched into the device and passed to the 8 bit D-to-A converter. Also latched on the falling edge of the clock signal, the $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$ inputs add the necessary weighted currents to the analog outputs to produce the required output levels for use in video applications. Table 1 details how the $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, $\overline{\text{REFWHITE}}$ and $\overline{\text{OVERBRT}}$ inputs modify the DAC output levels.

To obtain a high data throughput rate, the decoding logic of the MV95408 is fully pipelined. This introduces a one clock cycle delay between the latching of the input data and the resultant DAC output.

It also ensures synchronisation of the internal data and a minimal output glitch energy.

The DAC employed by the MV95408 eliminates the need for precision component ratios by using a segmented architecture in which equal weight bit currents are either routed to $I_{OUT}$ or $\overline{I_{OUT}}$. The use of identical current sources and current steering their outputs means that monotonicity is guaranteed.

The MV95408 eliminates the need for an external voltage reference by providing a nominally 1.0V reference on chip. An on-chip loop amplifier also provides stability of the full scale output current against power supply and temperature variations. The full scale output current is set by an external resistor $R_{SET}$. By adjustment of this value it is possible to implement RS-343A or RS-170 video levels as explained in the application notes.

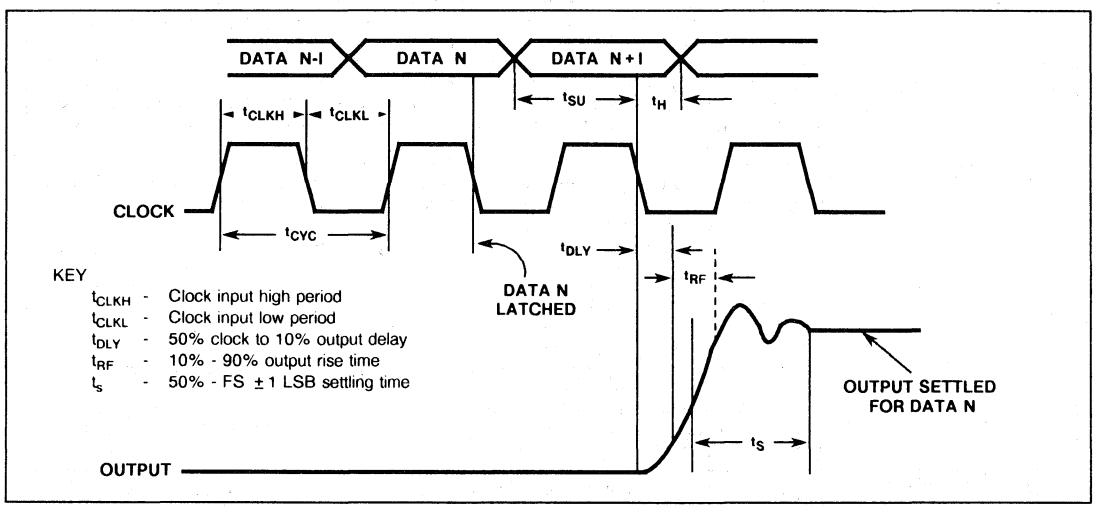



*Fig.3 Timing Diagram*

| Description | $\overline{\text{STRDAC}}$ | $\overline{\text{SYNC}}$ | $\overline{\text{BLANK}}$ | $\overline{\text{REFWHITE}}$ | $\overline{\text{OVERBRT}}$ | INPUT DATA | $I_{OUT}$ (LSB) |
|---|---|---|---|---|---|---|---|
| REFWHITE + 10% | 1 | 1 | 1 | 0 | 0 | × | 414 |
| REFWHITE | 1 | 1 | 1 | 0 | 1 | × | 387 |
| FULL WHITE | 1 | 1 | 1 | 1 | 1 | $FF | 387 |
| OVERBRIGHT | 1 | 1 | 1 | 1 | 0 | DATA | DATA + 132 + 27 |
| FULL BLACK | 1 | 1 | 1 | 1 | 1 | $00 | 132 |
| BLANK | 1 | 1 | 0 | × | × | × | 111 |
| DATA-SYNC | 1 | 0 | 1 | 1 | 1 | DATA | DATA + 21 |
| SYNC | 1 | 0 | 0 | × | × | × | 0 |
| STRDAC MODE | 0 | × | 1 | 1 | × | DATA | DATA |

*Table 1: Video Output Truth Table*

## PIN DESCRIPTIONS

| Pin | Name | Description |
|---|---|---|
| 2 | CLK | **The clock input.** The falling edge of the clock latches the $\overline{DATA}$, $\overline{BLANK}$, $\overline{SYNC}$, $\overline{OVERBRT}$ and $\overline{REFWHITE}$ inputs into the logic pipeline. The decoded data will be latched into the DAC output 1 clock cycle later. The clock frequency determines the update rate of the DAC output. |
| 3-10 | $D_7$-$D_0$ | **The data inputs.** $D_0$ is the least significant bit (LSB). The coding is in straight binary only. |
| 13,15 | $I_{OUT}$, $\overline{I_{OUT}}$ | **The current output and it's complement.** These are the high impedance current source outputs of the DAC capable of driving a 75Ω load up to a voltage of 1.5V. |
| 14 | GND | **Analog ground for the DAC.** |
| 20 | $V_{DD}$ | **Analog power for the DAC.** |
| 11 | $V_{REF}$ | **The output of the internal voltage reference generator.** This output is nominally 1V, and should be decoupled with a 10nF capacitor. |
| 12 | $R_{SET}$ | **The full scale adjust control.** The $R_{SET}$ resistor is connected from this pin to ground. An internal loop amplifier adjusts a reference current flowing through the $R_{SET}$ resistor so that the voltage across the resistor is equal to the $V_{REF}$ voltage. This reference current has a weighting equal to 16 LSB's. |
| 1 | $\overline{BLANK}$ | **The composite blank control input.** A logical zero on this input removes the Black pedestal from the $I_{OUT}$ output, whilst forcing the internal data to the DAC to $00. This input is latched on the clock falling edge and will override the $\overline{REFWHITE}$ and $\overline{OVERBRT}$ inputs. The Black pedestal is 7.5 IRE units (actually 21 LSB's). If left open circuit this input is internally tied high. |
| 17 | $\overline{SYNC}$ | **The composite sync control input.** A logical zero on this input removes the Blank pedestal from the $I_{OUT}$ output. The Blank pedestal is nominally 40 IRE units (actually 111 LSB's). The $\overline{SYNC}$ input does not override any of the other control lines. This input is latched on the clock falling edge. If left open circuit this input is internally tied high. |
| 19 | $\overline{REFWHITE}$ | **The reference white level control input.** A logical zero on this input overrides the input data, forcing the data to $FF. The $\overline{BLANK}$ input will override this input. If left open circuit this input is internally tied high. |
| 18 | $\overline{OVERBRT}$ | **The 10% overbright control input.** A logical zero on this input switches the Overbright pedestal into the $I_{OUT}$ output. The Overbright pedestal is 10 IRE units (actually 27 LSB's). This input does not override any other input. The $\overline{BLANK}$ input overrides this input. If left open circuit this input is internally tied high. |
| 16 | $\overline{STRDAC}$ | **The straight DAC control input.** A logical zero on this input causes the Black, Blank and Overbright pedestals to be disabled, removing them from both $I_{OUT}$ and $\overline{I_{OUT}}$. This allows the DAC contribution to the output to be extended to a full 1 Volt. To obtain this extra DAC range, it is necessary to reduce the $R_{SET}$ resistor value, see application notes. The $\overline{BLANK}$ and $\overline{REFWHITE}$ inputs may still be used to force the input data to $00 or $FF respectively. With the $\overline{STRDAC}$ pin held low the output current can be calculated from:<br><br>Output current = Data × 1 LSB<br><br>Where 1 LSB = $\frac{V_{REF}}{16 \times R_{SET}}$<br><br>Full scale = 255 LSB<br>$V_{REF}$ = 1.0V typ.<br>The exact value of 1 LSB must be calculated from the full scale output.<br><br>If left open circuit this input is internally tied high and the device will be configured for video graphics. In this mode the output current can be calculated from:<br><br>Output current = (DATA + 21 + 111) × 1 LSB<br>$V_{REF}$ = 1.0V typ. |

## APPLICATIONS INFORMATION

### RS-343A and RS-170 Video Generation

For generation of RS-343A compatible video levels (see Fig. 4) it is recommended that a singly terminated 75Ω load be used with an $R_{SET}$ resistor value of approximately 1.82kΩ.

Similarly for the generation of RS-170 video levels a singly terminated 75Ω load should be used, but in association with an $R_{SET}$ value of approximately 1.29kΩ to provide the increased voltage range.

### Non-Video Applications

The MV95408 may be used in non video applications as explained in the pin description for $\overline{STRDAC}$ mode. The relationship between $R_{SET}$ and the full scale output current has been explained previously and for a singly terminated 75Ω load an $R_{SET}$ resistor value of approximately 1.19KΩ should be used.

## PCB LAYOUT CONSIDERATIONS

The PCB layout should provide low noise on the MV95408 power and ground lines by shielding the digital inputs and providing adequate decoupling. The PCB should utilise both power and ground planes for best performance, connecting both planes to their respective regular PCB planes through a ferrite bead located as close as possible to the device. For best performance, a 100nF capacitor should be used to decouple the reference and supply pins. Decoupling should take place as close to the device as possible to reduce lead inductance. The digital inputs to the device should be isolated as much as possible from the analog outputs and other analog circuitry and should not overlay the analog ground and power planes.

To reduce noise pickup, long clock lines to the device should be avoided. For best performance the analog output should have a 75Ω load connected to analog ground.

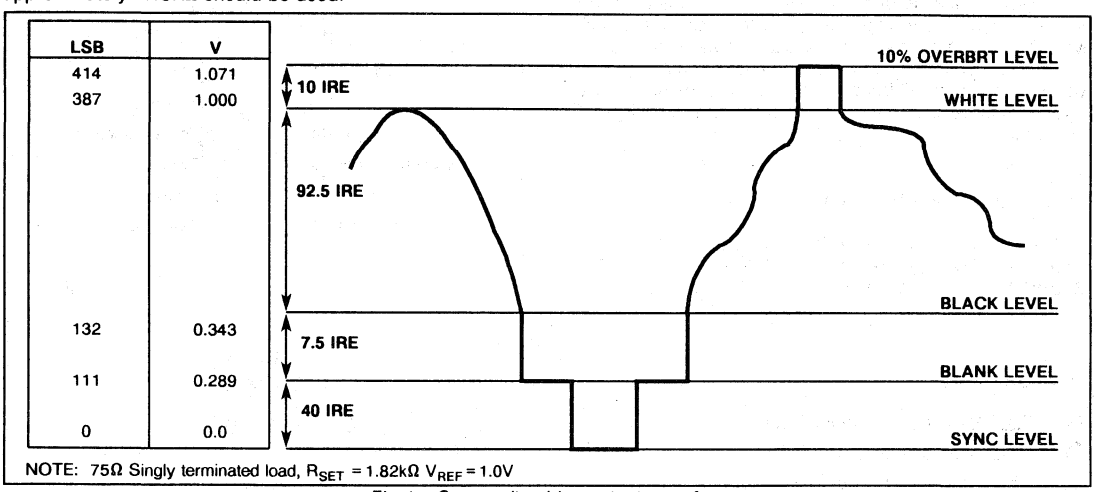



*Fig.4. Composite video output waveform*

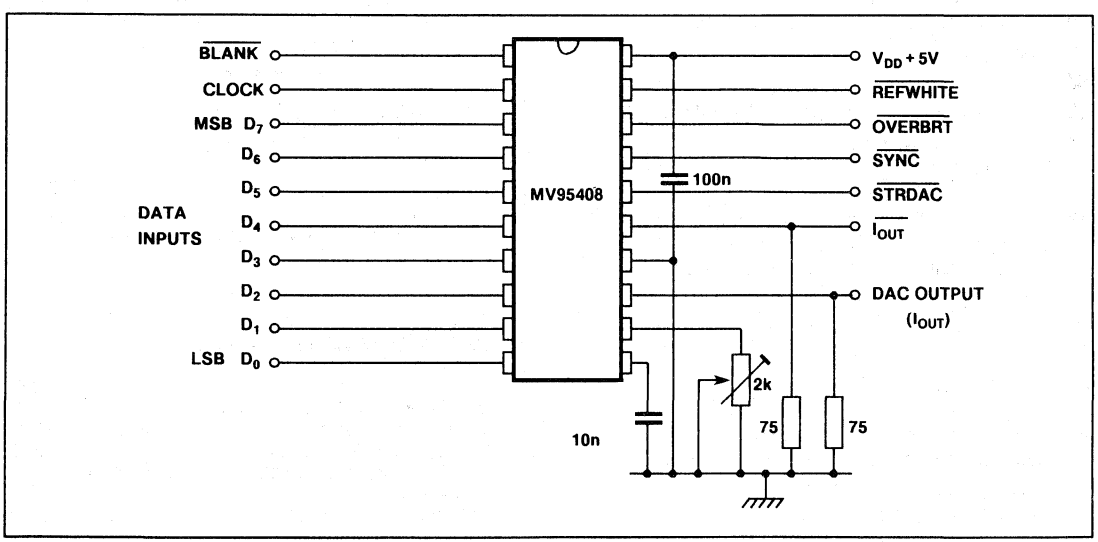



*Fig.5 Applications/test board*

# SL9999

## 400MHz ADC DRIVER-AMPLIFIER

The SL9999 is a monolithic high speed high performance operational amplifier. Although primarily intended to drive the inputs of analog to digital converters, the device is capable of driving any other circuit including those that present a low impedance and high capacitive load. Many other internal features such as programmable open loop gain, programmable output current, internal band gap voltage reference, DC buffer and output DC offset circuitry give the device the flexibility for use in a wide range of applications.

### ORDERING INFORMATION

**SL9999C DP** (Commercial Plastic DIL 0° to 70°C)
**SL9999B DG** (Commercial Ceramic DIL -40° to +85°C)
**SL9999B LC** (Commercial LCC -40° to +85°C)
**SL9999NA IC** (Naked Chip)

### FEATURES

- Gain-Bandwidth Product 2GHz at 20dB
- Unity Gain-Bandwidth 400MHz
- Slew Rate 1300V/ µs Rising (typ)
- Slew Rate 630/V µs Falling (typ)
- ±50mA Output Current (Programmable)
- Non-saturating
- High Output Drive
- On-chip LF Buffer for Applying DC Offset
- Flexible Supply Range:
  $V_{CC}$ = +8V to +12V
  $V_{EE}$ = -4.5V to -5.5V
- Output Signal Handling ($V_{CC}$ = +12V, $V_{EE}$ = -5.2V)
  $V_{out}$ = 6V p-p (max.)
- Input Signal Handling ($V_{CC}$ = +12V, $V_{EE}$ = -5.2V)
  $V_{in}$ = +2.8V to -2.5V (max.)

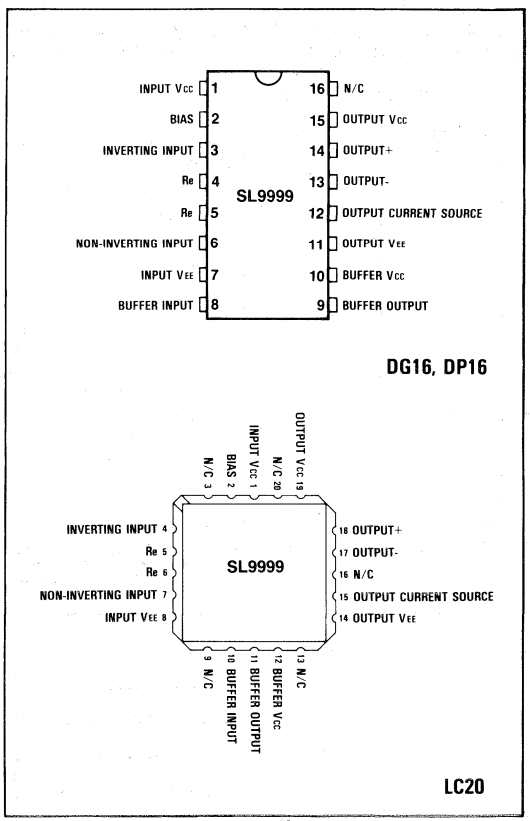



*Fig.1 Pin connections - top view*

### APPLICATIONS

- High Speed Flash ADC Driver
- Wideband, Buffer/Level Shifter
- Wideband IF Amplification
- Video Amplifier/Line Driver
- Fast Settling Pulse Amplifier
- High Speed Op-Amp Applications

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage ($V_{CC}$ to $V_{EE}$) | 20V |
| Input Voltage (Inv I/P to Non-Inv I/P) | ±5V |
| Storage Temperature | -65°C to +175°C |
| Chip Operating Temperature | +175°C |
| Operating Temperature: DIL | -40°C to +85°C |
| Thermal Resistances: | |
| DG Chip-to-Ambient: DIL | 120°C/W |
| DG Chip-to-Case: DIL | 40°C/W |
| DP Chip-to-Ambient: DIL | 100°C/W |
| DP Chip-to-Case: DIL | 40°C/W |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ 25° C, $V_{CC}$ +12V, $V_{EE}$ -5V, Test circuit Fig.3.

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Equivalent input noise | | 33 | | nV/√Hz | 50Ω source impedance, BW = 100MHz |
| Supply current (no load) | | 35 | 43 | mA | $V_{CC}$ = +12V, $V_{EE}$ = -5V |
| Gain-bandwidth product | | 2 | | GHz | ×10 gain |
| Unity gain bandwidth (small sig) | | 400 | | MHz | $R_e$ = 820Ω, $R_L$ = 50Ω |
| Slew rate RISING | 800 | 1300 | | V/μs | $R_L$ = 50Ω |
| Slew rate FALLING | 500 | 630 | | V/μs | $R_L$ = 50Ω |
| Settling time | | 24 | | ns | To 1% (×10 gain) |
| Open loop gain | | 65 | | dB | 50Ω load |
| Maximum $I_{out}$ | | | ±50 | mA | Programmable See Application Notes |
| Output bias current | 15 | 17 | 20 | mA | Pin 12 O/C |
| Supply line rejection | | 40 | | dB | Referred to input |
| Supply voltage $V_{EE}$ to $V_{CC}$ | 12.5 | | 18 | V | |
| Common mode rejection | 55 | | | dB | 50Ω load |
| Input offset (Note 1) | | ±5 | ±15 | mV | $R_e$ = 100Ω |
| Input bias current | | 4.5 | 18 | μA | |
| Buffer bandwidth | | 60 | | MHz | -3dB $R_L$ = 1kΩ (Pulldown resistor) |
| Buffer output current | | | 15 | mA | |

NOTE
Input offset is dependent on $R_e$. For lowest offset $R_e$ = 0 ohms.

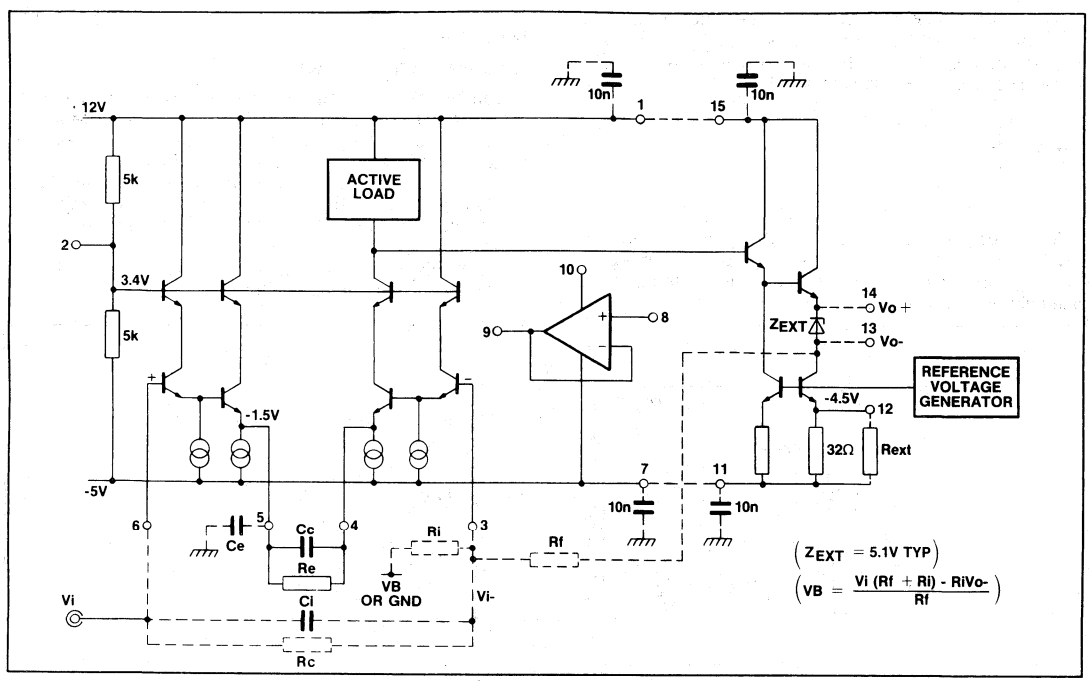



*Fig.2 Equivalent circuit with standard external components*

## APPLICATION NOTES

The SL9999 may be used as a high frequency amplifier in any of the usual op-amp configurations (amplifiers, integrators, etc.).

In most applications, the output of the SL9999 is taken from pin 13 ($V_{out-}$), DC level shifting can be obtained by applying feedback from pin 13 to pin 3 and taking the output from pin 14 ($V_{out+}$, see Fig.2). Alternatively, a DC offset can be applied through the low-drift on-chip buffer (pins 8 and 9) to $V_B$.

The Zener diode between pins 13 and 14 can also be divided into smaller value Zeners or resistors to give a range of DC levels at the output.

### Biasing Conditions (25° C)

For undistorted outputs the peak signal voltages on Vo +, Vo- and the inputs should comply with the following conditions:

A. $Vo+_{(MIN)} \geqslant \frac{V_{CC} + V_{EE}}{2} - 1.4V$

B. $Vo+_{(MAX)} \leqslant V_{CC} - 4.0V$

C. $Vo-_{(MIN)} \geqslant V_{EE} + 1.4V$

D. $Vi+ \text{ and } Vi- \leqslant \frac{V_{CC} + V_{EE}}{2} - 0.9V$

E. $Vi+ \text{ and } Vi- \geqslant V_{EE} + 3.2V$

Bias voltage values at several nodes are indicated on Fig.2.

$R_{ext}$ is connected from pin 12 to pin 11 ($V_{EE}$) to increase output bias current $I_{out}$. This current should not exceed 50mA. The value of $R_{ext}$ is calculated as follows:

$$R_{ext} \equiv \left[\frac{500}{I_{out} - 16}\right] \Omega$$

where $I_{out}$ is in mA.

The on-chip LF buffer has a small-signal bandwidth of 60MHz with 1kΩ load, and has an input/output signal handling capability of 8V. The output can deliver 15mA; an external pull-down resistor is required.

### High Frequency Stability

All component leads should be kept as short as possible, particularly at the summing junction. Also it is important to keep stray capacitance at the summing junction to an absolute minimum.

A ground plane should be used to minimise any earth induced currents between the input and output circuits.

The use of good power supply bypass capacitors (10nF Ceramic) will improve the overall performance. They should be close to the device supply pins. We also recommend electrolytic capacitors in parallel with Ceramic for supply decoupling.

Locate the signal source and load close to the circuit with proper termination - for 50Ω source use a 50Ω bead resistor. Other resistors should be carbon composition.

### Voltage Gain

Stable closed loop operation is ensured by changing the value of the degeneration resistor ($R_e$) between pins 4 and 5 according to the selected closed loop gain. As closed loop gain decreases the value of $R_e$ should be increased.

A graph of recommended $R_e$ with gain is given in Fig.4.

### Power Dissipation

A Zener diode is used between pins 13 and 14 to dissipate power externally and to provide DC offset of the output.

For -5V, ± 12V range a 4.7V to 5.1V Zener may be used.

For lower cost applications a bypassed resistor can conveniently replace the Zener diode. Its value may be calculated from the voltage drop and current through the output stage. For example, for 15mA output current a 330Ω resistor could be used.

Although some power is dissipated in the external Zener, a heatsink on the SL9999 will be necessary if power >800mW is to be dissipated.

### Bandwidth Compensation

Bandwidth at higher gains can be improved by a capacitor ($C_c$) across the degeneration resistor $R_e$. For example, a non-inverting closed loop gain of 10, 10pF will increase the bandwidth to 280MHz at 50Ω load condition.

A decoupling capacitor ($C_e$) from pin 5 will compensate the first pole roll-off and hence reduce the noise bandwidth. For a 200MHz bandwidth an 18pF capacitor may be used with the suggested PCB layout on page 6.

A capacitor ($C_i$) and resistor ($R_c$) of suitable value between the two inputs will reduce high frequency peaking.

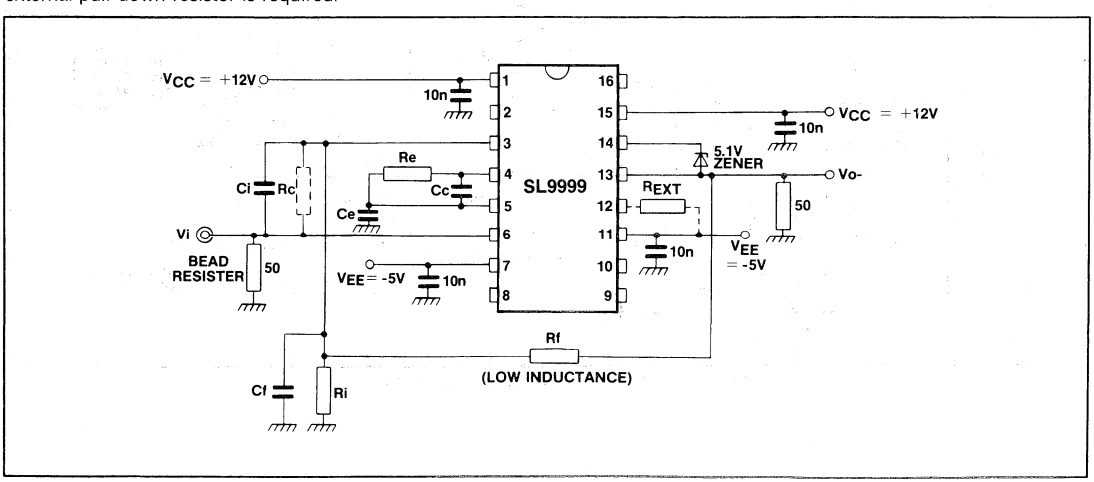



*Fig.3 Test/applications circuit for 50Ω load, 10nF ceramic decoupling capacitors*

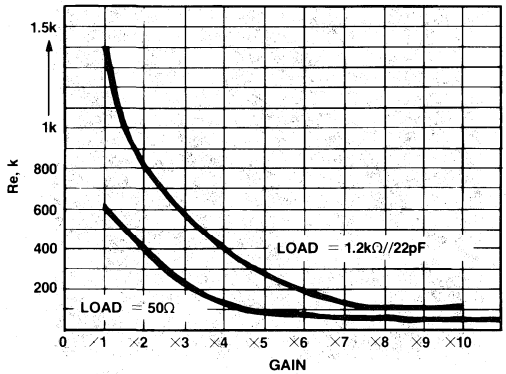



*Fig.4 Typical closed loop gain v. minimum value of degeneration resistor $R_e$*

*NOTE: Input offset is proportional to $R_e$ value*

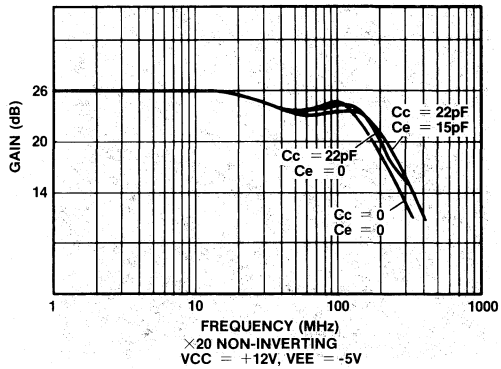



*Fig.5 Typical frequency response for the test circuit of Fig.3, ×20 gain, non-inverting, 50Ω load, $R_f$ = 10.6kΩ, $R_1$ = 560Ω, $R_e$ = 22Ω.*

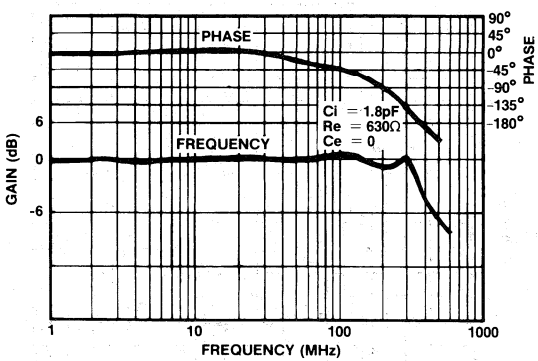



*Fig.6 Typical frequency/phase performance graphs for the circuit of Fig.3, ×1 gain, non-inverting, 50Ω load, $R_f$ = 560Ω, $R_1$ = ∞.*

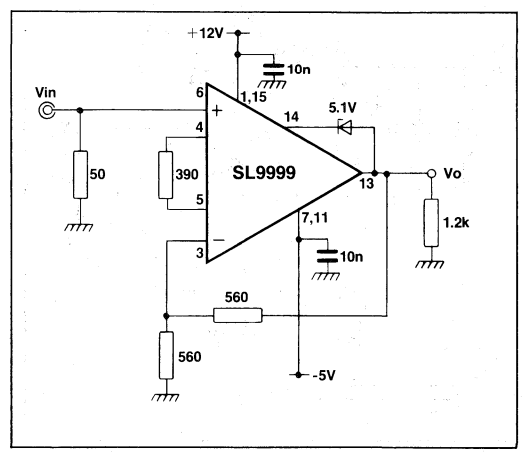



*Fig.7 Test circuit for large and small signal response, and slew rate (see Figs. 8 to 11). $V_{CC}$ = +12V, $V_{EE}$ = -5V.*

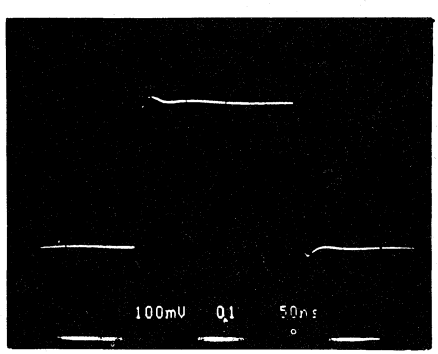



*Fig.8 Small signal response*

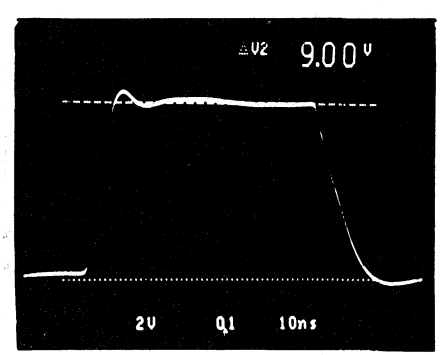



*Fig.9 Large signal response*

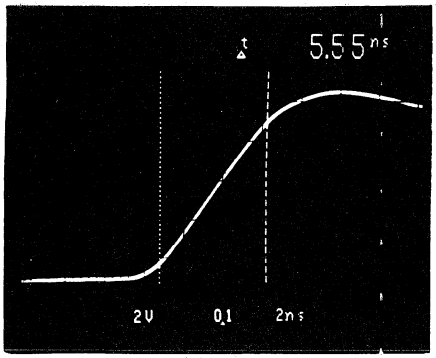



*Fig.10 Rising edge 10% to 90% points 1300V/μs*

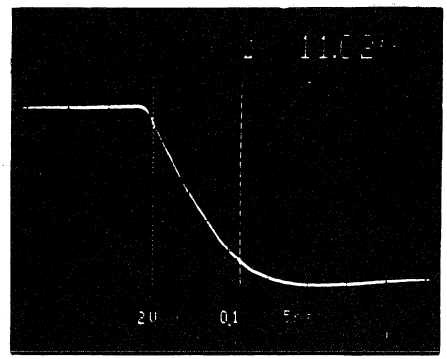



*Fig.11 Falling edge 10% to 90% points 630V/μs*

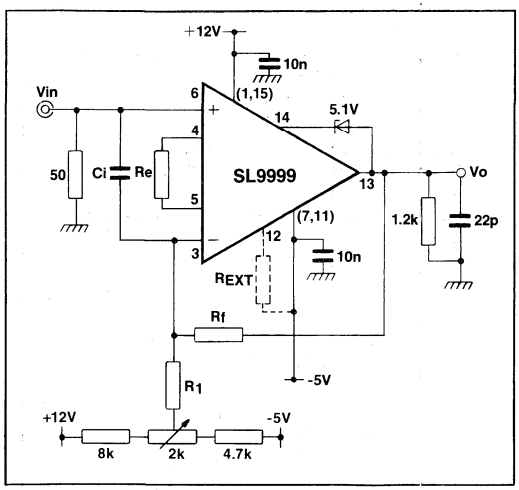



*Fig.12 Application circuit for capacitor load e.g. high speed flash ADC input*

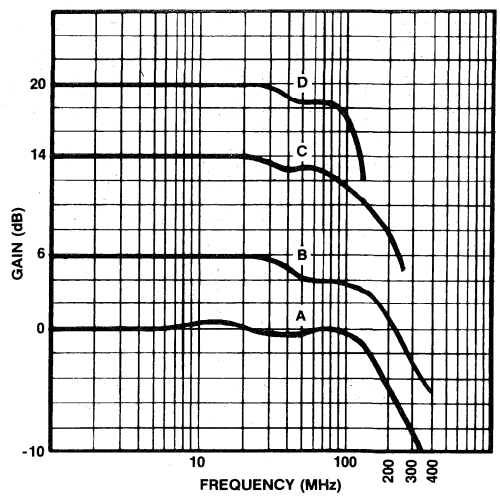



*Fig.13 Typical frequency response plots for the circuit of Fig.12 (Load 22pF//1.2kΩ).*

## TYPICAL APPLICATION

| Response (see Fig.13) | Gain | $R_f$ (Ω) | $R_I$ (Ω) | $R_e$ (Ω) | $C_f$ (Pf) | $R_{ext}$ (Ω) | VO/P (p-p) | $V_{CC}$ (V) | $V_{EE}$ (V) |
|---|---|---|---|---|---|---|---|---|---|
| A | ×1 | 2.2k | ∞ | 1.8k | 0 | ∞ | 1 | +12 | -5 |
| B | ×2 | 560 | 560 | 1.2k | 18 | 50 | 2 | +12 | -5 |
| C | ×5 | 2.2k | 560 | 270 | 10 | ∞ | 1 | +12 | -5 |
| D | ×10 | 5.6k | 560 | 68 | 0 | 10 | 1 | +12 | -5 |

*Table 1 Recommended components values for the test circuit of Fig.12*

NOTE
$C_f$ and $C_i$ are dependent on layout and used to compensate the effects of strays.

For applications that require accurate gain flatness over the full frequency range, the inverting mode of operation is recommended. See Fig.14.

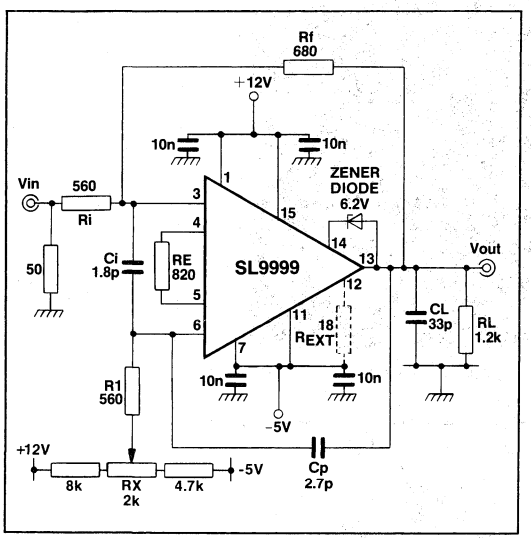



*Fig.15 Typical test/applications circuit for inverting mode. Load 33pF/1.2kΩ.*

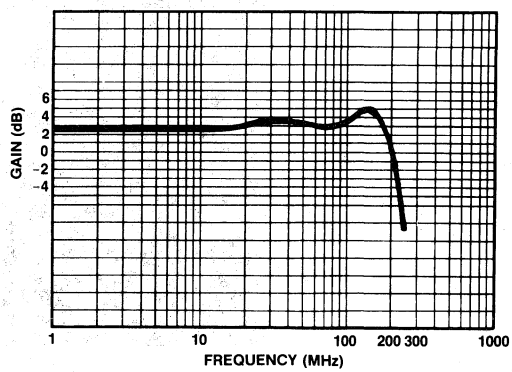
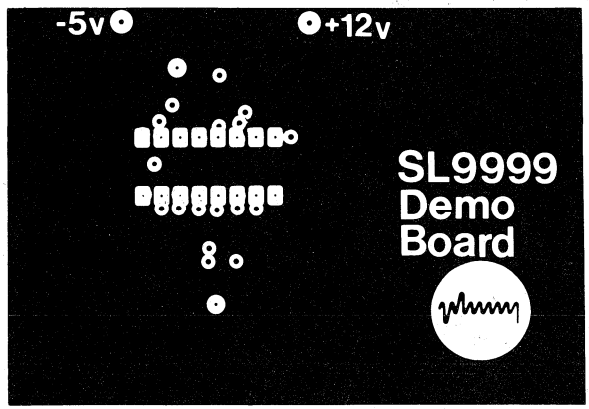
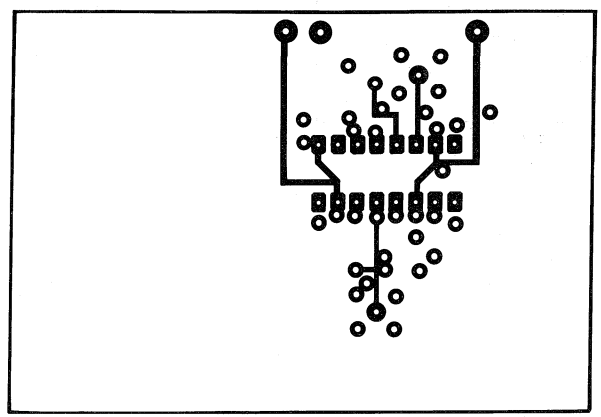



*Fig.16 Frequency response of SL9999 with $C_L$ = 33pF, $C_P$ = 2.7pF, $R_f$ = 680, $R_L$ = 1.2k, $C_i$ = 1.8pF, $R_1$ = 560, $V_O$ = 1V p-p (See Test Circuit of Fig.15)*

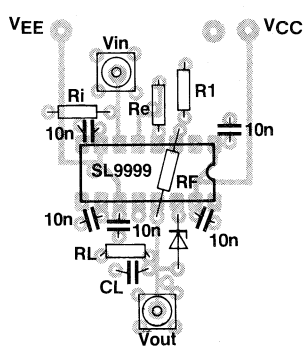
## CONSTRUCTION




*(a) SL9999 ground plane, component side*

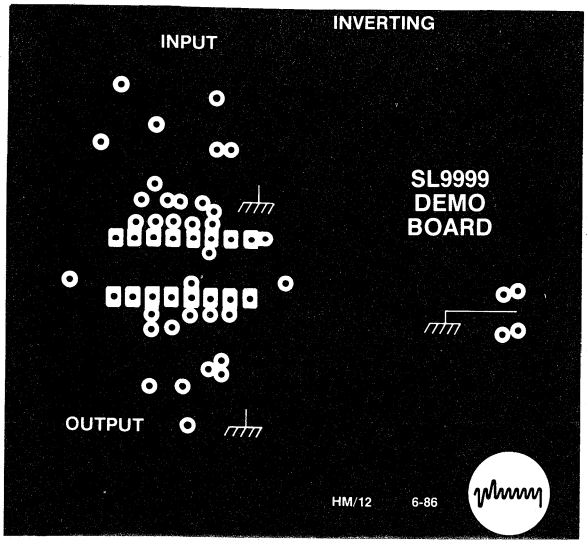


*(b) SL9999 board, track side*

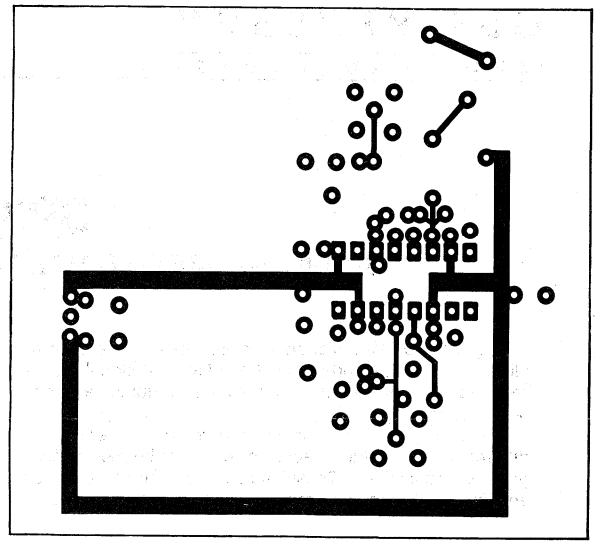



*(c) Component location. NOTE: I/P and O/P are sub-vis type 50Ω connectors.*

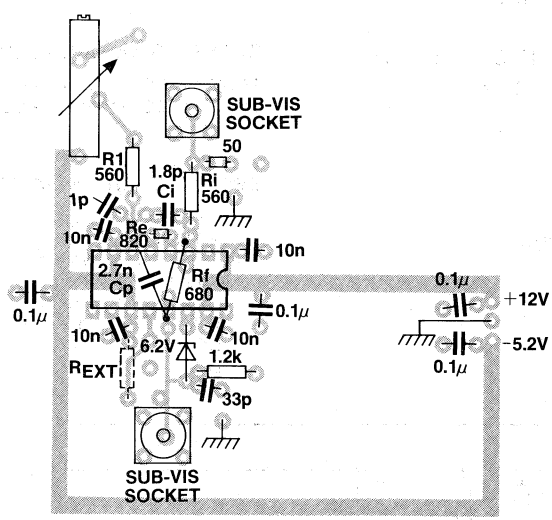
*Fig.16 PCB layout for SL9999 demonstration board (Fig.12) viewed from component side and underside*




(a) SL9999 ground plane, component side



(b) SL9999 board, track side




(c) Component location (1:1 scale)

*Fig.17 PCB layout for SL9999 demonstration board. NOTE: I/P and O/P are sub-vis type 50Ω connectors. Rf and C f are on the track side. Gold socket pins to mount SL9999 for test circuit*

# SP92701

## SUB-NANOSECOND ECL LINE RECEIVER AND DRIVER

The SP92701 is designed with an on-chip reference to allow either single ended or differential ECL signals to be received. The inverted and non-inverted outputs can drive 50Ω lines directly.

The use of a fixed current source in the tail of the differential input stage, enables the device to be used in more general applications. These include operational amplifier applications where low propagation delays are required.

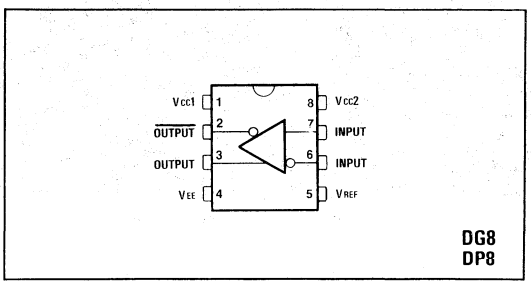



*Fig.1 Pin connections - top view*

### FEATURES

- ECL 10K Compatible
- Single or Differential Operation
- 50 Ohm Line Driving Capability
- Sub-nanosecond Performance
- ECL Reference Output
- Operating Temperature -40°C to +85°C (DG)
- Full Static Protection on All Pins

### APPLICATIONS

- Line Receiver
- Line Driver
- Clock Buffering/Distribution
- Op-amp Circuits
- Fanout Expansion
- Schmitt Trigger Circuits
- Fast Peak Detector

### ORDERING INFORMATION

**SP92701C DP** (Industrial - Plastic DIL package)
**SP92701B DG** (Industrial - Ceramic DIL package)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage $V_{CC}$-$V_{EE}$ | 8V |
| Input voltage | 0V to $V_{EE}$ |
| Differential input voltage | 3.3V |
| Output source current | 50mA |
| Storage temperature range | -55°C to 150°C |
| Junction operating temperature | |
| DG | 175°C |
| DP | 150°C |

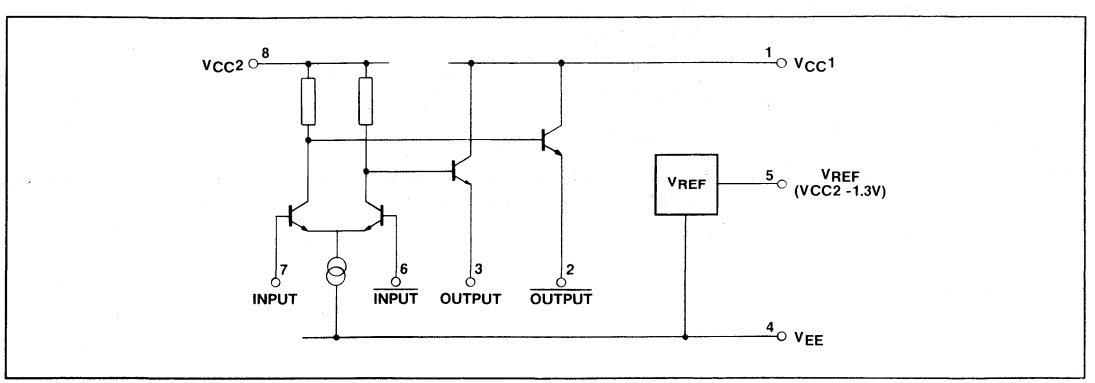



*Fig.2 Internal diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = −40 °C to +85 °C (DG package), 0 °C to +70 °C (DP package); $V_{EE}$ = −5.2V ± 0.25V

### DC Characteristics

| Characteristic | Symbol | Value | | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | −40 °c (DG) | | 25 °C (DP & DG) | | 85 °C (DG) | | | |
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| Power supply current | $I_{EE}$ | | 12 | | 12 | | 12 | mA | No load |
| Input current high | $I_{INH}$ | | | | 350 | | | μA | Inputs ECL high |
| Input leakage current | $I_{cbo}$ | | 50 | | 40 | | 40 | μA | Inputs ECL low |
| Reference voltage | $V_{REF}$ | −1.43 | −1.29 | −1.35 | −1.23 | −1.29 | −1.15 | V | |
| High output voltage | $V_{OH}$ | −1.06 | −0.86 | −0.96 | −0.81 | −0.89 | −0.70 | V | Load = 50Ω to −2V |
| Low output voltage | $V_{OL}$ | −1.90 | −1.66 | −1.85 | −1.62 | −1.83 | −1.57 | V | Load = 50Ω to −2V |
| High input voltage | $V_{IH}$ | −1.19 | −0.88 | −1.09 | −0.81 | −1.03 | −0.7 | V | |
| Low input voltage | $V_{IL}$ | −1.90 | −1.53 | −1.85 | −1.48 | −1.83 | −1.44 | V | |

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Common mode range | $V_{cmr}$ | | −2.85 to−0.8 | | V | At 25 °C |
| Input sensitivity (differential) | $V_{pp}$ | | 150 | | mV | At 25 °C |
| Differential gain | | | 25 | | dB | At 25 °C |

### AC Characteristics

$T_{amb}$ = 25 °C

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Propagation delay | $t_{pd}$ | | 0.8 | 0.96 | ns | |
| Transition time, 20 % to 80 % | $t_r$, $t_f$ | | 0.8 | 0.95 | ns | |

NOTE Guaranteed but not tested.

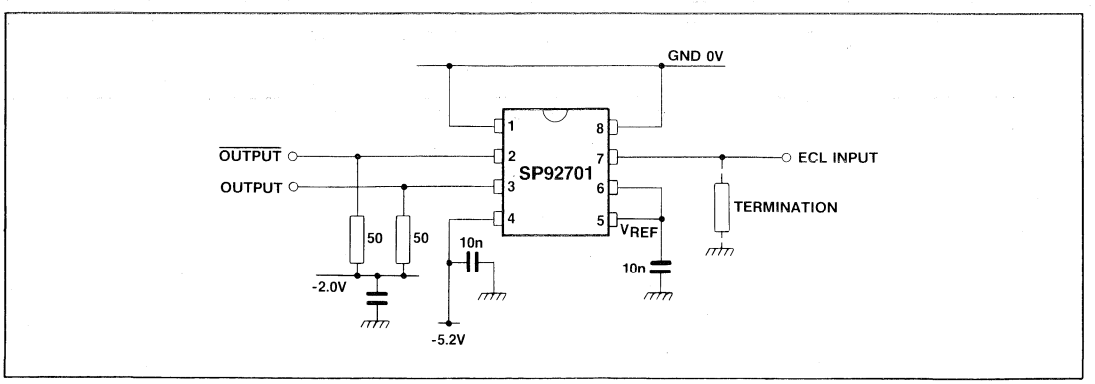



*Fig.3 Test/applications circuit*

## OPERATING NOTES

The SP92701 has been designed primarily for enhancing the edges of ECL signals.

With most systems using ECL it is necessary to minimise the amount of edge jitter on clock signals etc. By reducing the rise times of the ECL edges it is possible to reduce the amount of voltage noise to time jitter conversion that occurs with slower edge.

The SP92701 can also be used to expand fanout and provide conversion from single ended to differential or differential to single ended ECL.

A current source located in the tail of the differential pair (Fig.2) gives the SP92701 a wide common mode range. This enables it to be used in other applications such as comparators or low cost wideband amplifiers.

Used as a line receiver in single ended non-inverting mode, the typical maximum frequency of operation is 700MHz.

### Outputs

The outputs of the SP92701 are open emitter and hence require an external pulldown resistor for evaluation or test. It can also be useful to apply $V_{CC} = +2V$ and $V_{EE} = -3.2V$ for direct drive of 50Ω instruments.

### Schmitt Trigger

Positive feedback can be applied from the output for applications that require input hysteresis.

### Board Layout

Care should be taken with component placement. Use a solid ground plane under the device. Tracks should be short or terminated with their characteristic impedance. The supply pins should be decoupled to ground with good high frequency decoupling capacitors, located close to the device pins.

## ANALOG APPLICATION (Fig.4)

SP92701, SL560 combination. Forming a low noise, low cost 30dB amplifier and differential line driver (100Ω twisted pair). Response is flat to 350MHz ± 1dB.

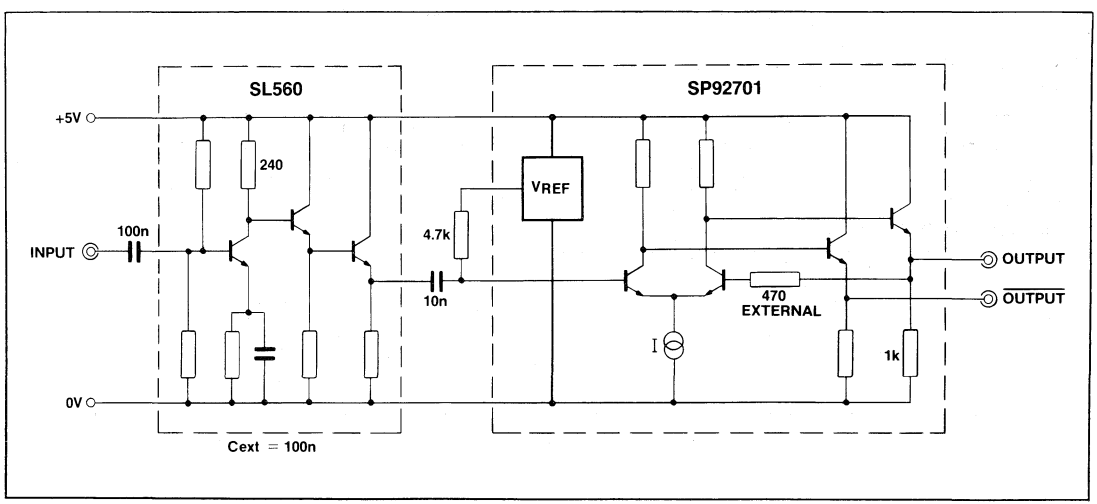



*Fig.4 Low noise amp and driver*

# SP93802

## SUB-NANOSECOND DUAL COMPARATOR

The SP93802 contains two independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The gain of this comparator has been optimised for low propagation delay and high stability, therefore hysteresis is rarely required.

Each comparator includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. As each comparator is separately clocked, the device can be used as a matched pair.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

### FEATURES

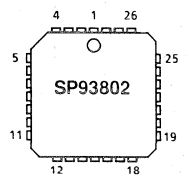
- -40°C to +85°C Temperature Range
- Typical Delay < 1ns
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 2 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching < 100ps
- High Input Impedance
- Quad and Octal Versions SP93804/SP93808

### APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers

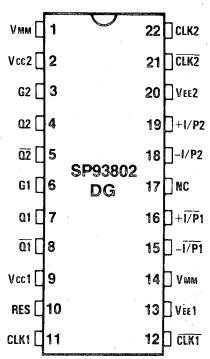
### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC} - V_{MM}$ | +6V |
| Supply voltage $V_{MM} - V_{EE}$ | -6V |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -55°C to +125°C |
| Output current | ≤30mA |
| Maximum input voltage | |
| Common mode positive | ≤$V_{CC}$ |
| Common mode negative | ≥$V_{EE}$ |
| Differential input voltage | ≤±3.8V |




HG28

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 1 | $V_{MM}$ | 8 | NC | 15 | CLK1 | 22 | NC |
| 2 | $V_{CC}2$ | 9 | G1 | 16 | $\overline{CLK1}$ | 23 | -I/P2 |
| 3 | O/P $V_{CC}2$ | 10 | Q1 | 17 | $V_{EE}1$ | 24 | +I/P2 |
| 4 | NC | 11 | $\overline{Q1}$ | 18 | $V_{MM}$ | 25 | NC |
| 5 | G2 | 12 | O/P $V_{CC}1$ | 19 | NC | 26 | $V_{EE}2$ |
| 6 | Q2 | 13 | $V_{CC}1$ | 20 | -I/P1 | 27 | $\overline{CLK2}$ |
| 7 | $\overline{Q2}$ | 14 | RESET | 21 | +I/P1 | 28 | CLK2 |




DG22

*Fig.1 Pin connections - top view*

### ORDERING INFORMATION

**SP93802 B HG** (Industrial - Quad Cerpac (J-Form) package)
**SP93802 B DG** (Industrial - Ceramic DIL package)

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = -40 °C to +85 °C, I/P and O/P $V_{CC}$ = +5V ± 0.25V,
$V_{EE}$ = -5V ± 0.25V, $V_{MM}$ = 0V (see Fig.4), Load = 50Ω to $V_{CC}$ - 2V

**Static Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply current | $I_{CC}$ | | 38.5 | 50 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5V<br>No load. Each comparator. |
| Negative supply current | $I_{EE}$ | | 16.0 | 21 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5V<br>No load. Each comparator. |
| Positive supply voltage | $V_{CC}$ | I/P MAX<br>+1.55 | 5.0 | I/P MIN<br>+7.3 | V | |
| Negative supply voltage | $V_{EE}$ | -5.5 | -5.0 | -4.9 | V | |
| Input offset voltage | $V_{OS}$ | -3.5 | | +3.5 | mV | |
| Input bias current | $I_B$ | | 5.25 | 9 | μA | |
| Input offset current | $I_{OS}$ | | 0.95 | 1.2 | μA | |
| Input capacitance | $C_I$ | | 1.5<br>(Note 1) | | pF | HG package |
| Input impedance | $R_I$ | | 250 | | kΩ | Measured at DC |
| Differential input range | $V_{DIF}$ | | | ±3.8 | V | |
| Common mode input range | CMIR | -2.1 | | +2.6 | V | |
| Output voltage high | $V_{OH}$ | $V_{CC}$-1.050 | | $V_{CC}$-0.81 | V | +25 °C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-1.140 | | $V_{CC}$-0.91 | V | -40 °C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-0.965 | | $V_{CC}$-0.704 | V | +85 °C, $V_{IN}$ > 60mV |
| Output voltage low | $V_{OL}$ | $V_{CC}$-1.712 | | $V_{CC}$-1.544 | V | +25 °C, $V_{IN}$ < -60mV |
| | | $V_{CC}$-1.792 | | $V_{CC}$-1.650 | V | -40 °C, $V_{IN}$ < -60mV |
| | | $V_{CC}$-1.638 | | $V_{CC}$-1.465 | V | +85 °C, $V_{IN}$ < -60mV |
| Gain (transparent mode) | | | 20 | | dB | Differential |
| Common mode rejection | CMRR | | 50 | | dB | +25 °C, with respect to I/P |
| Supply voltage rejection | PSRR | | 70 | | dB | +25 °C, with respect to I/P offset |
| Clock input: | | | | | | |
| Common mode range | CMRC | $V_{MM}$+2V | | $V_{CC}$-1.35V | V | |
| Differential swing | DS | 400 | | 1600 | mV | |

NOTES 1 Guaranteed but not tested.

**Dynamic Characteristics (Note 1)** See dynamic test circuit Fig.9.

| Characteristic | Symbol | Value | | | Units | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Latch setup time | $t_S$ | | 150 | | ps | 20mV overdrive |
| Hold time | $t_H$ | | 600 | | ps | 20mV overdrive |
| Input to Q delay | $t_{IQ}$ | | 800 | | ps | 20mV overdrive |
| Latch to Q delay | $t_{LQ}$ | | 1500 | | ps | 20mV overdrive |
| Glitch capture regeneration | $t_{RD}$ | | 900 | | ps | 20mV overdrive at Qn |
| Propagation delay matching | $t_{PDM}$ | -100 | | +100 | ps | Within each device |
| Min. compare pulse width | $t_{PW}$ | | 950 | | ps | 20mV overdrive |
| Min. reset pulse width | $t_{RM}$ | | 800 | | ps | |
| Max. flip flop reset time | $t_{RR}$ | | 800 | | ps | |
| Min. hold time of Qn after reset | $t_{GH}$ | | 800 | | ps | |
| Delay between Qn and Gn | $t_{QG}$ | | 900 | | ps | |
| Propagation delay RES to Gn | $t_{RG}$ | | 800 | | ps | |

NOTES 1. Guaranteed but not tested.

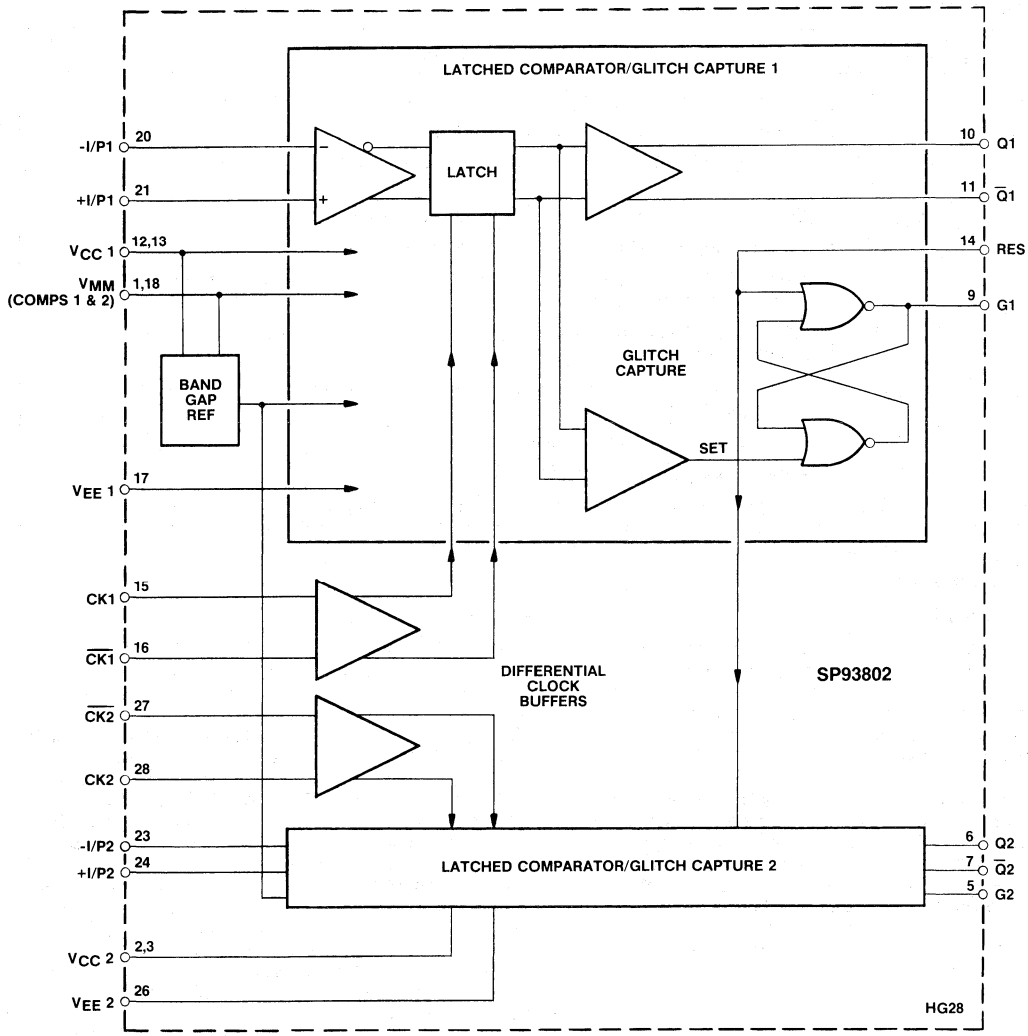



*Fig.2 Internal block diagram, with pins shown for HG28 package (comparator 2 as detailed for comparator 1)*

## PIN FUNCTIONS

| Name | HG28 Pin | Description |
|---|---|---|
| $V_{CC}1$ | 13,12 | Positive supply connection for comparator 1 and the bandgap reference. |
| $V_{CC}2$ | 2,3 | Positive supply connection for comparator 2. |
| -I/Pn<br>+I/Pn | 20/23, 21/24 | Inverting and non-inverting inputs to comparators 1 and 2, respectively. |
| Qn/$\overline{Q}$n | 10/11, 6/7 | Q and $\overline{Q}$ outputs of comparators 1 and 2, respectively. |
| Gn | 9,5 | Outputs of glitch capture circuits 1 and 2, respectively. |
| RESET | 14 | Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (Gn) of the Glitch capture circuits to '0'. |
| CLK1, $\overline{CLK}$1 | 15/16 | Clock input pins for comparator 1. Active low signal which latches the outputs of comparator 1. |
| CLK2, $\overline{CLK}$2 | 28/27 | Clock input pins for comparator 2. Active low signal which latches the outputs of comparator 2. |
| $V_{EE}1$ | 17 | Negative supply voltage for comparator 1. |
| $V_{EE}2$ | 26 | Negative supply voltage for comparator 2. |
| $V_{MM}$ | 1,18 | Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref. |

## OPERATING NOTES

### Transparent Mode

The SP93802 has been designed to maximise high input impedance and minimise propagation delay.

While CLK is high ($\overline{CLK}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 20dB. In this mode, for example, a 20mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93802 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

### Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{CLK}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

### Supply Connections

The SP93802 operates from supply voltages of 0V, -5V and -10V (Fig.3) or ±5V (Fig.4). The choice of supply connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from $V_{CC}$, then to interface with other ECL circuits directly, supplies of 0V, -5V, -10V should be provided. This will give an input common mode range of -2.4V to -7.0V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage ($V_{MM}$), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5V supply is not available.

The SP93802 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5V rails.

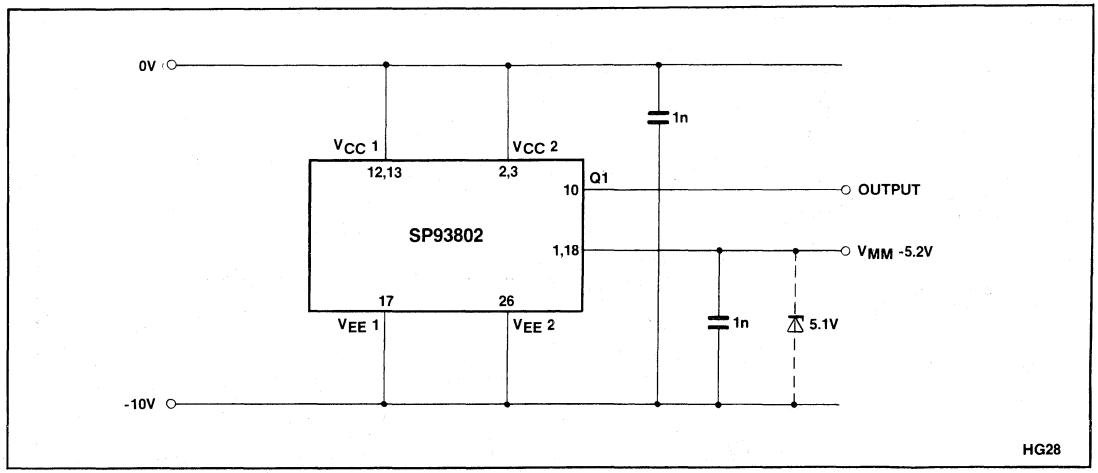



*Fig.3 Connection to 0V, -5.2V and -10V*

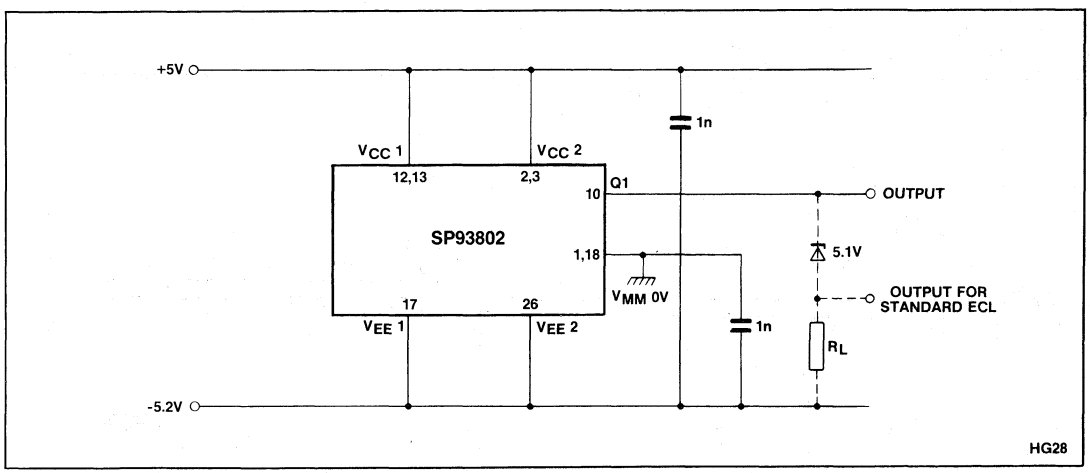



*Fig.4 Connection to ±5V*

## External Components

The Qn, $\overline{Qn}$ and Gn outputs are open emitters and therefore required external pulldown resistors ($R_L$). These resistors may be in the range of 50-250Ω connected to $V_{CC}$-2V ($V_T$) or 250-2000Ω connected to $V_{MM}$.

Due to the sub-ns conversion speeds and edge speeds of this device, the performance is dependent on both board layout and component placement.

The performance of the comparator is enhanced by minimising the number of external components and minimising the external strays around the device. The use of high quality chip resistors is recommended, especially for loads.

Decoupling capacitors should be positioned close to the device supply pins. Decoupling between supplies and $V_{EE}$ is also recommended.

The device has been packaged for maximum isolation between channels. This has been achieved by positioning an un-bonded (not internally connected) pin between each set of comparator inputs. These N/C pins can be connected to the ground plane, providing further isolation.

## Clock Inputs

The SP93802 can be used in transparent mode by connecting the CLK input to ECL '1' and the $\overline{CLK}$ input to an ECL '0'. The device can also be used as two single comparators as both comparators can be clocked separately.

As the device contains two clock input buffers, a range of clock input configurations are possible.

Optimum performance in terms of crosstalk will be acheived with a differential input of 400mV p-p.

$\overline{CLK1}$ (pin 15) comparator 1 latched when low.
$\overline{CLK1}$ (pin 16) inverse clock for comparator 1.
$\overline{CLK2}$ (pin 28) comparator 2 latched when low.
$\overline{CLK2}$ (pin 27) inverse clock for comparator 2.

The clock inputs should have fast rise times and low jitter. The Plessey SP92701 line receiver can be used to clean up the clock signal and provide a good differential ECL drive for this comparator.

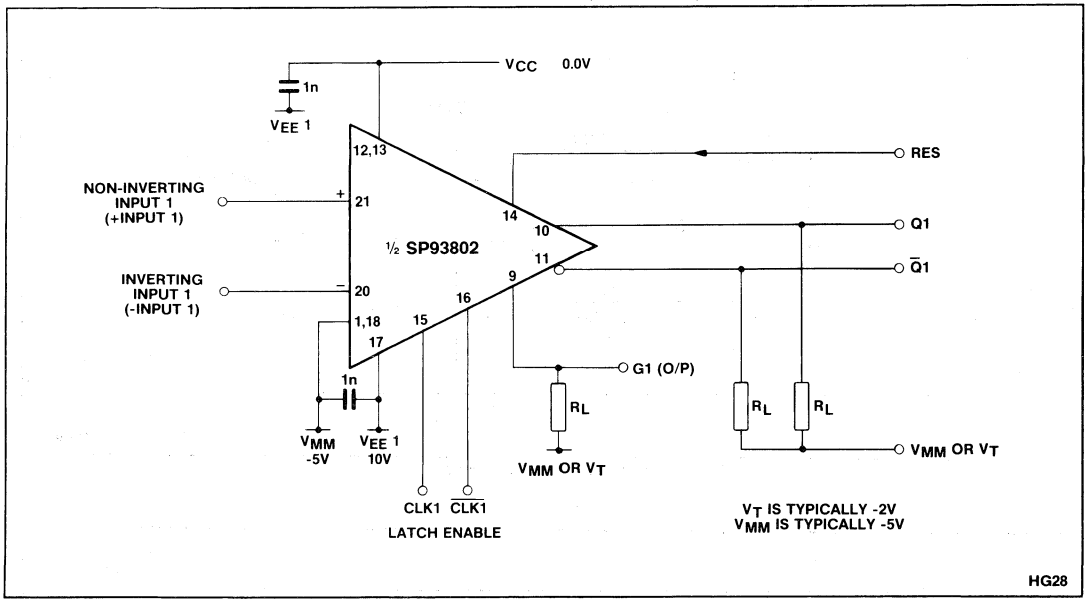



*Fig.5 Applications circuit (one channel)*

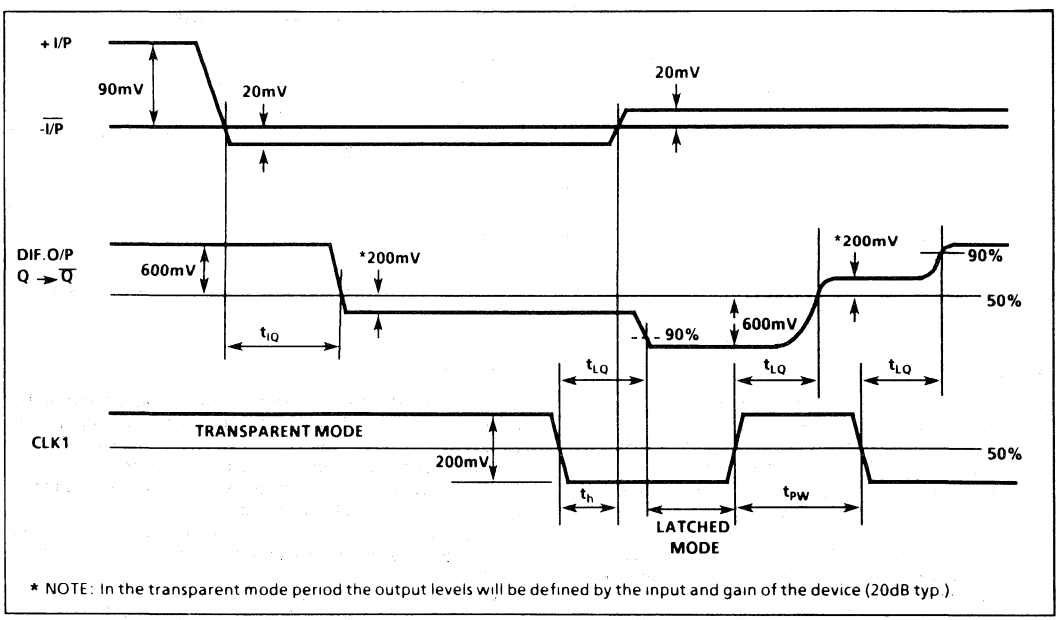



*Fig.6 Comparator timing diagram*

| I/P | CLK | Qn + 1 |
|---|---|---|
| X | 0 | Qn |
| 1 | 1 | 1 |
| 0 | 1 | 0 |

X = Don't Care

*Table 1 Truth table for comparator*

| RES | SET(1) (n + 1) | Gn + 1 |
|---|---|---|
| 1 | X | 0 |
| 0 | ↗ | ↗ |
| 0 | ↘ | 1 |
| 0 | 1 | 1 |
| 0 | 0 | Gn(2) |
| ↘ | 1 | ↗ |
| ↘ | 0 | 0 |

X = Don't Care

*Table 2 Truth table for glitch capture circuit*

## Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' ($V_{CC}$ - 0.8V) the RES pin will reset the Gn output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Qn goes positive by more than 20mV for a time $>t_{RD}$ then the Gn output will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

NOTES
1. SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.8.
2. Gn = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

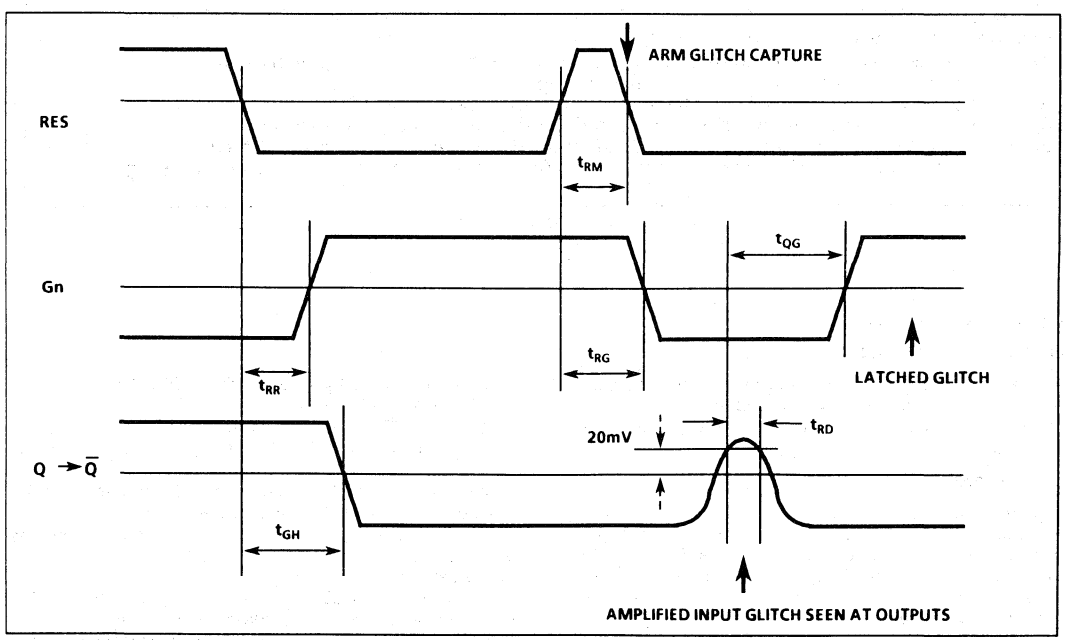
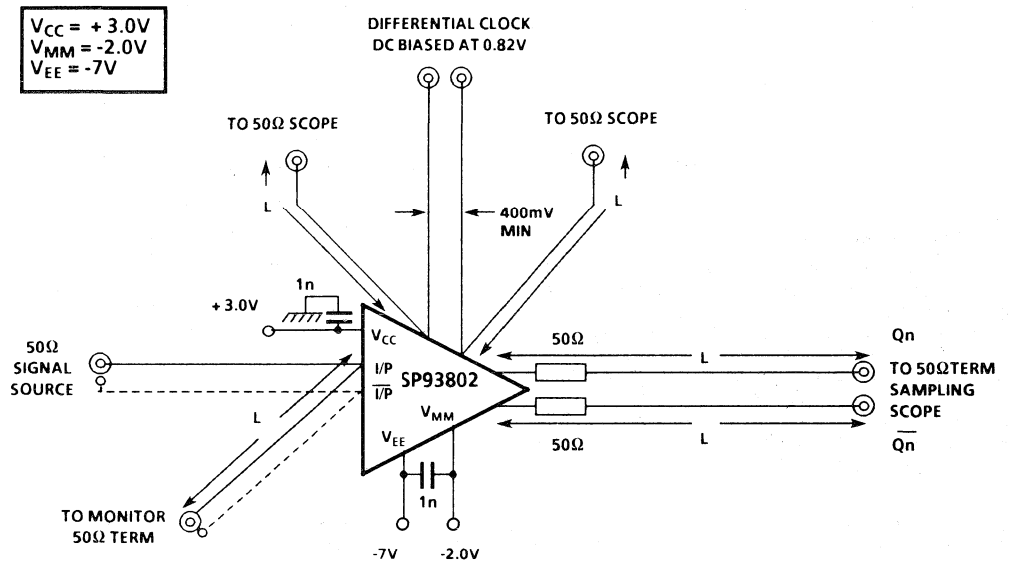



*Fig.7 Glitch capture circuit timing*




NOTES:-

The supplies have been chosen to allow direct connection of both the outputs and monitor points to measurement instruments with 50Ω input impedance.

1) Lead lengths should be as short as possible and also of equal length. (equal delay).
2) Decoupling should be close to the device (chip type if possible).
3) Use coaxial cables or stripline techniques in board construction.
4) Monitor and both scope channel 50Ω loads must be in circuit for correct termination.
5) A Plessey SP92701 can be used with supplies of +3V and -2V, to drive the clock input. The outputs of the SP92701 should have series 100Ω resistors to reduce the differential swing.

*Fig.8 Comparator dynamic test circuit (one channel)*

## APPLICATION NOTES

### High Gain Applications

Increased gain can be obtained on one channel by tying the Qn output to the Reset input. A Q phase ECL signal is then obtained from the Gn output. Approximately 40dB gain is achieved.

### Trigger Circuits

A narrow trigger pulse can be obtained directly from one of the two comparators. This is achieved by tying the Qn signal to the Reset input. The trigger pulse is obtained from the Gn output and is approximately 1ns wide, positive going and occurs synchronously with the rising edge of the conventional Q signal.

### Construction of Evaluation Board (DG22 Package)

This application board demonstrates the capability of the SP93802 functioning at 500MHz and produces edge speeds of less than one nanosecond.

In the application circuit (Fig.9) for the SP93802 both of the channels are driven together and clocked differentially.

$V_{MM}$ is generated by a Zener diode (5.1V) from the $V_{CC}$ (+3V) and $V_{EE}$ (-7V).

CLK, $\overline{CLK}$, RES inputs are biased for 50Ω termination.

Inverting inputs (18,15) and unused pin (17) should be tied to ground.

Input pins (16,19) are terminated by 50Ω monitor or scope channel to provide the correct terminations.

Outputs Q, $\overline{Q}$ (8,5,7,4) and glitch capture outputs G1,G2(6,3) are terminated through 50Ω series resistors to 50Ω wideband scope channel.

CLK, $\overline{CLK}$ and RESET signals can be generated from the input signal through a divide-by-two (Plessey SP9131, 520MHz ECL dual D-type flip-flop used in cascade to form a divide-by-2 and 4), so no external synchronisation is then needed. The latched outputs can be seen on the scope at 1/2 the normal ECL levels. Alternatively the CLK, $\overline{CLK}$, RESET signals from any other sources can be used phase locked to the input. The SP92701 is useful for driving the CLK lines.

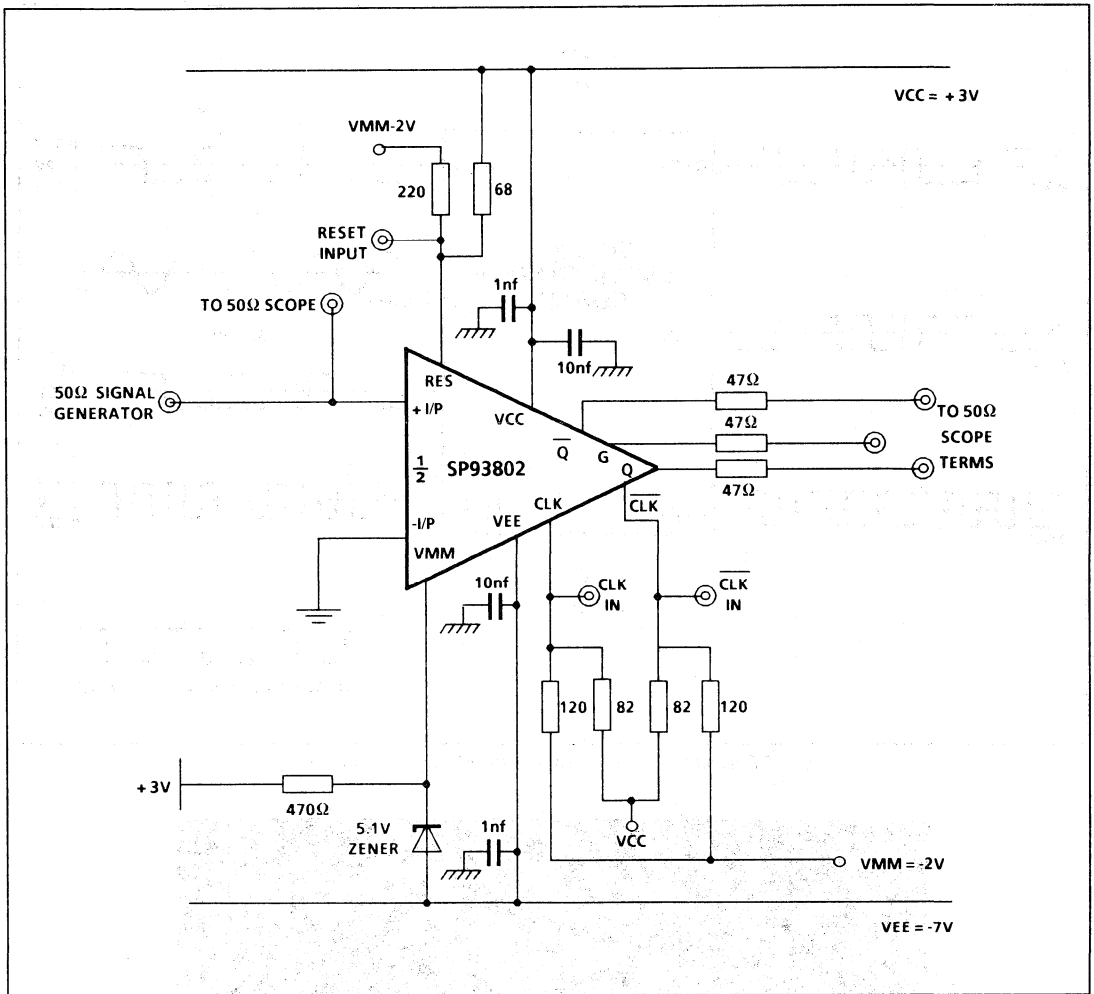



*Fig.9 SP93802 application board diagram for one channel*

| Function | $V_{MM}$ | NC | $V_{EE}$ | CLK | $\overline{CLK}$ | Q |
|---|---|---|---|---|---|---|
| Pin/DG22 | 1,14 | 17 | 13,20 | 11,22 | 12,21 | 4,7 |

| Function | $\overline{Q}$ | G | $V_{CC}$ | RES | +I/P | -I/P |
|---|---|---|---|---|---|---|
| Pin/DG22 | 5,8 | 3,6 | 2,9 | 10 | 16,19 | 15,18 |

*Table 3 SP93802 pin connections (DG22)*

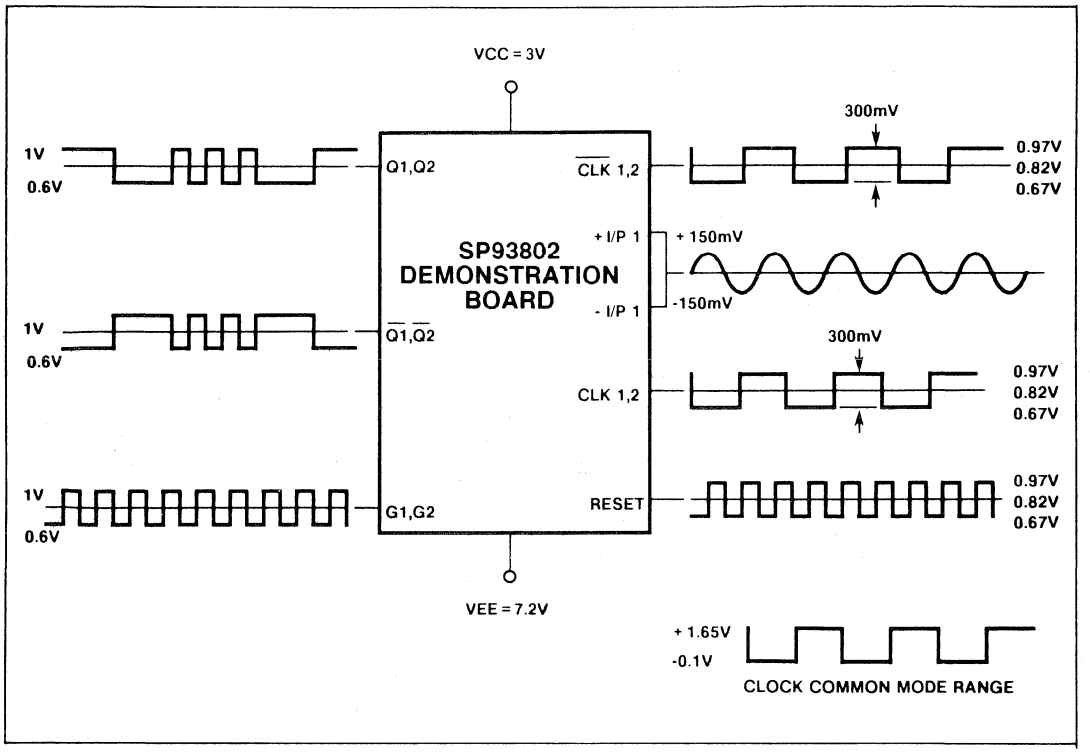
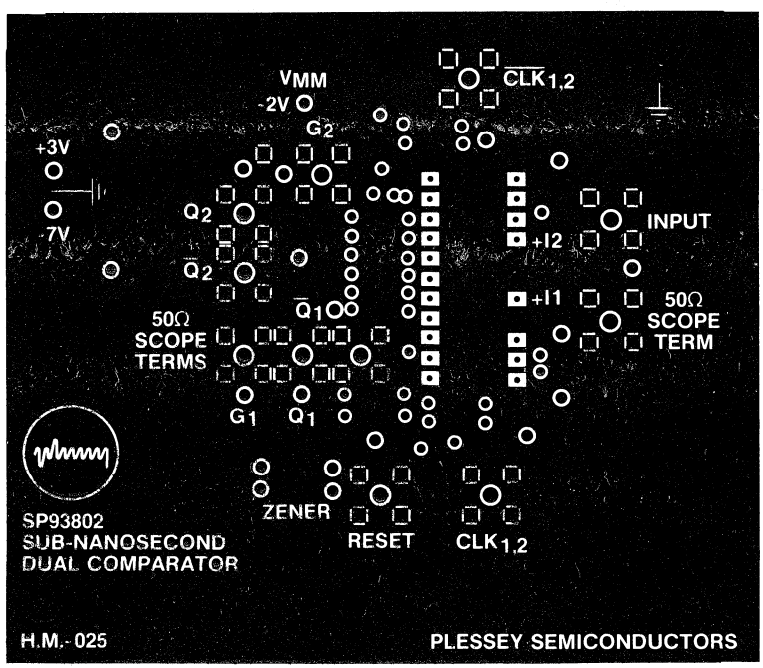
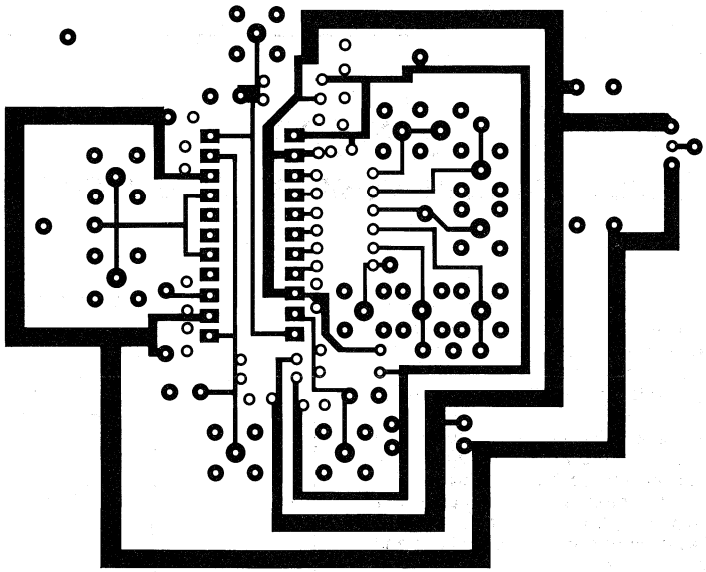


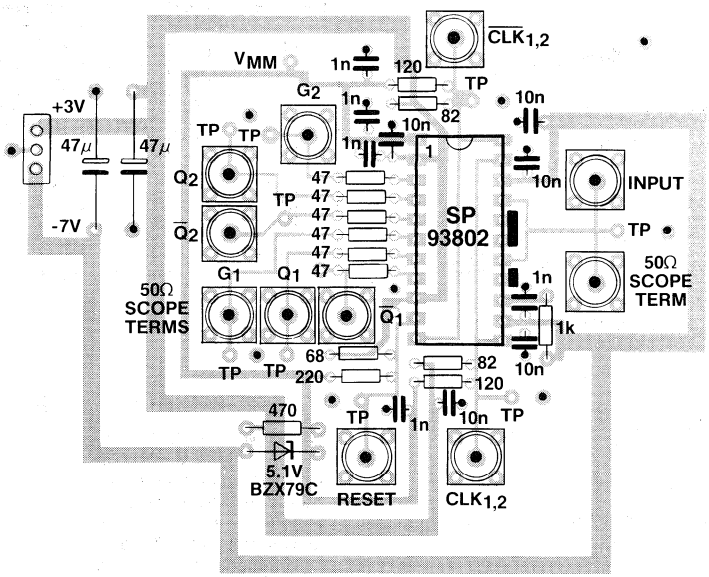

*Fig.10 Bias and timing diagram for SP93802 application board*




*(a) SP93802 ground plane*



*(b) SP93802 evaluation board, track side*




*(c) SP93802 evaluation board, component layout*

*Fig.11 PCB layout for SP93802 demonstration board (circuit of Fig.9). Scale 1:1*

# SP93804

## SUB-NANOSECOND QUAD COMPARATOR/GLITCH DETECTOR

The SP93804 contains four independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The gain of this comparator has been optimised for low propagation delay and high stability, therefore hysteresis is rarely required.

Each channel includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. The SP93804 can also be used as two matched dual devices, due to comparators 1 and 2 being clocked separately from comparators 3 and 4.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

### ORDERING INFORMATION

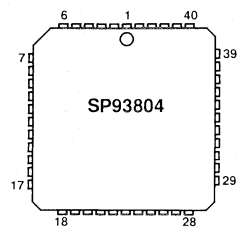
**SP93804 B HG** (Industrial Quad Cerpac (J-Form) package)

### FEATURES

- -40°C to +85°C Temperature Range
- Typical Delay <1ns
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 4 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching <100ps
- High Input Impedance
- Dual and Octal Versions SP93802/SP93808

### APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers




HG44

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 1 | I/P $V_{CC2}$ | 12 | NC | 23 | $V_{MM}$ | 34 | NC |
| 2 | O/P $V_{CC2}$ | 13 | G2 | 24 | RES | 35 | -I/P3 |
| 3 | G4 | 14 | $\overline{NC}$ | 25 | CLK1 | 36 | +I/P3 |
| 4 | $\overline{NC}$ | 15 | $\overline{Q2}$ | 26 | $\overline{CLK1}$ | 37 | NC |
| 5 | $\overline{Q4}$ | 16 | Q2 | 27 | $V_{EE1}$ | 38 | -I/P4 |
| 6 | Q4 | 17 | NC | 28 | $V_{MM}$ | 39 | +I/P4 |
| 7 | NC | 18 | $\overline{G1}$ | 29 | -I/P1 | 40 | NC |
| 8 | G3 | 19 | $\overline{Q1}$ | 30 | +I/P1 | 41 | $V_{EE2}$ |
| 9 | $\overline{NC}$ | 20 | Q1 | 31 | NC | 42 | $\overline{CLK2}$ |
| 10 | $\overline{Q3}$ | 21 | O/P $V_{CC1}$ | 32 | -I/P2 | 43 | CLK2 |
| 11 | Q3 | 22 | I/P $V_{CC1}$ | 33 | +I/P2 | 44 | $V_{MM}$ |

*Fig.1 Pin connections - top view*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC} - V_{MM}$ | +6V |
| Supply voltage $V_{MM} - V_{EE}$ | -6V |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -55°C to +125°C |
| Output current | ≤30mA |
| Maximum input voltage | |
| Common mode positive | ≤$V_{CC}$ |
| Common mode negative | ≥$V_{EE}$ |
| Differential input voltage | ≤±3.8V |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = -40°C to +85°C, I/P and O/P $V_{CC}$ = +5V ± 0.25V,
$V_{EE}$ = -5V ± 0.25V, $V_{MM}$ = 0V (see Fig.4), Load = 50Ω to $V_{CC}$-2V

**Static Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply current | $I_{CC}$ | | 38.5 | 50 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5V No load. Each comparator. |
| Negative supply current | $I_{EE}$ | | 16.0 | 21 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5V No load. Each comparator. |
| Positive supply voltage | $V_{CC}$ | I/P MAX +1.55 | 5.0 | I/P MIN +7.3 | V | |
| Negative supply voltage | $V_{EE}$ | -5.5 | -5.0 | -4.9 | V | |
| Input offset voltage | $V_{OS}$ | -3.5 | | +3.5 | mV | |
| Input bias current | $I_B$ | | 5.25 | 9 | μA | |
| Input offset current | $I_{OS}$ | | 0.95 | 1.2 | μA | |
| Input capacitance | $C_I$ | | 1.5 (Note 1) | | pF | |
| Input impedance | $R_I$ | | 250 | | kΩ | Measured at DC |
| Differential input range | $V_{DIF}$ | | | ±3.8 | V | |
| Common mode input range | CMIR | -2.1 | | +2.6 | V | |
| Output voltage high | $V_{OH}$ | $V_{CC}$-1.050 | | $V_{CC}$-0.81 | V | +25°C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-1.140 | | $V_{CC}$-0.91 | V | -40°C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-0.965 | | $V_{CC}$-0.704 | V | +85°C, $V_{IN}$ > 60mV |
| Output voltage low | $V_{OL}$ | $V_{CC}$-1.712 | | $V_{CC}$-1.544 | V | +25°C, $V_{IN}$ < -60mV |
| | | $V_{CC}$-1.792 | | $V_{CC}$-1.650 | V | -40°C, $V_{IN}$ < -60mV |
| | | $V_{CC}$-1.638 | | $V_{CC}$-1.465 | V | +85°C, $V_{IN}$ < -60mV |
| Gain (transparent mode) | | | 20 | | dB | Differential |
| Common mode rejection | CMRR | 50 | 50 | | dB | +25°C, with respect to I/P |
| Supply voltage rejection | PSRR | | 70 | | dB | +25°C, with respect to I/P offset |
| Clock input: | | | | | | |
| Common mode range | CMRC | $V_{MM}$+2V | | $V_{CC}$-1.35V | V | |
| Differential swing | DS | 400 | | 1600 | mV | |

NOTES 1. Guaranteed but not tested.

**Dynamic Characteristics (Note 1)**

See dynamic test circuit Fig.9.

| Characteristic | Symbol | Value | | | Units | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Latch setup time | $t_S$ | | 150 | | ps | 20mV overdrive |
| Hold time | $t_H$ | | 600 | | ps | 20mV overdrive |
| Input to Q delay | $t_{IQ}$ | | 800 | | ps | 20mV overdrive |
| Latch to Q delay | $t_{LQ}$ | | 1500 | | ps | 20mV overdrive |
| Glitch capture regeneration | $t_{RD}$ | | 900 | | ps | 20mV overdrive at Qn |
| Propagation delay matching | $t_{PDM}$ | -100 | | +100 | ps | Within each device |
| Min. compare pulse width | $t_{PW}$ | | 950 | | ps | 20mV overdrive |
| Min. reset pulse width | $t_{RM}$ | | 800 | | ps | |
| Max. flip flop reset time | $t_{RR}$ | | 800 | | ps | |
| Min. hold time of Qn after reset | $t_{GH}$ | | 800 | | ps | |
| Delay between Qn and Gn | $t_{QG}$ | | 900 | | ps | |
| Propagation delay RES to Gn | $t_{RG}$ | | 800 | | ps | |

NOTES 1. Guaranteed but not tested.

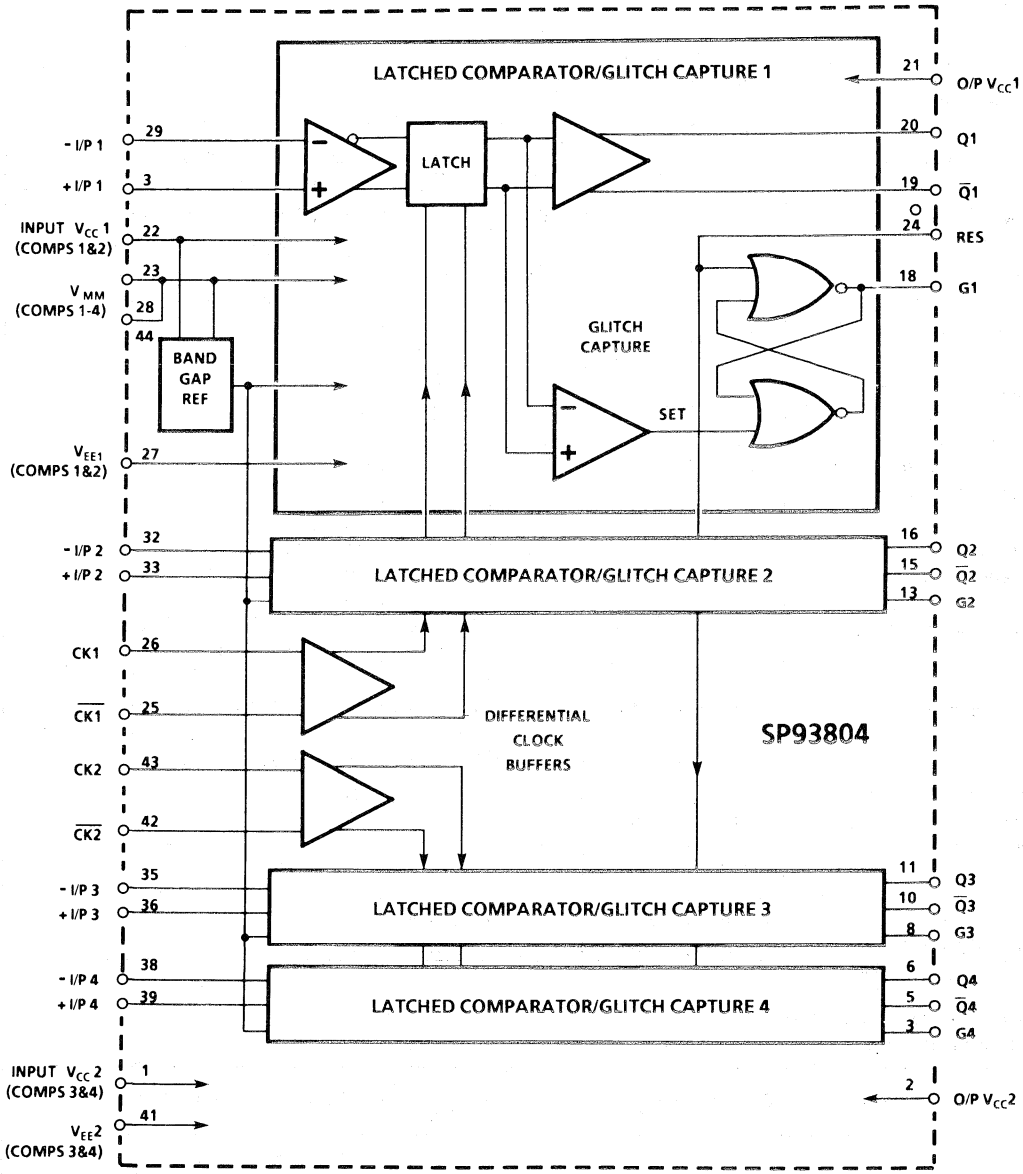



*Fig.2 Internal block diagram (all comparators are as detailed for comparator 1)*

## PIN FUNCTIONS

| Name | Pin | Description |
|---|---|---|
| I/P $V_{CC}1$ | 22 | Positive supply connection for comparators 1 and 2, and the bandgap reference. |
| O/P $V_{CC}1$ | 21 | Positive supply connection for the outputs Qn, $\overline{Qn}$ and Gn of comparators 1 and 2 (emitter follower outputs, see Fig.5). |
| I/P $V_{CC}2$ | 1 | Positive supply connection for comparators 3 and 4. |
| O/P $V_{CC}2$ | 2 | Positive supply connection for the outputs Qn, $\overline{Qn}$ and Gn of comparators 3 and 4 (emitter follower outputs, see Fig.5). |
| -I/Pn<br>+I/Pn | 29/32, 35/38,<br>30/33, 36/39 | Inverting and non-inverting inputs to comparators 1 to 4, respectively. |
| Qn/$\overline{Qn}$ | 6/5, 11/10,<br>16/15, 20/19 | Q and Q outputs of comparators 1 to 4, respectively. |
| Gn | 18,13,8,3 | Outputs of glitch capture circuits 1 to 4, respectively. |
| RES | 24 | Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (Gn) of the Glitch capture circuits to '0'. |
| CLK1, $\overline{CLK1}$ | 25, 26 | Clock input pins for comparators 1 and 2. Active low signal which latches the outputs of comparators 1 and 2. |
| CLK2, $\overline{CLK2}$ | 42, 43 | Clock input pins for comparators 3 and 4. Active low signal which latches the outputs of comparators 3 and 4. |
| $V_{EE}1$ | 27 | Negative supply voltage for comparators 1 and 2. |
| $V_{EE}2$ | 41 | Negative supply voltage for comparators 3 and 4. |
| $V_{MM}$ | 23,44,28 | Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref. |

## OPERATING NOTES

### Transparent Mode

The SP93804 has been designed to maximise high input impedance and minimise propagation delay whilst maintaining a high gain.

While CLK is high ($\overline{CLK}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 20dB. In this mode, for example, a 20mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93804 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

### Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{CLK}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

### Supply Connections

The SP93804 operates from supply voltages of 0V, -5V and -10V (Fig.3) or ±5V (Fig.4). The choice of supply connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from $V_{CC}$, then to interface with other ECL circuits directly, supplies of 0V, -5V, -10V should be provided. This will give an input common mode range of -2.4V to -7.3V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage ($V_{MM}$), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

Note that the O/P $V_{CC}$ pins are connected to the collectors of the output emitter followers; load return currents should therefore be directed towards these device pins.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5V supply is not available.

The SP93804 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5V rails.

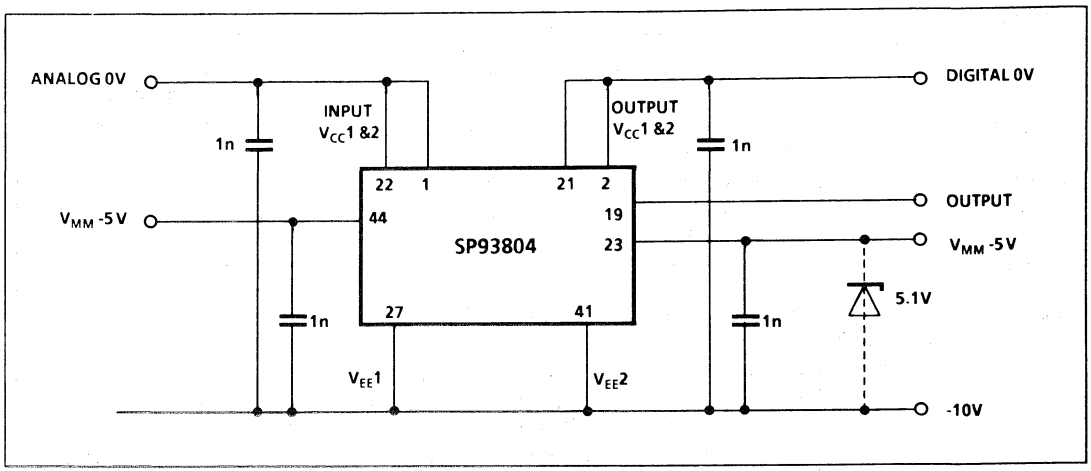



*Fig.3 Connection to 0V, -5V and -10V*

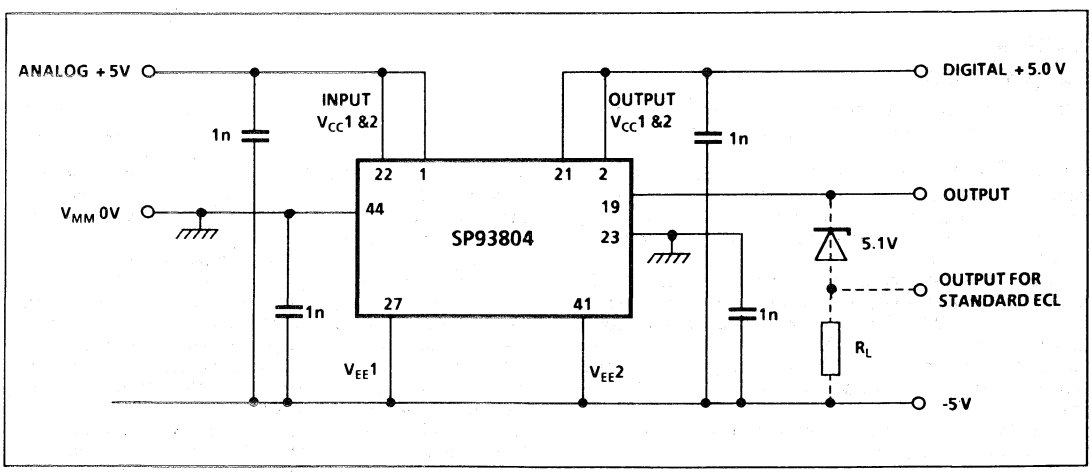



*Fig.4 Connection to ±5V*

## External Components

The Qn, $\overline{Q}$n and Gn outputs are open emitters and therefore required external pulldown resistors ($R_L$). These resistors may be in the range of 50-250Ω connected to $V_{CC}$-2V ($V_T$) or 250-2000Ω connected to $V_{MM}$.

Due to the sub-ns conversion speeds and edge speeds of this device, the performance is dependent on both board layout and component placement.

The performance of the comparator is enhanced by minimising the number of external components and minimising the external strays around the device. The use of high quality chip resistors is recommended, especially for loads.

Decoupling capacitors should be positioned close to the device supply pins. Decoupling between supplies and $V_{EE}$ is also recommended.

The device has been packaged for maximum isolation between channels. This has been achieved by positioning an un-bonded (not internally connected) pin between each set of comparator inputs. These N/C pins can be connected to the ground plane, providing further isolation.

## Clock Inputs

The SP93804 can be used in transparent mode by connecting the CLK input to ECL '1' and the $\overline{CLK}$ input to an ECL '0'. The device can also be used as two dual comparators as comparators 1 and 2 can be clocked separately from comparators 3 and 4.

As the device contains two clock input buffers, a range of clock input configurations are possible. With the device $V_{CC}$ connected to 0V the clock inputs will accept standard differential ECL signals. However optimum performance in terms of crosstalk will be achieved with a differential input of 400mV p-p.

A range of clock input configurations are possible according to the various supply operating.

$\overline{CLK1}$ (pin 25) comparators 1 and 2 latch when low.
$\overline{CLK1}$ (pin 26) inverse clock for comparators 1 and 2.
$\overline{CLK2}$ (pin 43) comparators 3 and 4 latch when low.
$\overline{CLK2}$ (pin 42) inverse clock for comparators 3 and 4.

The clock inputs should have fast rise times and low jitter. The SP92701 line receiver can be used to clean up the clock signal and provide a good differential ECL drive for this comparator

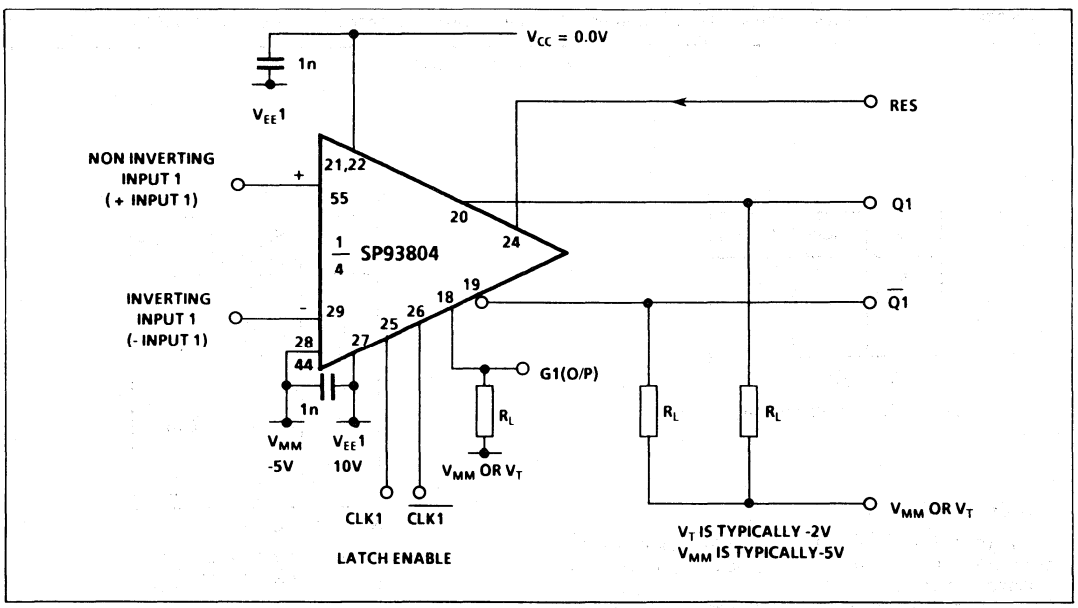



*Fig.5 Applications circuit (one channel)*

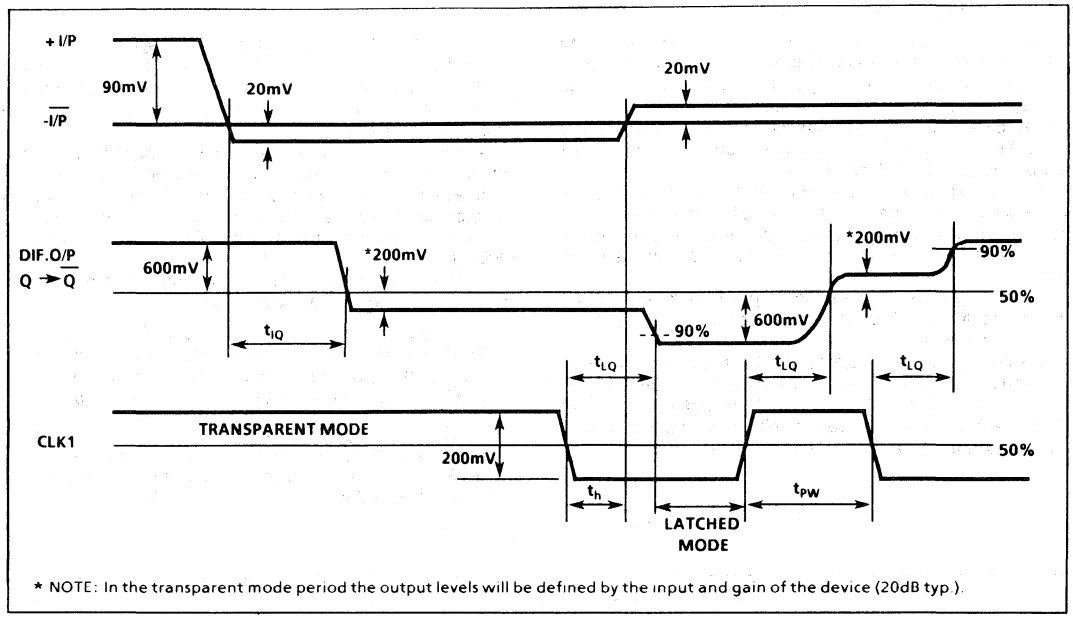



*Fig.6 Comparator timing diagram*

| I/P | CLK | Qn + 1 |
|---|---|---|
| X | 0 | Qn |
| 1 | 1 | 1 |
| 0 | 1 | 0 |

X = Don't Care

*Table 1 Truth table for comparator*

| RES | SET(1) (n + 1) | Gn + 1 |
|---|---|---|
| 1 | X | 0 |
| 0 | ↗ | ↗ |
| 0 | ↘ | 1 |
| 0 | 1 | 1 |
| 0 | 0 | Gn(2) |
| ↘ | 1 | ↗ |
| ↘ | 0 | 0 |

X = Don't Care

*Table 2 Truth table for glitch capture circuit*

## Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' ($V_{CC}$-0.8V) the RES pin will reset the Gn output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Qn goes positive by more than 20mV for a time $>t_{RD}$ then the Gn output will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

NOTES
1. SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.8.
2. Gn = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

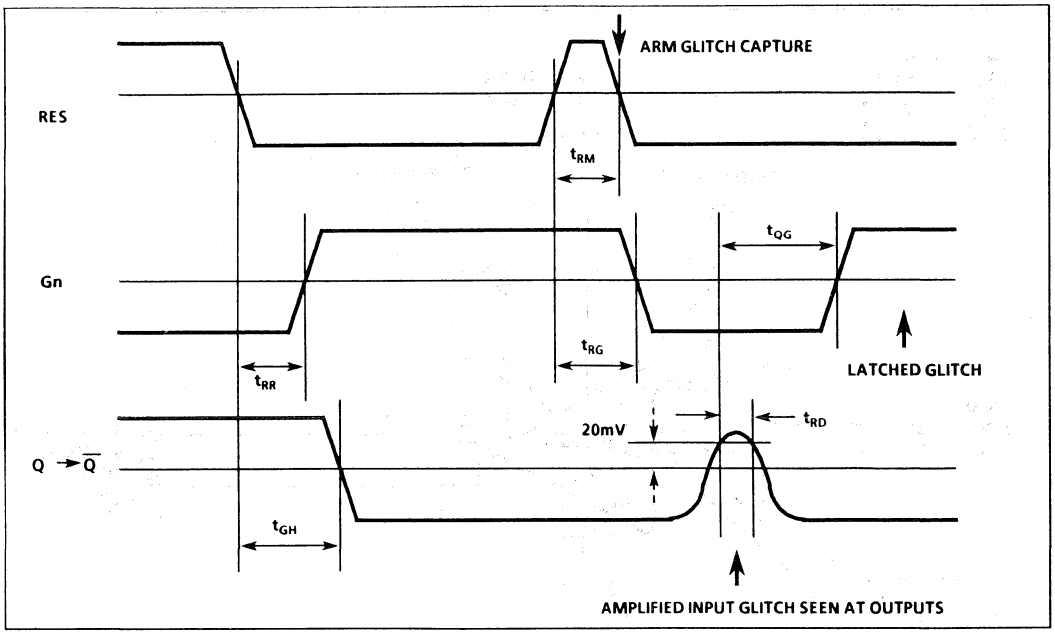
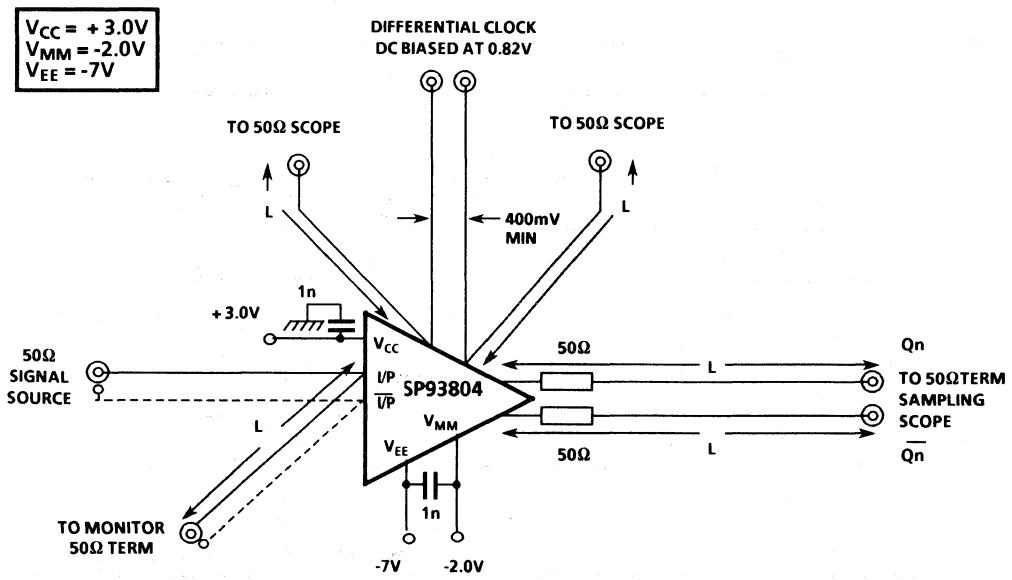



*Fig.7 Glitch capture circuit timing*




NOTES:-

The supplies have been chosen to allow direct connection of both the outputs and monitor points to measurement instruments with 50Ω input impedance.

1) Lead lengths should be as short as possible and also of equal length. (equal delay).
2) Decoupling should be close to the device (chip type if possible).
3) Use coaxial cables or stripline techniques in board construction.
4) Monitor and both scope channel 50Ω loads must be in circuit for correct termination.
5) An SP92701 can be used with supplies of +3V and -2V, to drive the clock input. The outputs of the SP92701 should have series 100Ω resistors to reduce the differential swing.

*Fig.8 - Comparator Test Circuit (one channel)*

# SP93808

## SUB-NANOSECOND OCTAL COMPARATOR

The SP93808 contains eight independent matched ultra high speed comparators. Each comparator is followed by a latch which may be used to sample the comparator output. The gain of this comparator has been optimised for low propagation delay and high stability, therefore hysteresis is rarely required.

Each channel includes a glitch capture circuit which enables the detection and latching of a 20mVns output glitch, when the device is in compare mode. The SP93808 can also be used as two matched quad devices, due to comparators 1 to 4 being clocked separately from comparators 5 to 8.

Special attention has been paid to the clock circuit and packaging to minimise crosstalk.

These features are not only beneficial to logic analyser and counter designs, but also in many other high speed data conversion or data communication systems.

### ORDERING INFORMATION

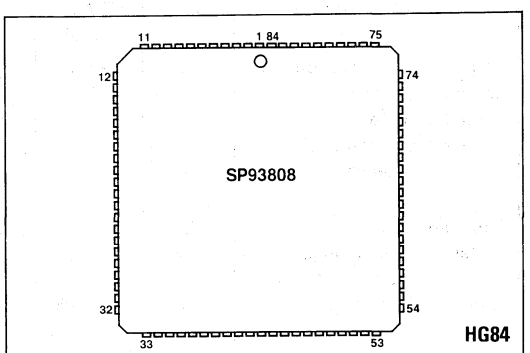
**SP93808 B HG** (Industrial - Quad Cerpac (J-Form) package)

### FEATURES

- -40°C to +85°C Temperature Range
- Typical Delay <1ns
- Glitch Capture, 20mVns (Typ.)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- 8 Matched Comparator/Latched Channels
- Channel Propagation Delay Matching <100ps
- High Input Impedance
- Dual and Quad Versions SP93802/SP93804

### APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers




| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 1 | O/P Vcc2 | 22 | G4 | 43 | I/P Vcc1 | 64 | +I/P4 |
| 2 | GB | 23 | NC | 44 | VMM | 65 | NC |
| 3 | NC | 24 | Q4 | 45 | RES | 66 | -I/P5 |
| 4 | Q8 | 25 | $\overline{Q4}$ | 46 | NC | 67 | +I/P5 |
| 5 | $\overline{Q8}$ | 26 | NC | 47 | CLK1 | 68 | NC |
| 6 | NC | 27 | G3 | 48 | CLK1 | 69 | -I/P6 |
| 7 | G7 | 28 | NC | 49 | NC | 70 | +I/P6 |
| 8 | NC | 29 | Q3 | 50 | VEE1 | 71 | NC |
| 9 | Q7 | 30 | $\overline{Q3}$ | 51 | VEE1 | 72 | -I/P7 |
| 10 | $\overline{Q7}$ | 31 | NC | 52 | VMM | 73 | +I/P7 |
| 11 | NC | 32 | G2 | 53 | NC | 74 | NC |
| 12 | G6 | 33 | NC | 54 | -I/P1 | 75 | -I/P8 |
| 13 | NC | 34 | Q2 | 55 | +I/P1 | 76 | +I/P8 |
| 14 | Q6 | 35 | $\overline{Q2}$ | 56 | NC | 77 | NC |
| 15 | $\overline{Q6}$ | 36 | NC | 57 | -I/P2 | 78 | VEE2 |
| 16 | NC | 37 | G1 | 58 | +I/P2 | 79 | VEE2 |
| 17 | G5 | 38 | NC | 59 | NC | 80 | $\overline{CLK2}$ |
| 18 | NC | 39 | Q1 | 60 | -I/P3 | 81 | CLK2 |
| 19 | Q5 | 40 | $\overline{Q1}$ | 61 | +I/P3 | 82 | VMM |
| 20 | $\overline{Q5}$ | 41 | O/P Vcc1 | 62 | NC | 83 | I/P Vcc2 |
| 21 | NC | 42 | O/P Vcc1 | 63 | -I/P4 | 84 | O/P Vcc2 |

*Fig.1 Pin connections - top view*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage Vcc - VMM | +6V |
| Supply voltage VMM - VEE | -6V |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -55°C to +125°C |
| Output current | ≤30mA |
| Maximum input voltage | |
| Common mode positive | ≤Vcc |
| Common mode negative | ≥VEE |
| Differential input voltage | ≤±3.8V |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ -40°C to +85°C, I/P and O/P $V_{CC}$ = +5V ± 0.25V,
$V_{EE}$ = -5V ± 0.25V, $V_{MM}$ = 0V (see Fig.4), Load = 50Ω to $V_{CC}$ - 2V

**Static Characteristics**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply current | $I_{CC}$ | | 65.5 | 84 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5V<br>No load. Each comparator. |
| Negative supply current | $I_{EE}$ | | 33.0 | 42 | mA | $V_{CC}$ = 5V, $V_{EE}$ = -5V<br>No load. Each comparator. |
| Positive supply voltage | $V_{CC}$ | I/P MAX<br>+1.55 | 5.0 | I/P MIN<br>+7.3 | V | |
| Negative supply voltage | $V_{EE}$ | -5.5 | -5 | -4.9 | V | |
| Input offset voltage | $V_{OS}$ | -3.5 | | +3.5 | mV | |
| Input bias current | $I_B$ | | 5.25 | 9 | μA | |
| Input offset current | $I_{OS}$ | | 0.95 | 1.2 | μA | |
| Input capacitance | $C_I$ | | 1.5<br>(Note 1) | | pF | |
| Input impedance | $R_I$ | | 250 | | kΩ | Measured at DC |
| Differential input range | $V_{DIF}$ | | | +3.8 | V | |
| Common mode input range | CMIR | -2.1 | | +2.6 | V | |
| Output voltage high | $V_{OH}$ | $V_{CC}$-1.050 | | $V_{CC}$-0.81 | V | +25°C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-1.140 | | $V_{CC}$-0.91 | V | -40°C, $V_{IN}$ > 60mV |
| | | $V_{CC}$-0.965 | | $V_{CC}$-0.704 | V | +85°C, $V_{IN}$ > 60mV |
| Output voltage low | $V_{OL}$ | $V_{CC}$-1.712 | | $V_{CC}$-1.544 | V | +25°C, $V_{IN}$ < -60mV |
| | | $V_{CC}$-1.792 | | $V_{CC}$-1.650 | V | -40°C, $V_{IN}$ < -60mV |
| | | $V_{CC}$-1.638 | | $V_{CC}$-1.465 | V | +85°C, $V_{IN}$ < -60mV |
| Gain (transparent mode) | | | 20 | | dB | Differential |
| Common mode rejection | CMRR | 50 | 50 | | dB | +25°C, with respect to I/P |
| Supply voltage rejection | PSRR | | 70 | | dB | +25°C, with respect to I/P offset |
| Clock input: | | | | | | |
| Common mode range | CMRC | $V_{MM}$+2V | | $V_{CC}$-1.35V | V | |
| Differential swing | DS | 400 | | 1600 | mV | |

NOTES 1. Guaranteed but not tested.

**Dynamic Characteristics (Note 1)** See dynamic test circuit Fig.9.

| Characteristic | Symbol | Value | | | Units | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Latch setup time | $t_S$ | | 150 | | ps | 20mV overdrive |
| Hold time | $t_H$ | | 600 | | ps | 20mV overdrive |
| Input to Q delay | $t_{IQ}$ | | 800 | | ps | 20mV overdrive |
| Latch to Q delay | $t_{LQ}$ | | 1500 | | ps | 20mV overdrive |
| Glitch capture regeneration | $t_{RD}$ | | 900 | | ps | 20mV overdrive at Qn |
| Propagation delay matching | $t_{PDM}$ | -100 | | +100 | ps | Within each device |
| Min. compare pulse width | $t_{PW}$ | | 950 | | ps | 20mV overdrive |
| Min. reset pulse width | $t_{RM}$ | | 800 | | ps | |
| Max. flip flop reset time | $t_{RR}$ | | 800 | | ps | |
| Min. hold time of Qn after reset | $t_{GH}$ | | 800 | | ps | |
| Delay between Qn and Gn | $t_{QG}$ | | 900 | | ps | |
| Propagation delay RES to Gn | $t_{RG}$ | | 800 | | ps | |

NOTES 1. Guaranteed but not tested.

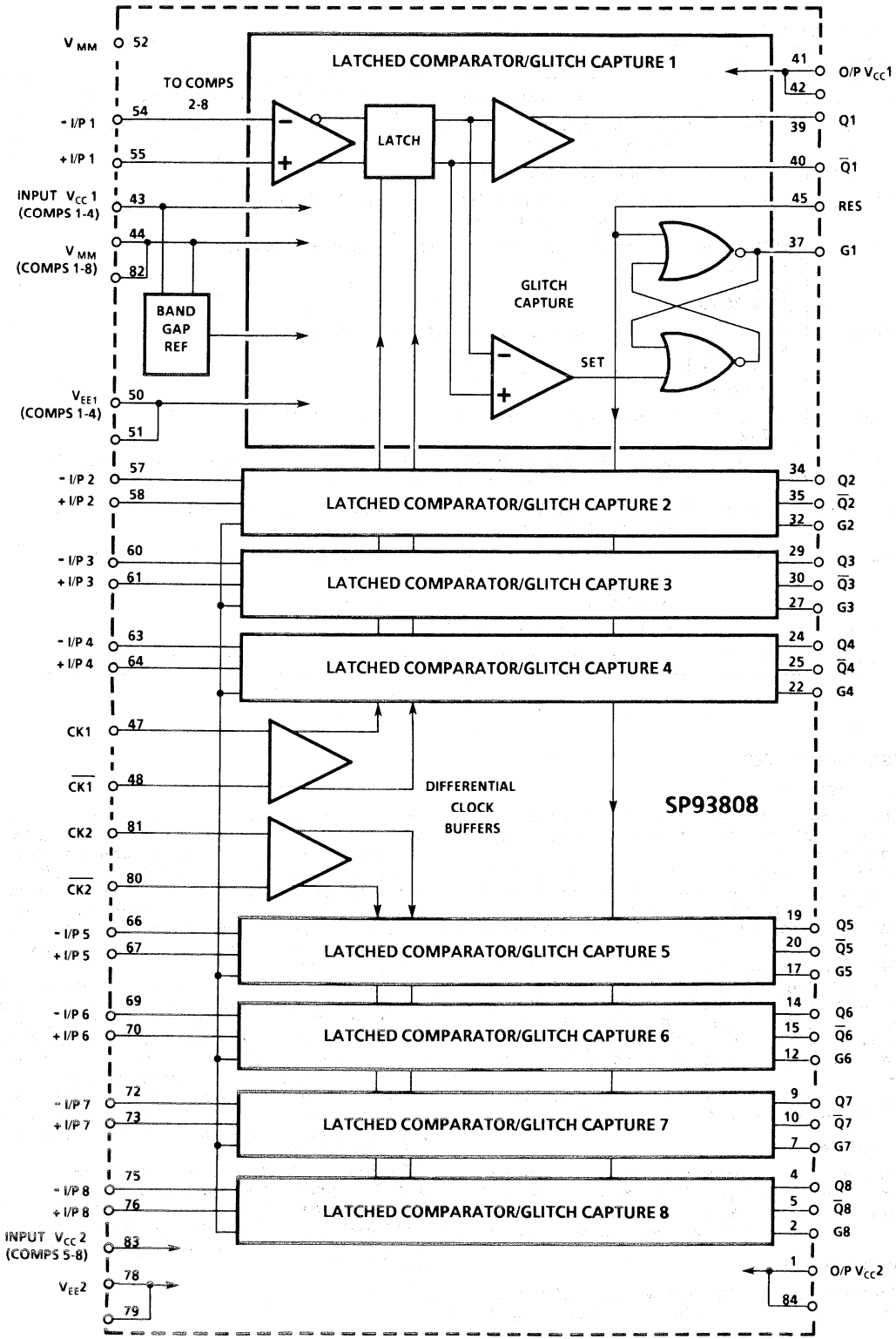



*Fig.2 Internal block diagram (all comparators are as detailed for comparator 1)*

## PIN FUNCTIONS

| Name | Pin | Description |
|---|---|---|
| I/P $V_{CC}1$ | 43 | Positive supply connection for comparators 1 to 4, and the bandgap reference. |
| O/P $V_{CC}1$ | 41 & 42 | Positive supply connection for the outputs Qn, $\overline{Q}$n and Gn of comparators 1 to 4 (emitter follower outputs, see Fig.5). |
| I/P $V_{CC}2$ | 83 | Positive supply connection for comparators 5 to 8. |
| O/P $V_{CC}2$ | 1 & 84 | Positive supply connection for the outputs Qn, $\overline{Q}$n and Gn of comparators 5 to 8 (emitter follower outputs, see Fig.5). |
| -I/Pn<br>+I/Pn | 54/55, 57/58, 60/61, 63/64, 66/67, 69/70, 72/73, 75/76 | Inverting and non-inverting inputs to comparators 1 to 8, respectively. |
| Qn/Qn | 40/39, 35/34, 30/29, 25/24, 20/19, 15/14, 10/9, 5/4 | Q and $\overline{Q}$ outputs of comparators 1 to 8, respectively. |
| Gn | 37,32,27,22, 17,12,7,2 | Outputs of glitch capture circuits 1 to 8, respectively. |
| RES | 45 | Reset pin for glitch capture circuit. This active high ECL signal will set the outputs (Gn) of the Glitch capture circuits to '0'. |
| CLK1, $\overline{CLK1}$ | 47,48 | Clock input pins for comparators 1 to 4. ECL active low signal which latches the outputs of comparators 1 to 4. |
| CLK2, $\overline{CLK2}$ | 80,81 | Clock input pins for comparators 5 to 8. ECL active low signal which latches the outputs of comparators 5 to 8. |
| $V_{EE}1$ | 50 & 51 | Negative supply voltage for comparators 1 to 4. |
| $V_{EE}2$ | 78 & 79 | Negative supply voltage for comparators 5 to 8. |
| $V_{MM}$ | 44,82,52 | Mid-supply voltage rail for reset, clock drivers, glitch capture and band gap ref. |

## OPERATING NOTES

### Transparent Mode

The SP93808 has been designed to maximise high input impedance and minimise propagation delay whilst maintaining a high gain.

While CLK is high ($\overline{CLK}$ low), the outputs of the comparators are unlatched and are therefore transparent, with a gain of typically 20dB. In this mode, for example, a 20mV input overdrive signal will result in a 200mV differential output.

For applications such as logic analyser probes etc. this output signal may then be passed along a transmission line to a second SP93808 to enable strobing at a remote point from the comparator. Thus the gain and delay has been distributed within the application. The net result is reduced overall propagation delay and reduced channel to channel time skew.

In the transparent mode of operation the glitch capture circuit is continuously active.

### Latched Mode

The output of each comparator is strobed into a very high bandwidth latch by taking CLK low ($\overline{CLK}$ high). The latch will then regenerate and produce full ECL output levels. This method produces the minimum system propagation delay.

### Supply Connections

The SP93808 operates from supply voltages of 0V, -5V and -10V (Fig.3) or ±5V (Fig.4). The choice of supply connections depends on the input voltage range required and also the input voltage of the following circuits. As the ECL outputs from this device are 0.8V down from $V_{CC}$, then to interface with other ECL circuits directly, supplies of 0V, -5V, -10V should be provided. This will give an input common mode range of -2.4V to -7.3V. Therefore when two devices are used in a system, the first (line driver) should have supplies as shown in Fig.3 and the second (line receiver) should have supplies as shown in Fig.4.

If it is inconvenient to provide the mid-supply voltage ($V_{MM}$), then a 5.1V Zener diode can be used. The current taken by this diode will be typically 32mA, see Fig.3.

Note that the O/P $V_{CC}$ pins are connected to the collectors of the output emitter followers; load return currents should therefore be directed towards these device pins.

The supply connections shown in Fig.3 give output levels that are directly compatible with ECL 10k inputs. An optional 5.1V Zener diode is shown; this is only required if a -5V supply is not available.

The SP93808 ECL outputs can be connected directly to other ECL circuitry if these circuits are supplied from the +5V and 0V rails (O/PH, see Fig.4). Alternatively, a 5.1V Zener diode can be used to level shift the outputs for connection to standard ECL circuits supplied from the 0V and -5V rails.

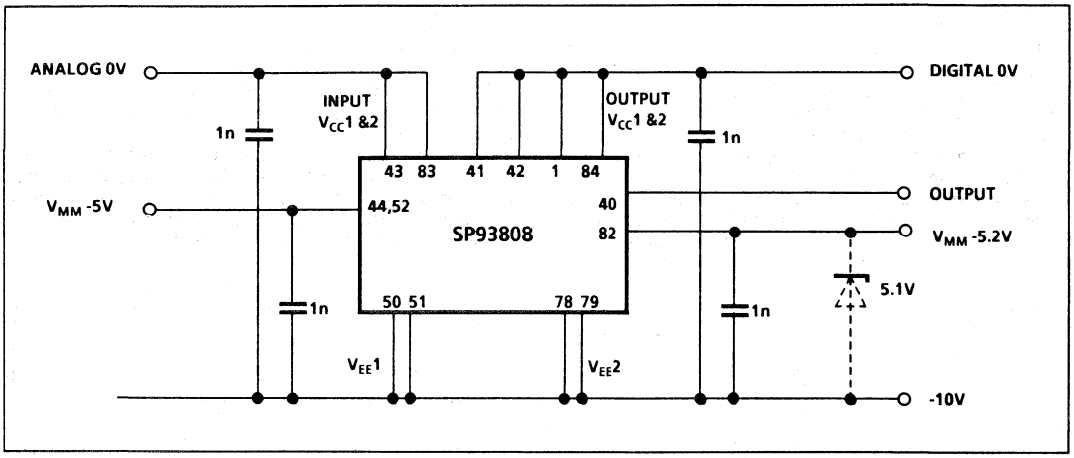



*Fig.3 Connection to 0V, -5V and -10V*

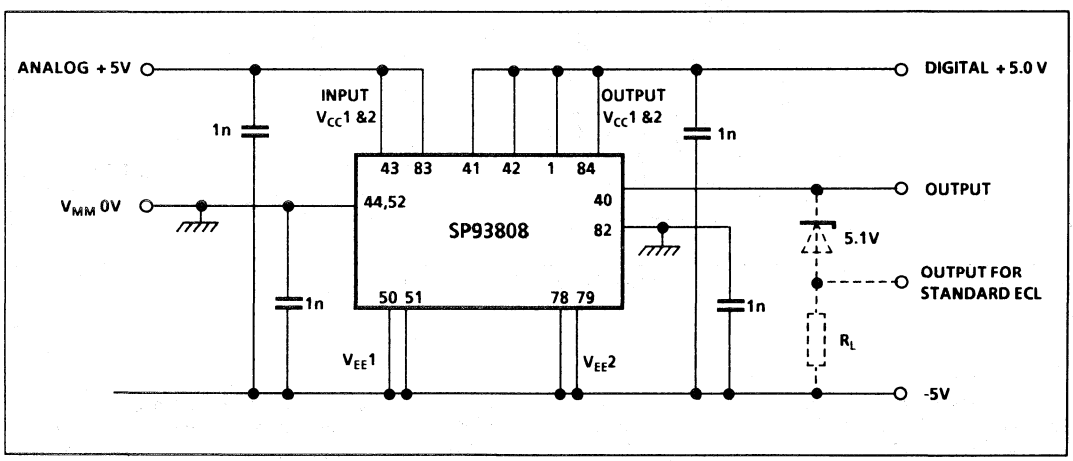



*Fig.4 Connection to ±5V*

## External Components

The Qn, $\overline{Qn}$ and Gn outputs are open emitters and therefore required external pulldown resistors ($R_L$). These resistors may be in the range of 50-250Ω connected to $V_{CC}$-2V ($V_T$) or 250-2000Ω connected to $V_{MM}$.

Due to the sub-ns conversion speeds and edge speeds of this device, the performance is dependent on both board layout and component placement.

The performance of the comparator is enhanced by minimising the number of external components and minimising the external strays around the device. The use of high quality chip resistors is recommended, especially for loads.

Decoupling capacitors should be positioned close to the device supply pins. Decoupling between supplies and $V_{EE}$ is also recommended.

The device has been packaged for maximum isolation between channels. This has been achieved by positioning an un-bonded (not internally connected) pin between each set of comparator inputs. These N/C pins can be connected to the ground plane, providing further isolation.

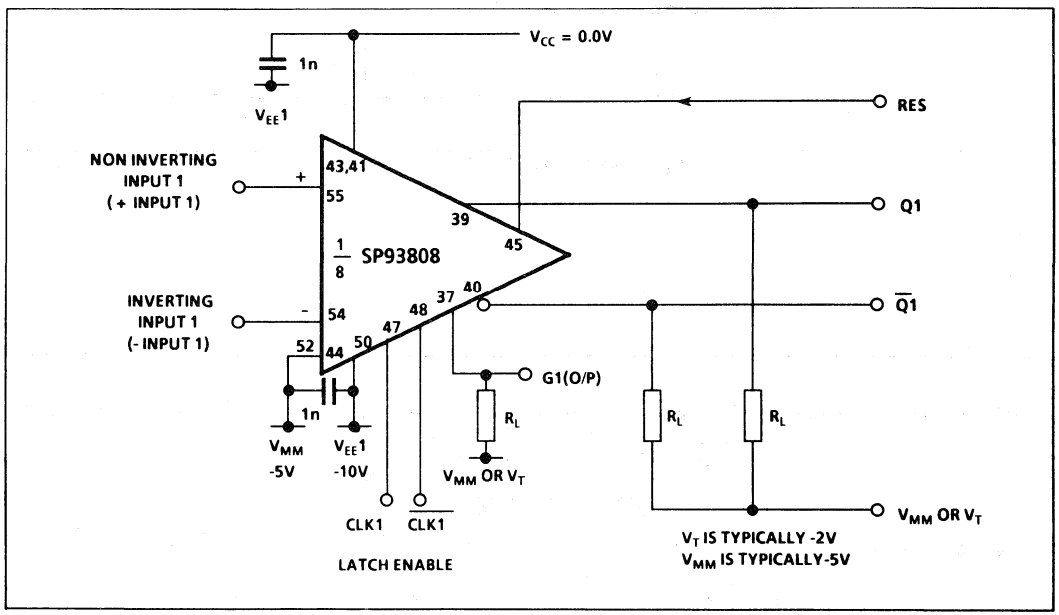



*Fig.5 Applications circuit (one channel)*

## Clock Inputs

The SP93808 can be used in transparent mode by connecting the CLK input to ECL '1' and the $\overline{CLK}$ input to an ECL '0'. The device can also be used as a dual quad comparator as comparators 1 to 4 can be clocked separately from comparators 5 to 8.

As the device contains two clock input buffers, a range of clock input configurations are possible. With the device $V_{CC}$ connected to 0V the clock inputs will accept standard differential ECL signals. However optimum performance in terms of crosstalk will be achieved with a differential input of 400mV p-p.

CLK1 (pin 47) comparators 1 to 4 latch when low.
$\overline{CLK1}$ (pin 48) inverse clock for comparators 1 to 4.
CLK2 (pin 81) comparators 5 to 8 latch when low.
$\overline{CLK2}$ (pin 80) inverse clock for comparators 5 to 8.

The clock inputs should have fast rise times and low jitter. The SP92701 line receiver can be used to clean up the clock signal and provide a good differential ECL drive for this comparator.

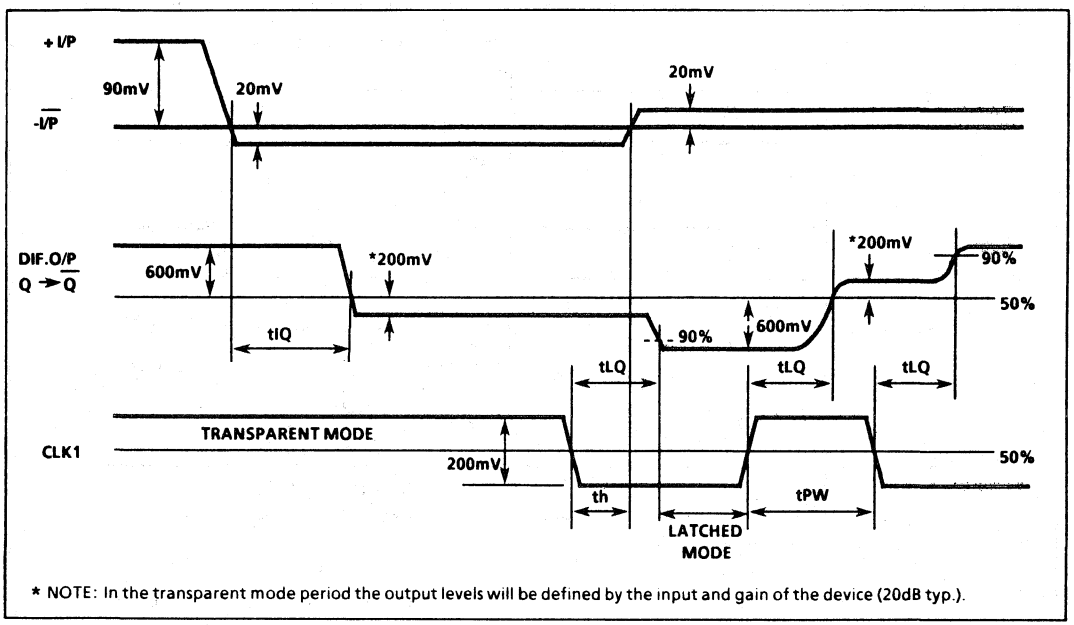



*Fig.6 Comparator timing diagram*

| I/P | CLK | Qn + 1 |
|---|---|---|
| X | 0 | Qn |
| 1 | 1 | 1 |
| 0 | 1 | 0 |

X = Don't Care

*Table 1 Truth table for comparator*

## Glitch Capture Circuit

This advanced feature enables the device to capture sub-nanosecond glitches that may have occurred before the comparator is latched.

The glitch capture circuit (see Fig.2) can be reset at any time by the RES input. When held at ECL '1' ($V_{CC}$-0.8V) the RES pin will reset the Gn output to '0' (ECL low). Glitch capture is active when the RES pin is taken low.

If Qn goes positive by more than 20mV for a time $>t_{RD}$ then the Gn output will be set to an ECL '1', it will remain in this state until the RES pin is again taken high.

| RES | SET(1) (n + 1) | Gn + 1 |
|---|---|---|
| 1 | X | 0 |
| 0 | ↗ | ↗ |
| 0 | ↘ | 1 |
| 0 | 1 | 1 |
| 0 | 0 | Gn(2) |
| ↘ | 1 | ↗ |
| ↘ | 0 | 0 |

X = Don't Care

*Table 2 Truth table for glitch capture circuit*

NOTES
1. SET is the input to the glitch capture circuit and is logically the same as the Q output from the comparator, see Fig.8.
2. Gn = 1 is evidence that a transition has occurred at the Q output since the last falling edge of the reset pulse.

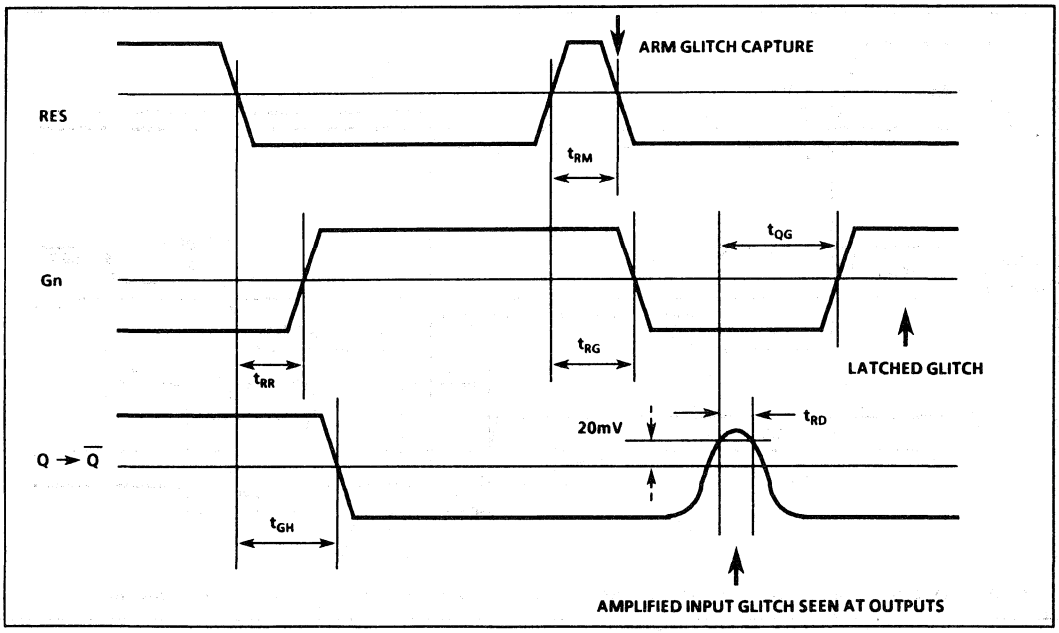
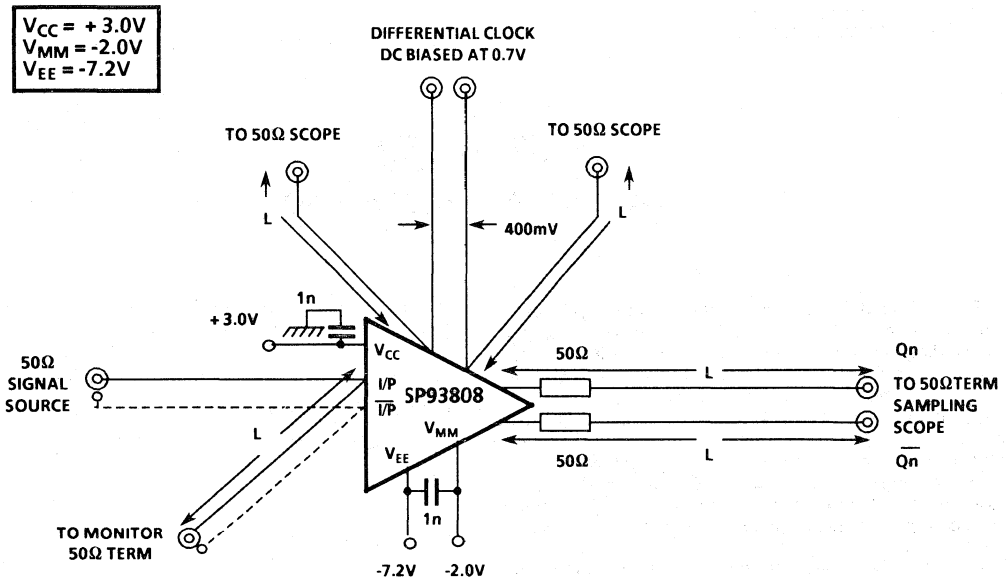



*Fig.7 Glitch capture circuit timing*




NOTES:-

The supplies have been chosen to allow direct connection of both the outputs and monitor points to measurement instruments with 50Ω input impedance.

1) Lead lengths should be as short as possible and also of equal length. (equal delay).
2) Decoupling should be close to the device (chip type if possible).
3) Use coaxial cables or stripline techniques in board construction.
4) Monitor and both scope channel 50Ω loads must be in circuit for correct termination.
5) An SP92701 can be used with supplies of + 3V and -2V, to drive the clock input. The outputs of the SP92701 should have series 100Ω resistors to reduce the differential swing.

*Fig.8 - Comparator Test Circuit (one channel)*

# SP94308

## 8-BIT VIDEO SYSTEM ADC

The SP94308 analog to digital converter has been specially designed for use with NTSC or PAL video signals.

A 1V video signal is AC coupled to the device input, where it is DC clamped, amplified by two and fed through a buffer which drives the ADC input capacitance.

A sync or burst gate pulse can be used to drive the DC clamp circuit. This circuit can be externally adjusted to provide conversion of video only or video and sync.

This analog to digital converter samples the input waveform on the rising edge of the clock and produces a latched output which can be acquired simply by an inverted clock signal.

Also within the SP94308 is an internal clock amplifier and driver. This allows a low level clock signal to be AC coupled directly into the device for applications that may be sensitive to clock radiation.

The clock frequency and analog bandwidth of the SP94308 are compatible with both PAL and NTSC standards where conversion of luma or full composite video signals are required.

### FEATURES

- 8 Bits, 20MHz
- ±0.75 LSB Differential Linearity (Typ.)
- No Sample and Hold or Input Buffer Required
- Internal Clock Amplifier
- Internal Clamp Circuit
- Internal Output Latch
- 6MHz Min. Analog Bandwidth
- Output Levels are TTL/CMOS Compatible
- 0°C to 70°C Temperature Range
- Full Static Protection
- On Chip ×2 Amplifier and ADC Buffer

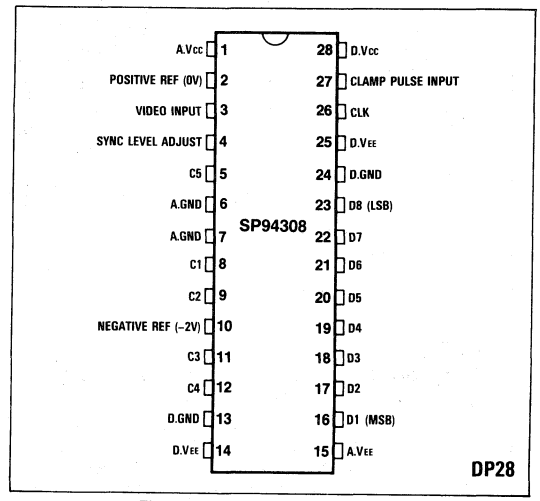



*Fig.1 Pin connections - top view*

### ORDERING INFORMATION

**SP94308C DP** (Commercial - Plastic DIL package)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$-$V_{EE}$ | <12V |
| Output current | <20mA |
| Storage temperature | -65°C to +150°C |
| Junction operating temperature | <150°C |

### THERMAL INFORMATION

Chip to ambient temperature $\theta_{JA}$ = 55°C/W

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 0°C to 70°C, $V_{CC}$ = +5V ± 0.25V, $V_{EE}$ = -5.2V ± 0.25V

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Positive supply current | $I_{CC}$ | | 35 | 44 | mA | |
| Negative supply current | $I_{EE}$ | | 110 | 150 | mA | |
| Power consumption | | | 750 | | mW | |
| Resolution | | 8 | | | Bits | |
| Reference current | $I_{ref}$ | | 12 | 16 | mA | $V_{ref}$ = -2V |
| Maximum clock rate | fc | 20 | | | MHz | |
| Clock input level | | 0.25 | | 1.0 | V p-p | AC coupled |
| Analog bandwidth | $f_a$ | 6 | | | MHz | Note 3 |
| Input impedance | $R_{IN}$ | 100K | | | Ω | |
| Differential linearity | | | ±0.75 | ±1.0 | LSB | 25°C |
| Integral linearity | | | | ±1.0 | LSB | 25°C |
| Differential gain | | | | 1.5 | % | fc = 20.0MHz |
| Differential phase | | | 1 | | Deg | |
| Logic '1' | $V_{OH}$ | Vcc-1.3 | Vcc-1 | | V | $I_{source}$ = 1mA |
| | $V_{OH}$ | Vcc-1.1 | Vcc-0.9 | | V | $I_{source}$ = 0.1mA |
| Logic '0' | $V_{OL}$ | | 0.3 | 0.4 | V | $I_{sink}$ = 1.6mA (Note 2) |
| Tilt/line | | | -1.5 | | mV | 100nF input capacitor |
| Input level | | | 1 | | V p-p | AC coupled |
| Sync level adjust output | | | -1.4 | | V | Unadjusted (Note 1) |
| Data valid time | $t_V$ | | 45 | | ns | At 20MHz clock |

NOTES
1. Gain of x2 in input stage.
2. See Fig.7 for equivalent TTL load.
3. Guaranteed but not tested.

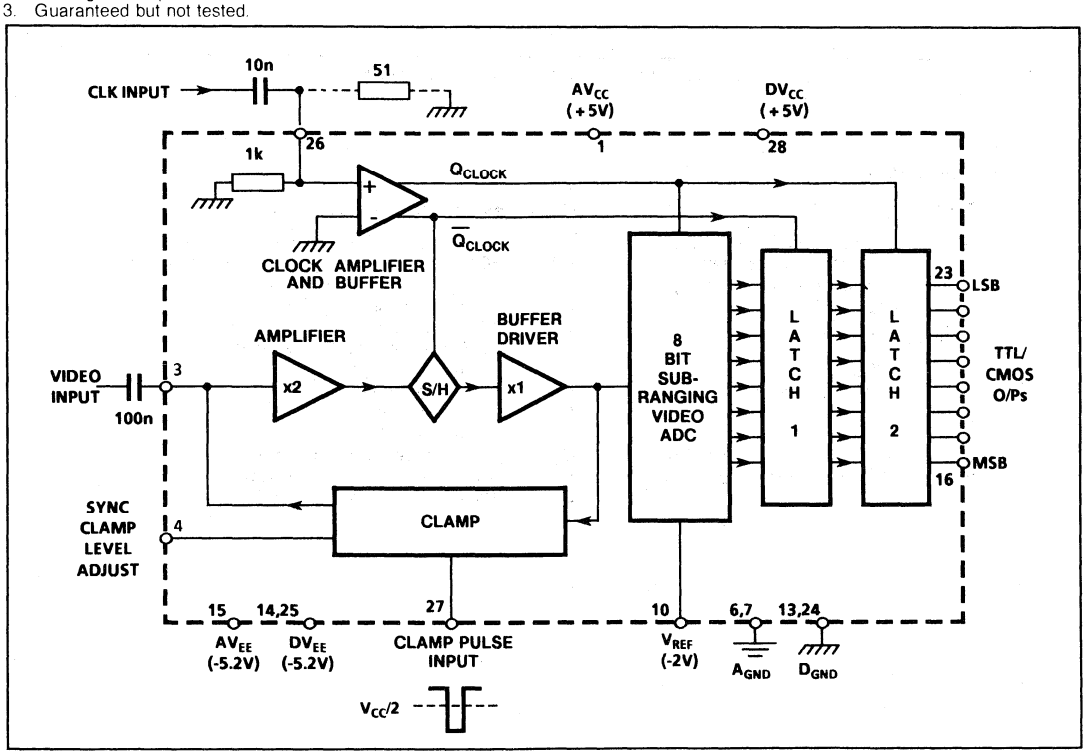



*Fig.2 Internal block diagram*

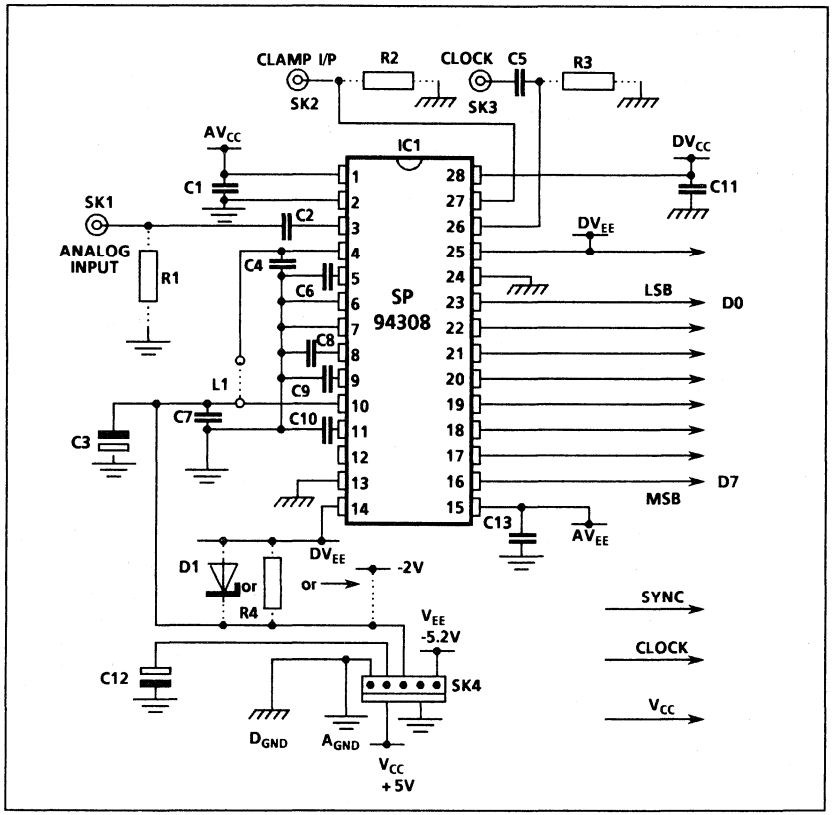



*Fig.3 Minimum component application circuit*

## COMPONENT LIST FOR FIG. 3

### Resistors

| | |
|---|---|
| **R1** | 75Ω (optional termination) |
| **R2** | 47Ω (optional termination) |
| **R3** | 47Ω (optional termination) |
| **R4** | Approx. 560Ω (optional) |

### Semiconductors

| | |
|---|---|
| **IC1** | SP94308 |
| **D1** | BZX79C3V0 (optional) |

### Sockets

| | |
|---|---|
| **S1-S3** | Sub Vis sockets (optional) |
| **S4** | KK Molex socket (optional) |

### Capacitors for ADC, clamp, bias etc.

| | |
|---|---|
| **C1** | 100nF (optional decoupling) |
| **C2** | 100nF (input coupling and line clamp) |
| **C3** | 47μF (electrolytic decoupling) |
| **C4** | 100nF (optional decoupling) |
| **C5** | 100nF (coupling) |
| **C6** | 27pF at 20MHz or 47pF at 10MHz clock |
| **C7** | 100nF (decoupling) |
| **C8** | 100nF (decoupling) |
| **C9** | 100nF (decoupling) |
| **C10** | 100nF (decoupling) |
| **C11** | 100nF (optional decoupling) |
| **C12** | 47μF (electrolytic decoupling) |
| **C13** | 100nF (optional decoupling) |

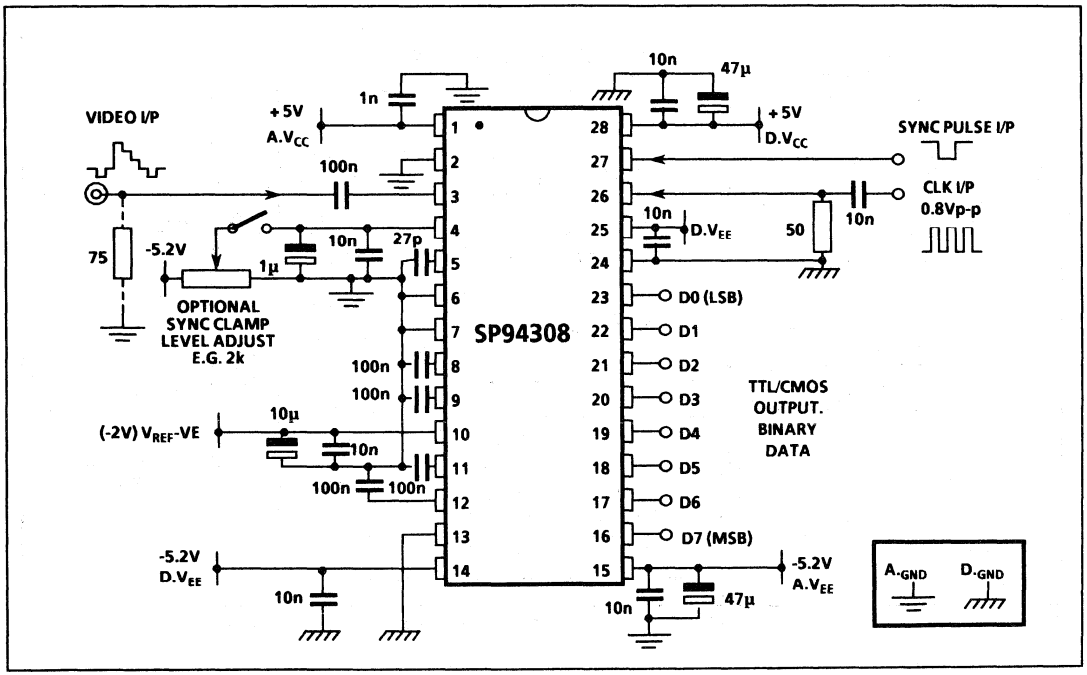



*Fig.4 Full test circuit*

## APPLICATIONS

The SP94308 combines a clamp circuit, sample and hold, x2 amplifier, ADC driver, video ADC and output latch that form a conventional 8-bit video digitising system.

An on-chip clock amplifier allows the device to be clocked from low level sine or square wave signals. This reduces the possibility of patterning due to crosstalk.

The device offers the flexibility for either sync clamping or black level clamping of the video signal.

### Sync Clamp

Sync clamping is provided by applying a negative going clamp pulse to pin 27 during the sync period. This pulse should be more than 1.5µs wide and it should cross the internal switching threshold of $V_{CC}/2$. Pin 4 should be connected to $V_{REF-}$ (pin 10 -2V) to allow the total video with its sync to be digitised.

### Black Level Clamping

This can be achieved by applying a negative clamp pulse to pin 27 within the back porch of the video signal. The clamp pulse should avoid the colour burst - this ensures no attenuation of the burst signal.

The clamping pulse can be derived from a burst gate pulse or by delaying the sync pulse with a dual monostable (SN74123N).

When using a back porch clamping pulse, pin 4 should be decoupled to analog ground using a 100nF capacitor. The device will then self-bias this pin to -1.4V. This provides full digitisation of the video and its sync.

It is also possible to adjust the voltage on pin 4 and reduce the reference voltage pin 10 to provide digitisation of the active video information only.

If a clamp pulse is not readily available within the application it can be generated from the incoming video signal (see circuit shown in Fig.5). The variable resistor RV can be adjusted for different slice levels of the incoming video sync.

The digital outputs of the SP94308 are latched and have a 90% of CLK, data valid time at 20MHz. This allows the 8-Bit TTL output to be acquired simply by an inverse CLK signal. See Fig.6.

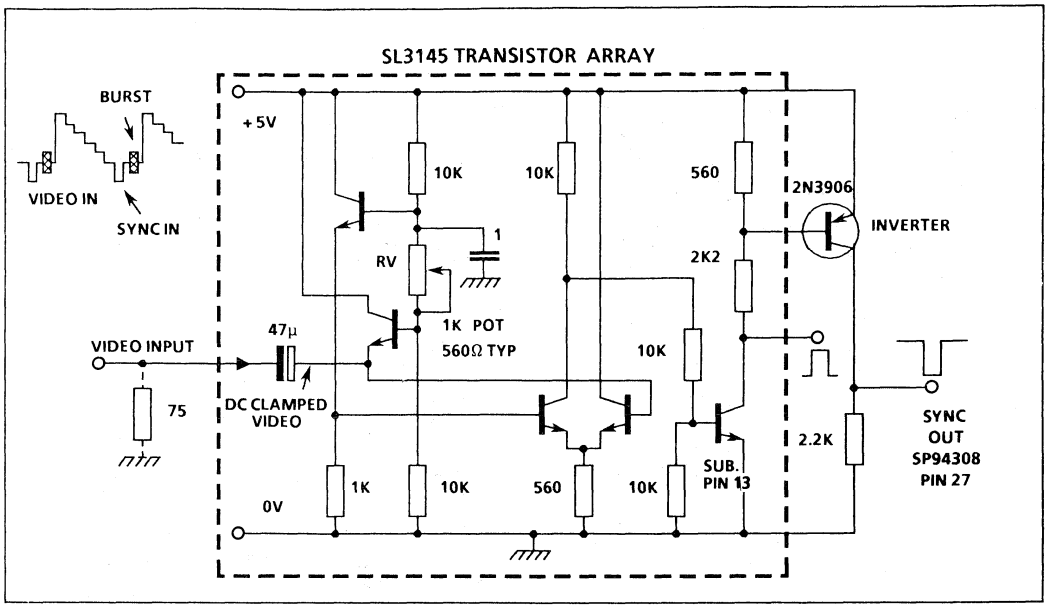



*Fig.5 Sync pulse generation for test/evaluation circuit*

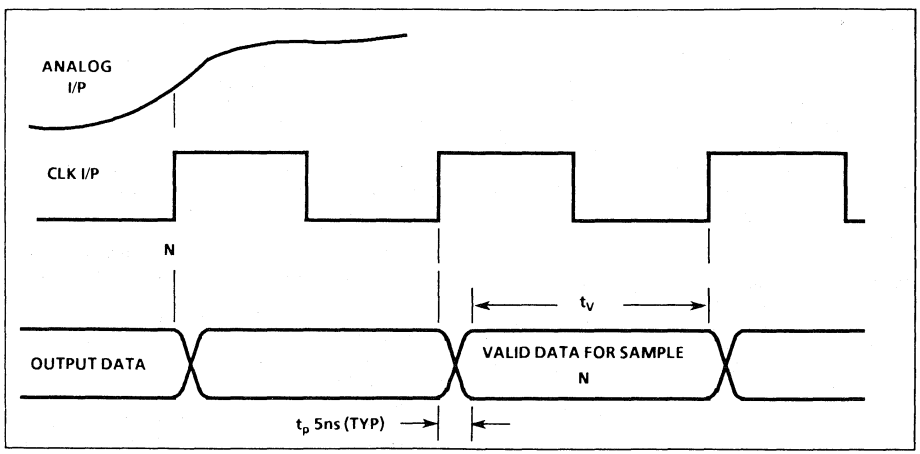



*Fig.6 Timing diagram*

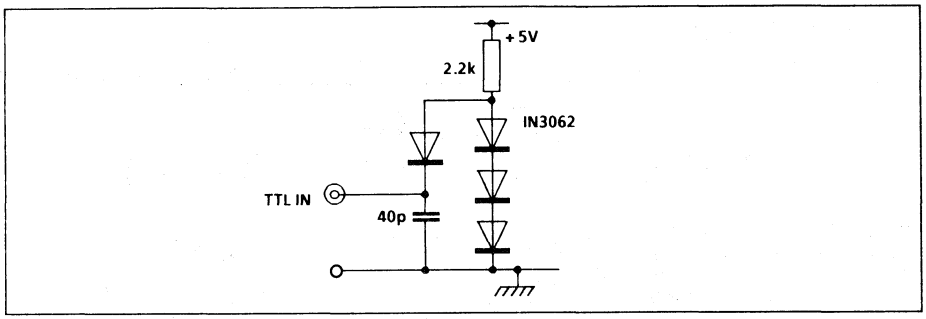



*Fig.7 Equivalent TTL test load*

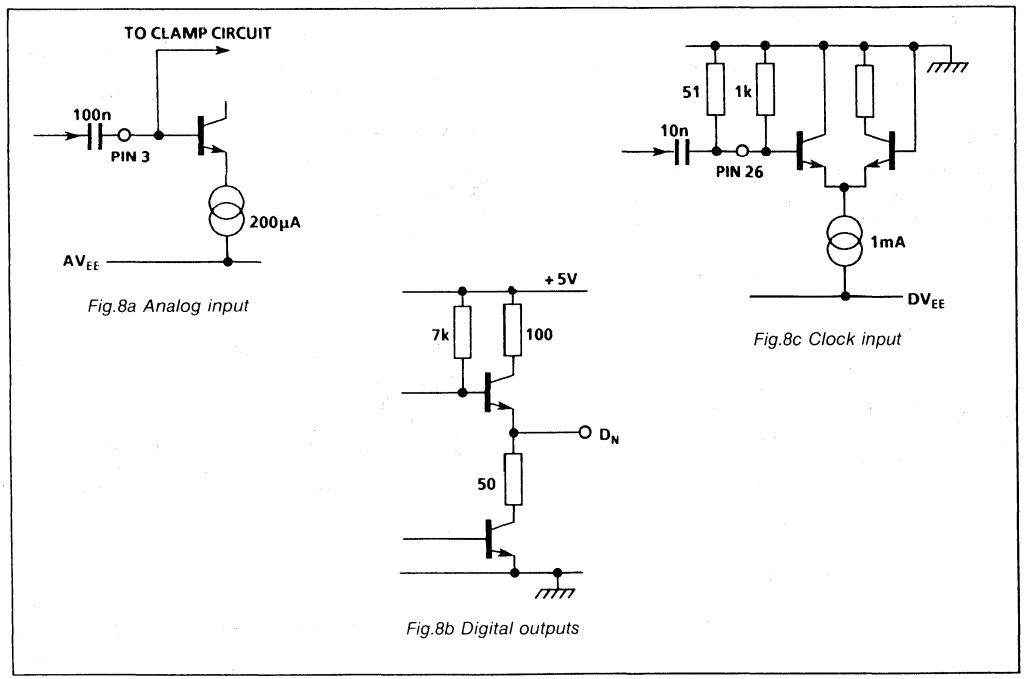



*Fig.8a Analog input*

*Fig.8b Digital outputs*

*Fig.8c Clock input*

*Fig.8 Equivalent device inputs and outputs.*

# SP973T8

## 30MHz 8-BIT FLASH ADC (TTL/CMOS OUTPUTS)

The SP973T8 is a wideband, full flash analog- to-digital converter that requires no preceding sample and hold. The device contains a full 8-bit D-type latch which ensures that the 8 TTL/CMOS outputs are accurately registered and have a good data valid time at high clock speeds.

Operating from a single +5 volt supply the device is capable of conversion rates well in excess of 30 MHz and its wideband input allows signals with frequencies up to the Nyquist limit to be digitised with high accuracy. An internal bandgap voltage regulator gives low DC drift over a wide operating temperature range (-40°C to +85°C in DG package).

The SP973T8 is designed for applications where power consumption and package size is at a premium.

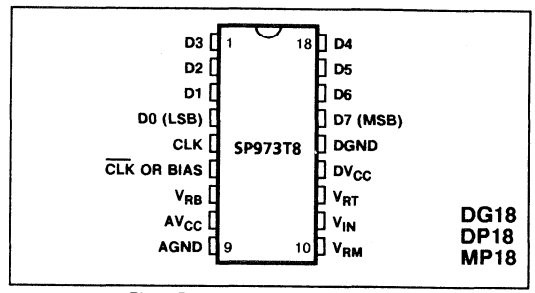



*Fig.1 Pin connections - top view*

### FEATURES

- Flash Converter, No Sample and Hold Required
- Wideband Analog Input 70MHz, 3dB (Typ.)
- Low Power Consumption (600 mW Typ.)
- Latched TTL/CMOS Compatible Outputs
- Wide Operating Temperature Range
- No Missing Codes - Guaranteed
- Designed for Wideband Operation
- Single 5V Supply
- Production Tested at 30MHz

### APPLICATIONS

- Studio Quality Video
- DBS Broadcast Video
- High Resolution TV
- Nucleonics
- Radar
- Computing

### ORDERING INFORMATION

**SP973T8 B DG** (Industrial - Ceramic DIL package)
**SP973T8 C DP** (Commercial - Plastic DIL package)
**SP973T8 C MP** (Commercial - Miniature Plastic DIL package)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | 7V |
| Output Current | 10mA |
| Input Voltage, $V_{IN}$ | $V_{CC}$ |
| Operating Temperature | -40°C to +85°C (BDG) |
| | 0°C to +70°C (CDP/CMP) |
| Storage Temperature | -65°C to +150°C |

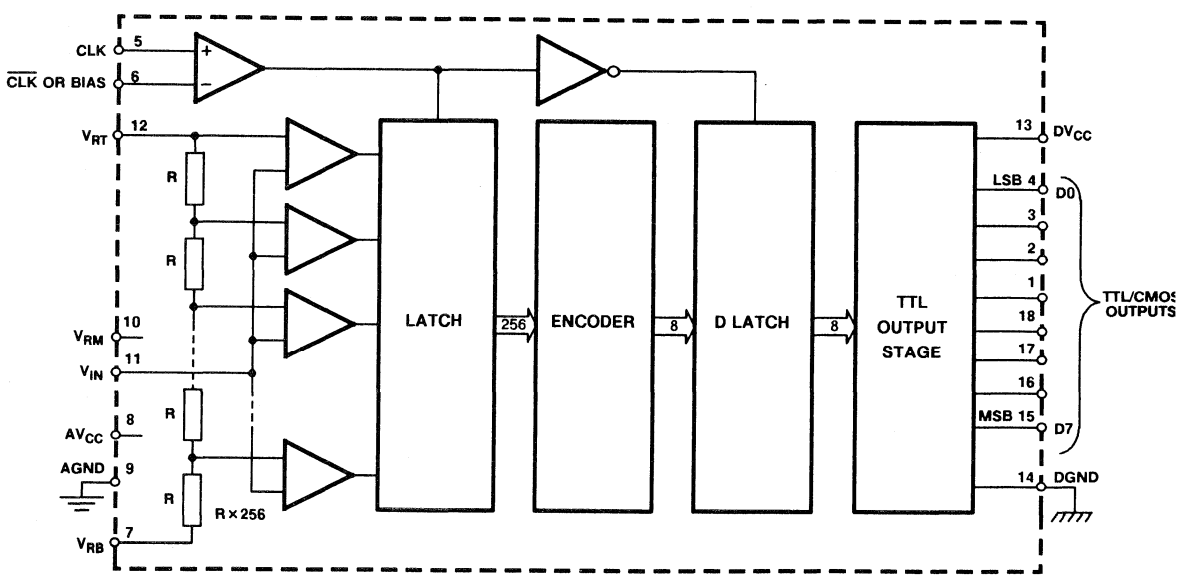



*Fig.2 Internal block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = 25°C, $V_{CC}$ = +5V ± 0.25V

Full temperature range = -40°C to +85°C (SP973T8 B DG), 0°C to +70°C (SP973T8 C DP and SP973T8 C MP)

### DC CHARACTERISTICS

| Characteristic | Symbol | Temp. | Test level | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| **Power Supply** | | | | | | | | |
| Supply current | $I_{CC}$ | Full | 4 | 100 | | 140 | mA | |
| | | 25 | 1 | 110 | 120 | 130 | mA | |
| Power dissipation | $P_D$ | Full | 4 | 475 | | 735 | mW | |
| | | 25 | 1 | 520 | 600 | 680 | mW | |
| **Analog Input** | | | | | | | | |
| Input range | $V_{IN}$ | Full | 4 | 1.8 | | $V_{CC}$-0.7 | V | |
| Input bias current | $I_{IN}$ | 25 | 1 | 150 | 390 | 1100 | µA | $V_{IN} = V_{RT}$ |
| 3dB bandwidth | $f_{3dB}$ | 25 | 4 | | 70 | | MHz | |
| Input capacitance | $C_{IN}$ | 25 | 4 | | 30 | | pF | |
| **Reference Ladder** | | | | | | | | |
| Ladder resistance | $R_D$ | 25 | 1 | 325 | 400 | 475 | Ω | |
| Ladder voltage (top) | $V_{RT}$ | Full | 4 | | 4.3 | $V_{CC}$-0.7 | V | |
| Ladder voltage (bottom) | $V_{RB}$ | Full | 4 | 1.8 | 2.3 | | V | |
| Ladder offset (top) | $V_{RT0}$ | 25 | 5 | | -4 | | mV | |
| Ladder offset (bottom) | $V_{RB0}$ | 25 | 5 | | +3 | | mV | |
| Ladder temp. coeff. | $R_{TC}$ | Full | 5 | | 1.5 | | Ω/°C | |
| **Clock Input** | | | | | | | | |
| Logic '1' voltage | $V_{IH}$ | Full | 4 | 2.75 | 4.3 | $V_{CC}$ | V | A swing of 1V centred on the voltage applied to the $\overline{CLK}$ pin |
| Logic '1' current | $I_{IH}$ | 25 | 1 | | | 25 | µA | |
| Logic '0' voltage | $V_{IL}$ | Full | 4 | 1.75 | 3.3 | $V_{CC}$-1.0 | V | |
| Logic '0' current | $I_{IL}$ | 25 | 1 | | | 2 | µA | |
| **Digital outputs** | | | | | | | | |
| Logic '1' voltage | $V_{OH}$ | Full | 4 | 3.3 | | | V | Into Standard LS TTL Load |
| | | 25 | 1 | 3.5 | 3.8 | | V | |
| Logic '0' voltage | $V_{OL}$ | Full | 4 | | | 0.4 | V | |
| | | 25 | 1 | | 0.1 | 0.4 | V | |
| **Static performance** | | | | | | | | |
| Differential non-linearity | DNL | Full | 4 | | | ±1 | LSB | |
| | | 25 | 4 | | | ±0.5 | LSB | |
| Integral non-linearity | INL | Full | 4 | | | ±1 | LSB | |
| | | 25 | 4 | | | ±1 | LSB | |

### AC CHARACTERISTICS (Refer to Fig 7.)

| Characteristic | Symbol | Temp. | Test level | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| Clock min. high | $t_{PW1}$ | 25 | 4 | 10 | | | ns | |
| Clock min. low | $t_{PW0}$ | 25 | 4 | 10 | | | ns | |
| Max. conversion rate | | Full | 4 | 30 | 50 | | MHz | $A_{IN}$ = 15MHz at FS |
| Aperture delay | $t_{AD}$ | 25 | 5 | | 3 | | ns | |
| Output data delay | $t_D$ | 25 | 4 | | 7 | | ns | |
| Output rise time | $t_R$ | 25 | 4 | | 6 | | ns | |
| Output fall time | $t_F$ | 25 | 4 | | 8 | | ns | |
| **Dynamic Performance** | | | | | | | | With $F_{CLK}$ = 30 MHz |
| Differential non-linearity | DNL | 25 | 1 | -0.85 | ±0.5 | +1 | LSB | $A_{IN\ MAX}$ = 10MHz at FS |
| Integral non-linearity | INL | 25 | 1 | | ±1 | ±2 | LSB | $A_{IN\ MAX}$ = 10MHz at FS |
| S/N ratio | SNR | 25 | 1 | 40.9 | 44.5 | | dBc | $A_{IN\ MAX}$ = 1MHz at FS |
| | | | 4 | | 44.1 | | dBc | $A_{IN\ MAX}$ = 5MHz at FS |
| | | | 4 | | 43.3 | | dBc | $A_{IN\ MAX}$ = 10MHz at FS |
| Effective No. of bits | ENOB | 25 | 1 | 6.5 | 7.1 | | bits | $A_{IN\ MAX}$ = 1MHz at FS |
| | | | 4 | | 7.0 | | bits | $A_{IN\ MAX}$ = 5MHz at FS |
| | | | 4 | | 6.9 | | bits | $A_{IN\ MAX}$ = 10MHz at FS |
| Bit Error Rate | BER | 25 | 4 | | 1 in $10^9$ | | | |

## ELECTRICAL CHARACTERISTICS DEFINITIONS

### Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis is 3dB down on the DC level.

### Aperture Delay
The delay between the falling edge of the CLOCK signal and the instant at which the analog input is sampled.

### Bit Error Rate (BER)
The number of spurious code errors produced for any given input sinewave frequency. In this case it is the number of codes occuring outside the histogram cusp for a ½ F.S. sinewave.

### Differential Non-Linearity (DNL)
The deviation of any code width from an ideal 1LSB step.

### Effective Number of Bits (ENOB)
This is a measure of the dynamic performance and is calculated from the following expression.

$$ENOB = \frac{SNR-1.76}{6.02}$$

SNR is the signal-to-noise ratio, in decibels, at the test frequency.

### Integral Non-Linearity (INL)
The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

### Output Data Delay
The delay between the 50% point of the falling edge of the clock signal and the 50% point of any data output change.

### Reference Ladder Offset
The voltage error at the ends of the resistor chain caused by the lead frame and bond wire.

### Signal-to-Noise Ratio (SNR)
The ratio of the RMS signal amplitude to the RMS value of 'noise' which is defined as the sum of all other spectral components including harmonics but excluding DC with a full scale analog input signal.

### Test Levels
**Level 1** - 100% production tested
**Level 2** - 100% production tested at 25°C and sample tested at specified temperatures
**Level 3** - Sample tested only
**Level 4** - Parameter is guaranteed by design and characteristics testing
**Level 5** - Parameter is a typical value only

## PIN DESCRIPTIONS

| Pin No. | Function | Description |
|---|---|---|
| 1, 2, 3, 4 | D3, D2, D1, D0 | Output data bits 3, 2, 1, 0 |
| 5 | CLK | Clock input pin |
| 6 | $\overline{CLK}$ | Clock threshold level pin |
| 7 | $V_{RB}$ | Bottom of reference resistor chain |
| 8 | $AV_{CC}$ | 5 Volt power to all circuitry except the TTL output |
| 9 | AGND | 5 Volt power to all circuitry except the TTL output |
| 10 | $V_{RM}$ | Middle of reference resistor chain |
| 11 | $V_{IN}$ | Analog input voltage pin |
| 12 | $V_{RT}$ | Top of reference resistor chain |
| 13 | $DV_{CC}$ | 5 Volt power supply to the TTL output stage |
| 14 | DGND | 5 Volt power supply to the TTL output stage |
| 15 | D7 | Most significant bit (output data bit 7) |
| 16, 17, 18 | D6, D5, D4 | Output data bits 6, 5, 4 |

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply Voltage $V_{CC}$ | +5.0V |
| Reference $V_{RT}$ | +4.3V |
| Reference $V_{RB}$ | +2.3V |
| $AV_{CC}$ to $DV_{CC}$ | 0mV |
| AGND to DGND | 0mv |
| Analog Input $V_{IN}$ | 2 Vp-p max |

## THERMAL CHARACTERISTICS

| | DG | DP | MP |
|---|---|---|---|
| Thermal resistance, chip-to-case $\theta_{jc}$ | 21 | 20 | 30 °C/W |
| Thermal resistance, chip-to-ambient $\theta_{jA}$ | 92 | 75 | 98 °C/W |

## APPLICATION NOTES

### Analog Input Pin (Fig 3.)

The analog input of the SP973T8 is connected to 256 comparators which have a combined capacitance of about 30pF. The sample/latch operation of the comparators causes the input capacitance to vary slightly as the comparator input transistors turn on/off. For this reason the input driver circuit should provide a low impedance signal to keep the harmonic distortion levels of the driver to a minimum.

The maximum amplitude of the analog input is defined by the setting of the two reference voltages $V_{RT}$ and $V_{RB}$. Optimum performance will be obtained with the input signal biased midway between $V_{RT}$ and $V_{RB}$ with a peak to peak amplitude of $V_{RT}$-$V_{RB}$. The SP973T8 has excellent overload tracking of input signals with amplitudes greater than $V_{RT}$-$V_{RB}$, and will not be damaged if the absolute maximum ratings are adhered to.

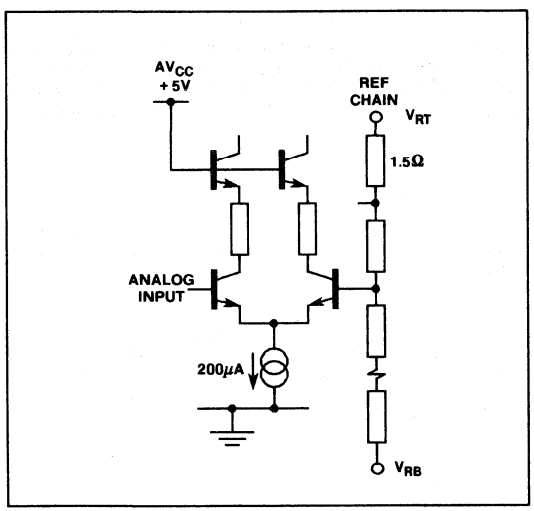



*Fig.3 One of 255 analog inputs connected to pin 11*

### Voltage Reference Pins (Fig 4.)

The SP973T8 converts analog signals in the range $V_{RB} < V_{IN} < V_{RT}$ into digital format, where $V_{RB}$ produces code 0 and $V_{RT}$ produces code 255. Between the pins $V_{RT}$ and $V_{RB}$ are a series of 256 resistors forming a reference chain with a total resistance of 425Ω (typically). The centre point of the reference chain is also connected to an external pin named $V_{RM}$ by which it is possible to provide precision trimming of the integral linearity of the device.

The maximum value of $V_{RT}$ is $V_{CC}$-0.7 volts since values above this figure will start to saturate the comparator, resulting in noticeable distortion. Optimum performance from a +5 Volt power supply is obtained with $V_{RT}$ < +4.3V and $V_{RB}$ a further 2 volts below $V_{RT}$. In addition the $V_{RT}$, $V_{RB}$ and $V_{RM}$ pins should be decoupled to ground close to the device pins using good quality 10nf capacitors. A simple method for providing the reference voltages is shown in Fig. 4, and further information may be found in applications note AN72 (page 4-74). With a reference ladder voltage of less than 2V the reduced LSB size causes a larger differential linearity error. Operation of the device below 1.5V may therefore cause missing codes.

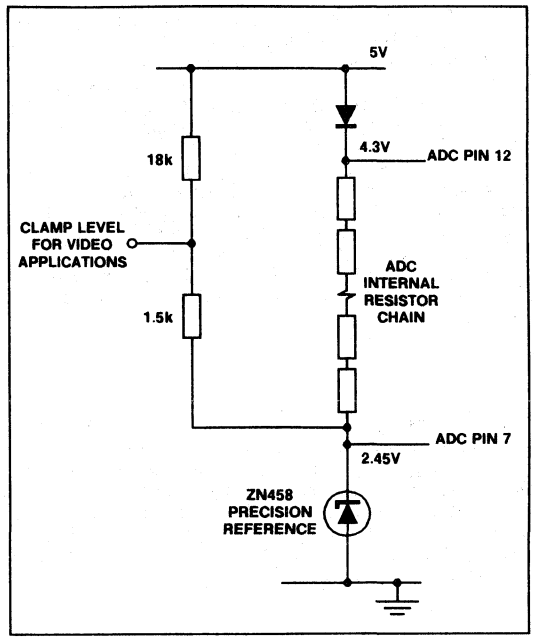



*Fig.4 Simple reference voltage generation*

### TTL/CMOS Outputs (Fig. 5)

The data output levels of the SP973T8 are TTL/CMOS compatible and switch from 0V to +4V. The output circuit is capable of operation at clock frequencies in excess of 60MHz when driving into a standard LSTTL load.

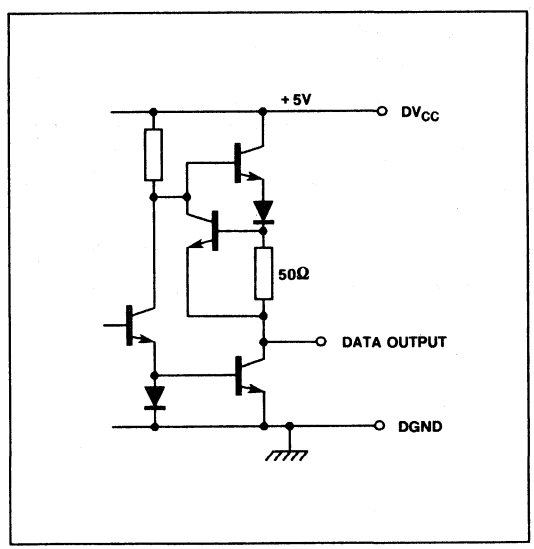



*Fig.5 TTL output stage*

## Clock Input (Fig. 6)

The SP973T8 will operate at clock frequencies up to and above 30MHz. The clock input has been designed to accept a 1Vpp signal, in either differential or single-ended mode, between the $V_{IH(MAX)}$ and $V_{IL(MIN)}$ levels indicated in the electrical specification. At $V_{IH(MAX)}$ or $V_{IL(MIN)}$ the $\overline{CLK}$ input will sink 800µA or source 3.2mA of current, respectively. (See Fig. 6)

When used in single-ended operation, $\overline{CLK}$ may be decoupled to ground so that this input will then self-bias at approximately 1.2V below the supply $V_{CC}$. It may then be used to bias the $\overline{CLK}$ input, through a termination resistor, for AC-coupled applications as shown in Fig. 8.

Alternatively a TTL level clock may be used by inserting an appropriate value resistor in series with the coupling capacitor.

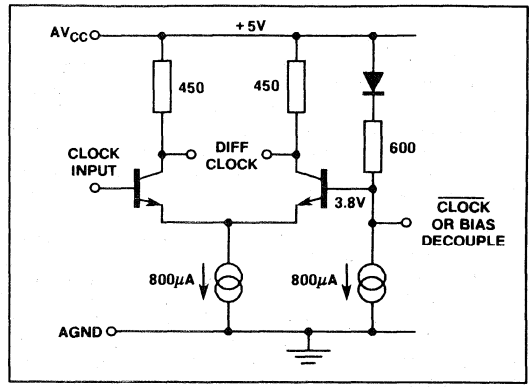



*Fig.6 Clock input stage*

## TIMING (Fig. 7)

The analog input is sampled by the SP973T8 approximately 3ns ($t_{AD}$) after the falling edge of the clock. Due to the pipelined operation of the device, a further one clock cycle is required to produce the output data. As shown in Fig. 7, the output has a good data valid time, enabling the data to be latched at both the rising and fallingedges of the clock.

However, for clock frequencies above 25MHz the clock-to-output delay time may lead to an inadequate data set up time relative to the rising clock edge and it is therefore recommended that the output data is latched on the falling clock edge.

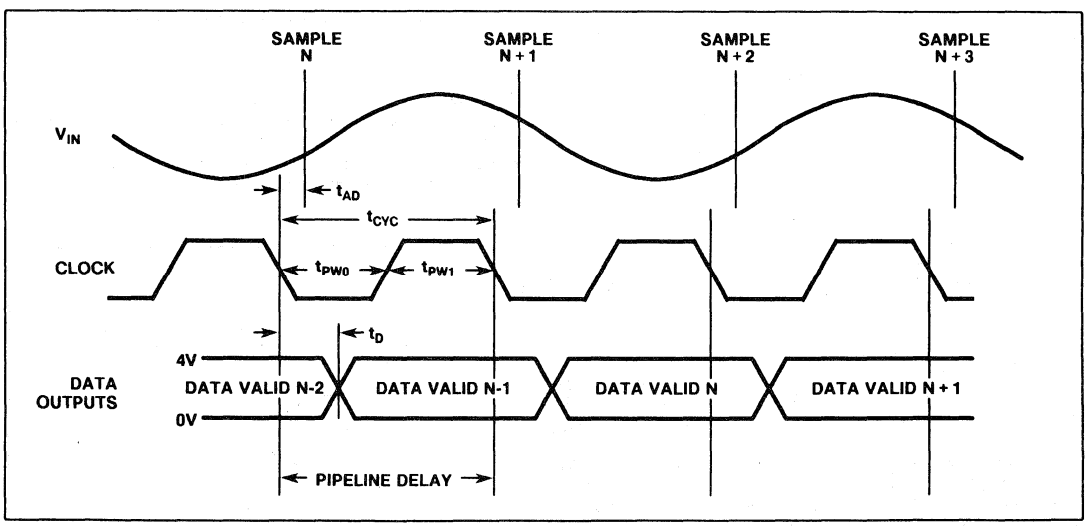



*Fig.7 Timing diagram*

## Circuit Board Construction (Fig. 8)

Excellent performance can be obtained from this ADC using only one solid ground plain for both analog and digital signals.

With all flash ADCs it is important to restrict digital crosstalk into the input, not only within the wanted signal bandwidth but also at frequencies between Nyquist and clock, as such signals will be aliased down into the wanted signal bandwidth.

We can give the designer two useful suggestions to reduce the above. First, due to the on-chip clock regeneration circuit, a low level clock can be fed to the ADC 1V p-p is recommended. The second suggestion is the addition of a small bead inductor in series with and close to the device analog input.

Supply line decoupling is very important when dealing with a mix of analog and digital signals as they can provide a source of digital feedback from the digital output currents. It is wise, therefore, to decouple the SP973T8 close to the device supply pins with good quality, high frequency, low inductance capacitors.

Due to the high clock rates involved, long clock lines to the device should be avoided to reduce the noise pick up.

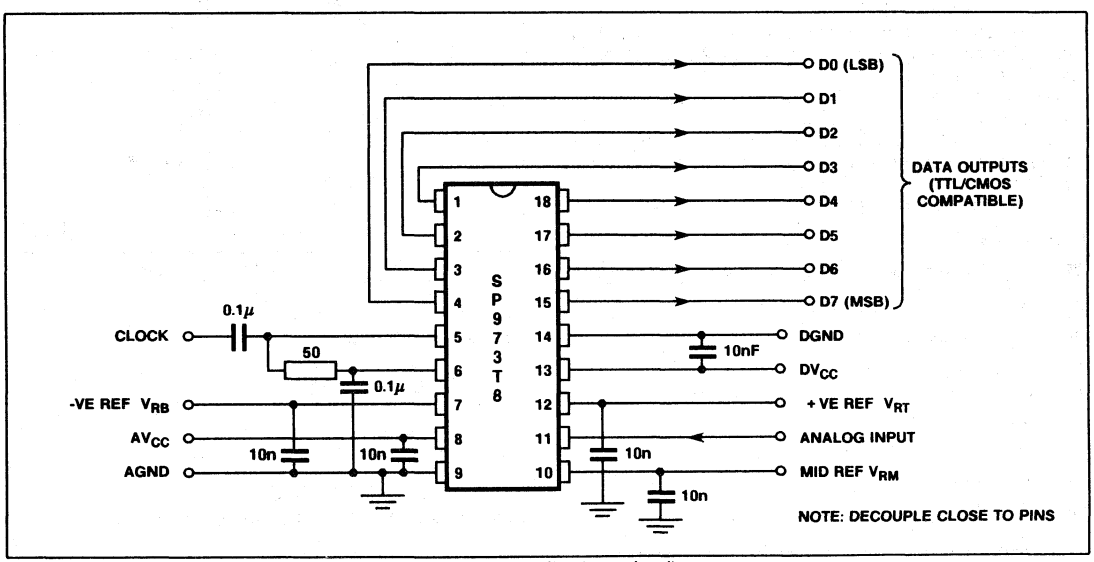



*Fig.8 Test/applications circuit*

# SP97504

## HIGH SPEED FOUR BIT EXPANDABLE A TO D CONVERTER

*(SUPERSEDES SP9754, DIRECT PIN REPLACEMENT)*

The SP97504 is a fast 4-bit ECL A-D converter, expandable up to 8 bits without additional encoding circuitry.

Designed to maintain high accuracy at high analog input frequencies, the SP97504 is a pin for pin replacement for the industry standard SP9754.

It can convert at sample rates from DC to 110MHz, with analog inputs above Nyquist frequencies. All output levels are ECL compatible.

The latch function to the device provides on-chip sampling which allows the converter to operate without an external sample and hold. Data is clocked through the device in master/slave fashion, ensuring that all outputs are synchronous.

The SP97504 operates from a +5V, -7V supply.

### FEATURES

- Operating Temperature Range -30°C to +85°C
- No External Components for 4-Bit Conversion
- 110MHz Conversion Rate
- On-Chip Encoding for Expansion to 8 Bits
- No External Sample and Hold Needed
- Bit Size 10-100mV
- Over 100MHz Full Power Bandwidth
- 10ps Aperture Uncertainty Time
- 8-Bit Accuracy (When Expanded)

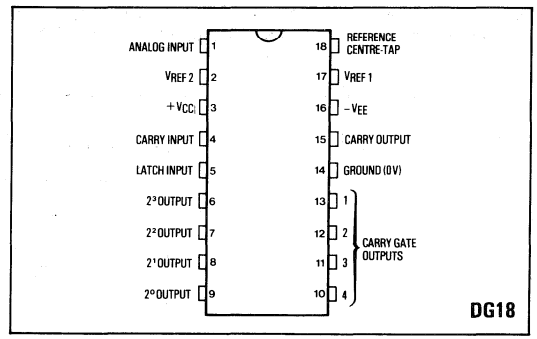



*Fig.1 Pin connections (top view)*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Positive supply voltage | +5.5V |
| Negative supply voltage | -7.5V |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |
| Lead temperature (soldering 60 sec) | 300°C |

### ORDERING INFORMATION

**SP97504 DG** (Industrial - Ceramic DIL package)

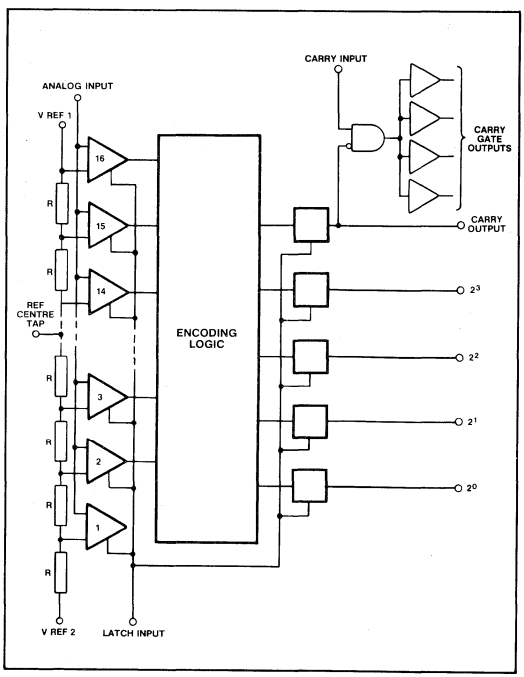



*Fig.2 Functional diagram*

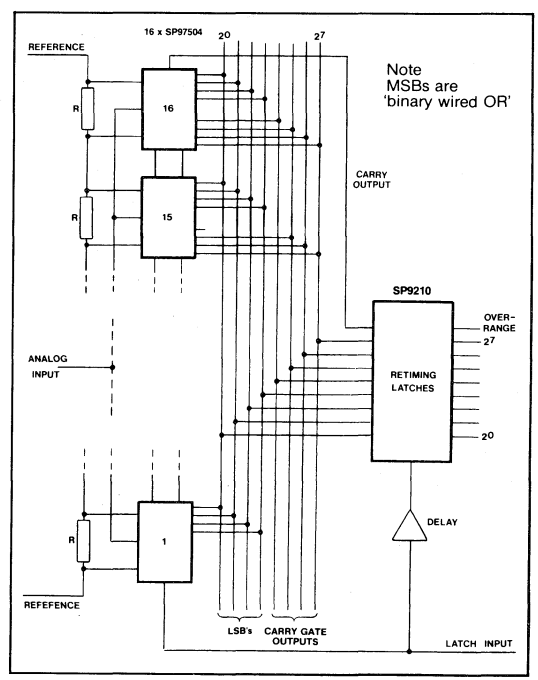



*Fig.3 8-bit all-parallel system*

## ELECTRICAL CHARACTERISTICS

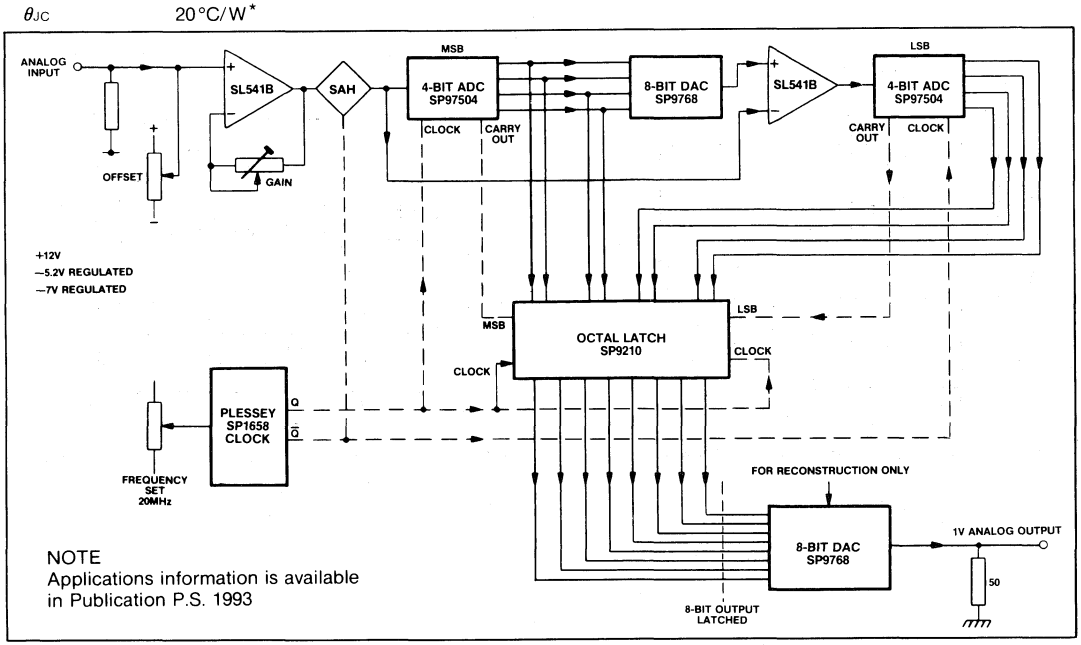
**Test conditions (unless otherwise stated):**
$T_{amb}$ = 25 °C, $V_{CC}$ = +5V ± 0.25V, $V_{EE}$ = -7V ± 0.25V, $R_L$ = 100Ω to -2V

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Analog input current | $I_B$ | | 30 | 100 | μA | $V_{IN}$ = 0V |
| Analog input capacitance | $C_{IN}$ | | 10 | | pF | |
| Common mode range | $V_{CM}$ | -2 | | +2 | V | |
| Maximum input slew rate | | | 1000 | | V/μs | |
| Latch input capacitance | $C_{IN}$ | | 2 | | pF | |
| Positive supply current | $I_{CC}$ | | 72* | 92* | mA | |
| Negative supply current | $I_{EE}$ | | 75* | 96* | mA | |
| Reference resistor chain | | | 25 | | Ω | Total |
| Reference bit size | | 10 | | 100 | mV | |
| Comparator offset voltage | $V_{OS}$ | | | -5 | mV | |
| Total power dissipation | $P_{DISS}$ | | 935* | 1230* | mW | All outputs loaded |
| Input and output logic levels | | | | | | |
| Logic high | $V_{OH}$ | -0.930 | | -0.720 | V | For 100Ω load |
| Logic low | $V_{OL}$ | -1.90 | | -1.620 | V | to -2V |
| Minimum latch set-up time | ts | | 1.5 | 2 | ns | 10mV overdrive |
| Data uncertain | | | 5 | | ns | <1mV overdrive |
| Latch to output propagation delay | | | | | | |
| Latch enable to output high | $t_{pd}$ + (E) | | 6* | 8 | ns | 10mV overdrive |
| Latch enable to output low | $t_{pd}$ - (E) | | 5 | 8 | ns | 10mV overdrive |
| Carry input to carry gate | $t_{pd}$ (C) | | 3 | 5 | ns | |
| O/P delay | | | | | | |
| Maximum sample rate | $F_{C\,max}$ | 100 | 110 | | MHz | |
| Aperture uncertainty time | ta | | 10 | | ps | |

* Values differ from SP9754

## THERMAL CHARACTERISTICS

| | |
|---|---|
| $\theta_{JA}$ | 90 °C/W* |
| $\theta_{JC}$ | 20 °C/W* |




NOTE
Applications information is available in Publication P.S. 1993

## PERFORMANCE CURVES

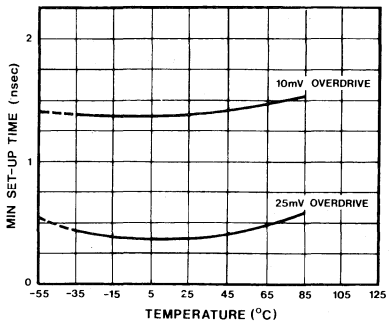



*Fig.5 Set-up time as a function of temperature*

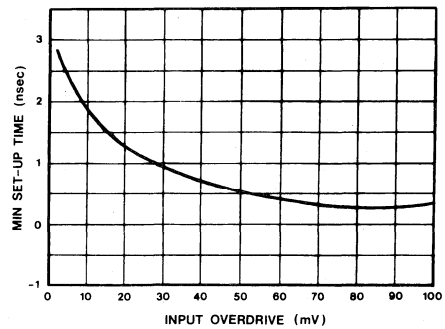



*Fig.6 Set-up time as a function of overdrive*

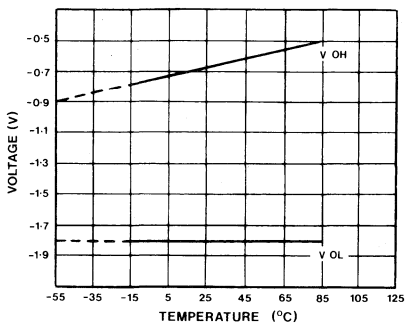



*Fig.7 Output logic levels as a function of temperature*

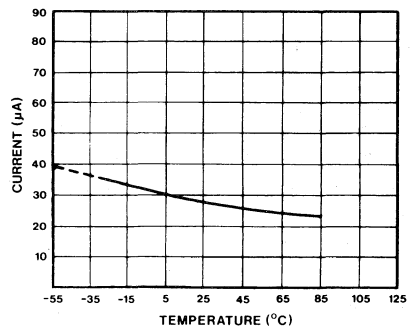



*Fig.8 Analog input current as a function of temperature*

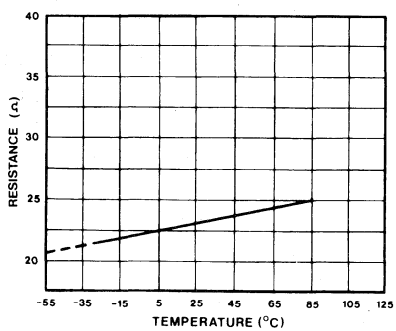



*Fig.9 Network resistance as a function of temperature*

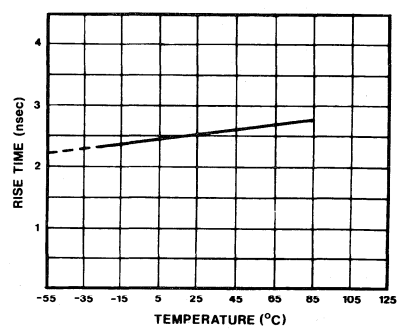



*Fig.10 MSB output edge speeds as a function of temperature*

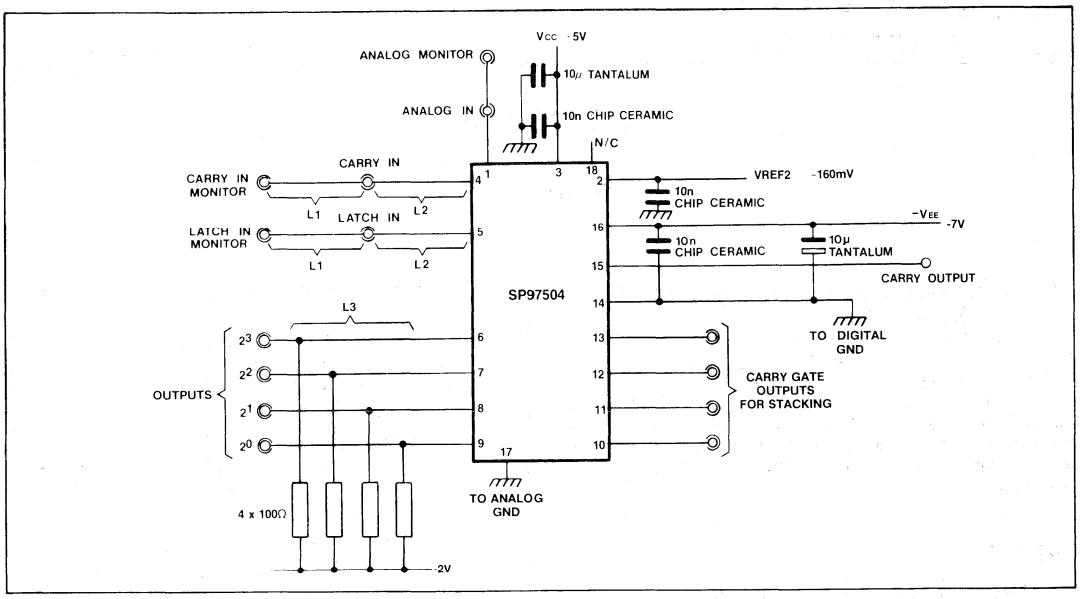



*Fig.11 High frequency test circuit*

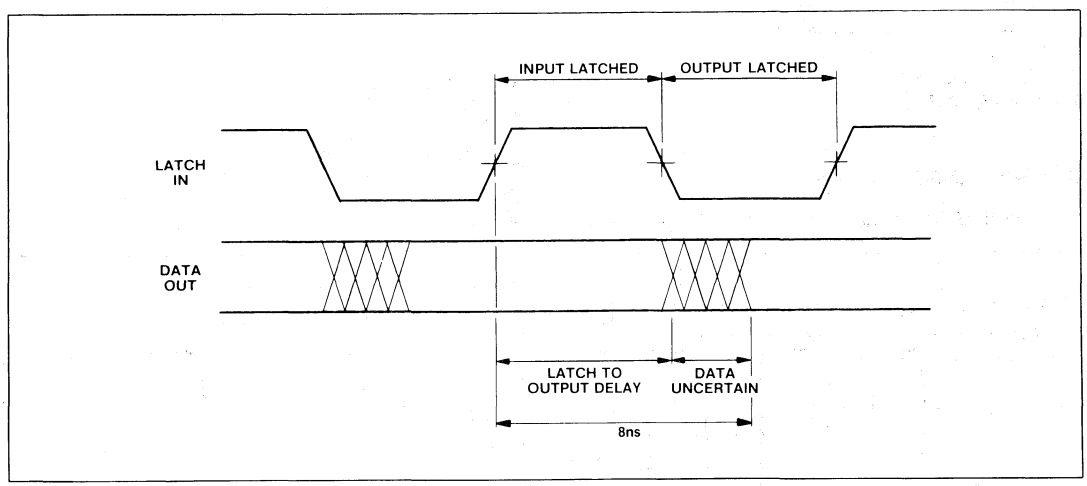



*Fig.12 Timing diagram*

## OPERATING NOTES

1. Carry output (pin 15) is high when the analog input exceeds the top reference voltage (pin 17).

Then the carry gate outputs (pins 10 to 13) go low regardless of carry input (pin 4), when the analog input is between $V_{REF}$ and $V_{REF2}$ and the carry output is low. The carry gate output will be high if the carry input is also high. Similarly if the carry input is low then the carry gate outputs will be low.

2. When used in an ambient temperature in excess of 65 °C the SP97504 must be provided with an external heatsink or forced air cooling. This will ensure that the junction temperature does not exceed 175 °C.

## APPLICATION NOTES

1. The SP97504 is ideally suited to subranging systems as it maintains good accuracy at low reference voltages. This enables the second rank to be driven at higher speed from the subtracting Op-Amp.
2. For applications that require low bit error rates at high frequency, the clock signal should be adjusted for 60% ECL low, 40% ECL high mark to space ratio.
3. The SP97504 is ideally suited to applications in communication systems that incorporate multi-level coding (quadrature amplitude modulation).
4. The SP97504 requires a fast edge speed clock. Rise and fall times of < 4ns are recommended.

# SP97506

## 110MHz 6-BIT FLASH ADC

The SP97506 is a 6-bit flash analog to digital converter that is pin compatible with the SP9756.

This device has improved speed combined with reduced bit error rate and therefore is ideally suited to critical applications such as video printers, nucleonics and instrumentation. As a direct replacement for the SP9756 the SP97506 provides reduced reference chain current with tap off points for non linear operation, internally biased mode input, higher sample rate and improved analog performance.

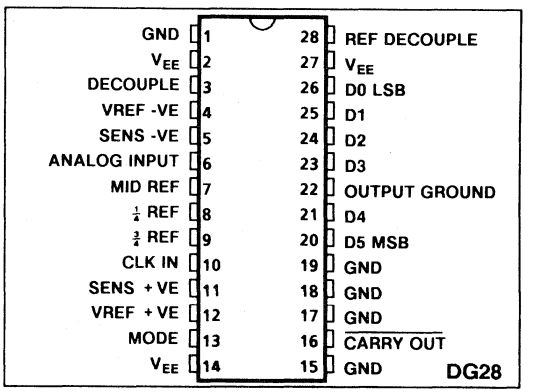



*Fig. 1 Pin Connections (top view)*

### FEATURES

- 110MHz Conversion Rate(typ. 150MHz)
- Monotonic
- SNR = 32dB at 50MHz Analog I/P Frequency
- Operating Temperature Range
  - 40°C to +85°C Industrial
- Bit Error Rate < 1 in $10^9$
- Single -5.2V Supply

### ORDERING INFORMATION

**SP97506 B DG** (Industrial - Ceramic DIL package)

### APPLICATIONS

- Instrumentation
- Nucleonics Research
- Video Printers
- Radar Video Digitising
- Medical Electronics

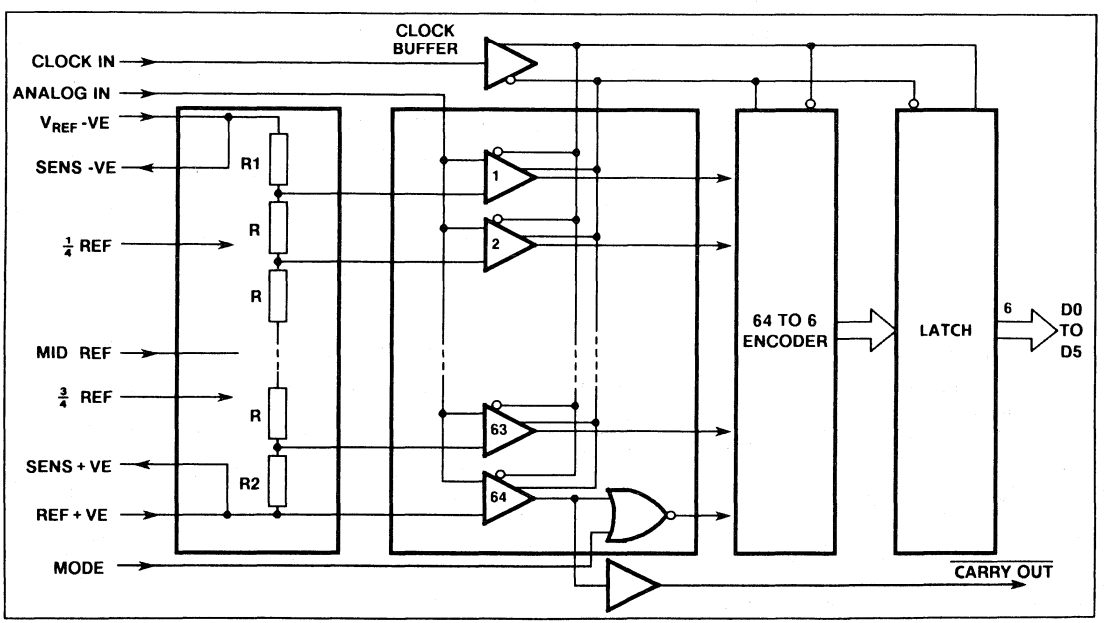



*Fig. 2 SP97506 functional block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = +25°C, $V_{EE}$ = -5.2V ±0.25V

### DC CHARACTERISTICS

| Characteristic | Symbol | Test level | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| **Power Supply** | | | | | | | |
| Supply current | $I_{EE}$ | 1 | -100 | -170 | -220 | mA | Excludes ECL O/P |
| Power dissipation | P | 1 | 520 | 884 | 1140 | mW | and ref. currents |
| **Analog Input** | | | | | | | |
| Input range | $V_{IN}$ | 4 | -2.2 | | 0 | V | |
| Input bias current | $I_{IN}$ | 1 | | | 2.2 | μA | |
| 3dB bandwidth | $f_{3dB}$ | 4 | | 250 | 700 | MHz | |
| Input capacitance | $C_{IN}$ | 4 | | 22 | | pF | |
| **Reference Ladder** | | | | | | | |
| Ladder resistance | $R_D$ | 1 | 60 | 80 | 100 | Ω | |
| Ladder voltage (top) | REF + VE | 4 | | 0 | | V | |
| Ladder voltage (bottom) | REF -VE | 4 | | -2 | | V | |
| Ladder temp. coeff. | $R_{TC}$ | 4 | | 0.33 | | %/°C | |
| Ladder voltage drop | | 4 | +0.5 | 2 | 2.2 | V | |
| **Clock Input** | | | | | | | |
| Logic '1' voltage | $V_{IH}$ | 4 | -1.0 | -0.8 | | V | |
| Logic '0' voltage | $V_{IL}$ | 4 | | -1.8 | -1.6 | V | |
| **Digital outputs** | | | | | | | |
| Logic '1' voltage | $V_{OH}$ | 4 | -1.0 | -0.8 | | V | |
| Logic '0' voltage | $V_{OL}$ | 4 | | -1.8 | -1.6 | V | |
| **Mode Input** | | | | | | | |
| Logic High | $V_{IH}$ | 4 | -50 | 0 | +100 | mV | |
| Logic Low | $V_{IL}$ | 4 | -3.5 | -2 | -0.5 | V | |
| **Static performance** | | | | | | | |
| Differential non-linearity | DNL | 1 | | ±0.2 | ±0.5 | LSB | |
| Integral non-linearity | INL | 1 | | | ±0.5 | LSB | |

### AC CHARACTERISTICS

| Characteristic | Symbol | Test level | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Clock min. high | $t_{HIGH}$ | 4 | 3 | | | ns | |
| Clock min. low | $t_{LOW}$ | 4 | 3 | | | ns | |
| Max. conversion rate | $f_{MAX}$ | 4 | 110 | 150 | | MHz | |
| Aperture delay | $t_{AD}$ | 5 | | 1.2 | | ns | |
| Output data delay | $t_D$ | 4 | 1.5 | 3.5 | 5 | ns | |
| Output rise time | $t_R$ | 4 | | 1.5 | | ns | |
| Output fall time | $t_F$ | 4 | | 1.5 | | ns | |
| Data valid time | $t_{DATA}$ | 4 | 3.6 | | | ns | |
| Clock to carry delay | $t_C$ | 4 | | 2 | | ns | |
| **Dynamic Performance** | | | | | | | |
| Differential non-linearity | DNL | 4 | | | ±0.5 | LSB | |
| Integral non-linearity | INL | 4 | | | ±0.75 | LSB | |
| S/N ratio | SNR | 4 | 32 | | | dB | $f_{CLK}$ = 150MHz, $f_{AIN}$ = 50MHz |
| Effective No. of bits | ENOB | 4 | 5 | | | bits | |
| Bit Error Rate | BER | 5 | | 1 in $10^9$ | | | $f_{CLK}$ = 125MHz, $f_{AIN}$ = 62.4MHz |

## ELECTRICAL CHARACTERISTICS DEFINITIONS

### Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis is 3dB down on the DC level.

### Aperture Delay
The delay between the falling edge of the CLOCK signal and the instant at which the analog input is sampled.

### Bit Error Rate (BER)
The number of spurious code errors produced for any given input sinewave frequency. In this case it is the number of codes occuring outside the histogram cusp for a ¼ F.S. sinewave.

### Differential Non-Linearity (DNL)
The deviation of any code width from an ideal 1LSB step.

### Effective Number of Bits (ENOB)
This is a measure of the dynamic performance and is calculated from the following expression.

$$\text{ENOB} = \frac{\text{SNR-1.76}}{6.02}$$

SNR is the signal-to-noise ratio, in decibels, at the test frequency.

### Integral Non-Linearity (INL)
The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

### Output Data Delay
The delay between the 50% point of the rising edge of the clock signal and the 50% point of any data output change.

### Reference Ladder Offset
The voltage error at the ends of the resistor chain caused by the lead frame and bond wire.

### Signal-to-Noise Ratio (SNR)
The ratio of the RMS signal amplitude to the RMS value of 'noise' which is defined as the sum of all other spectral components including harmonics but excluding DC with a full scale analog input signal.

### Test Levels
**Level 1** - 100% production tested
**Level 2** - 100% production tested at 25°C and sample tested at specified temperatures
**Level 3** - Sample tested only
**Level 4** - Parameter is guaranteed by design and characteristics testing
**Level 5** - Parameter is a typical value only

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Clock and Mode input | 0V to -3.5V |
| Supply voltage | -7V |
| Maximum junction temperature | 175°C |
| Storage temperature range | -65°C to +150°C |

## THERMAL CHARACTERISTICS

| | |
|---|---|
| Thermal resistance, chip-to-case $\theta_{JC}$ | 40 °C/W (typ) |
| Thermal resistance, chip-to-ambient $\theta_{JA}$ | 15 °C/W (typ) |
| $T_{AMB}$ (still air) | -40°C to +70°C |
| $T_{AMB}$ (in 500LFPM of air across package) | -55°C to +125°C |
| Pins I7, 18, I9 (continuous operation) | 25mA |

## OPERATING NOTES

### Analog Input

The Input voltage range is 0.0v to -2.2V. Optimum performance is achieved with an input of 2V p-p i.e. DC offset to -1.0V for symmetrical limiting. At temperatures below -30°C this input range may degrade to 1.8V p-p.

The input capacitance is of the order of 22pF therefore the source impedance should be low. The device is specified using an input drive from a 50Ω generator into a 50Ω termination resistor, i.e. 25Ω looking out of the device.

### Reference Voltage

The REF +VE (pin 12) should be connected to 0V (analog GND) and the REF-VE (pin 4) to a voltage between -0.5V and -2.0V.

Operation with -0.5V reference will minimise power consumption in the reference resistor and maximise the device sensitivity but at the cost of reduced differential linearity. Operation with -0.5V reference will also ease signal input power drive requirements and maximise the full power signal bandwidth.

Operation with -2.0V reference will maximise differential linearity accuracy and will also enable the device to be operated with non linear characteristic by applying additional bias levels to the $\frac{1}{4}$ REF, $\frac{3}{4}$ REF and mid-reference taps. This will enable an increase in system dynamic range to the equivalent of 8 bits resolution.

### MODE Input

The MODE input (pin 13) selects the output code when $V_{IN}$ is higher than REF +VE. For normal operation this pin should be open circuit. The SP97506 will then give an all ones output for any input greater than REF + VE. If the mode input is tied to GND the device will give all zeros when the input is higher than REF + VE.

### CLK Input

As the SP97506 features an internal differential clock driver, a single ended ECL clock signal is suitable.

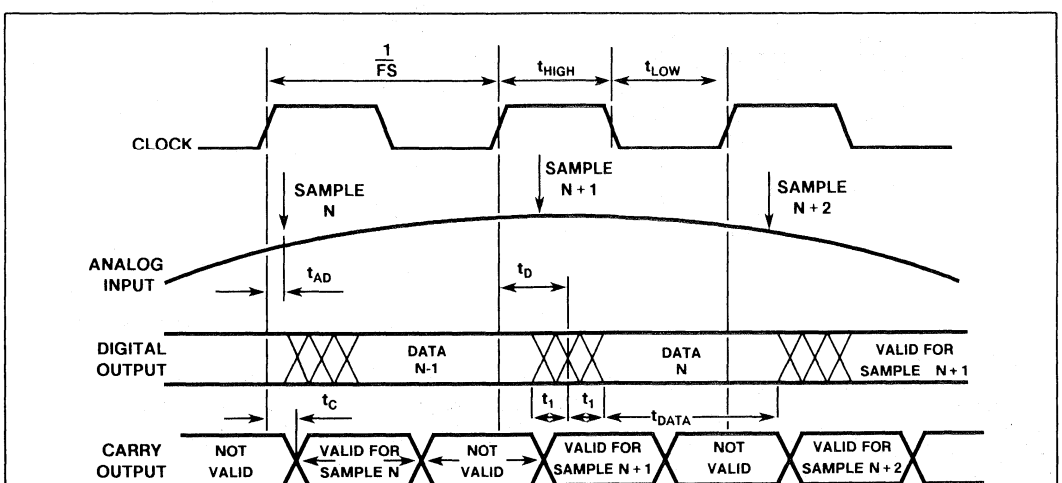
The aperture uncertainty of the device is in the order of 25ps, therefore the clock signal should have low edge jitter to be compatible.

### Clock Timing (See Fig. 3)

The first sample of the analog input is taken approximately 1.2ns after the rising edge of the clock. The input comparators then latch, holding their state until the falling edge.

When the SP97506 receives the first falling edge the device commences decoding and the input comparators are released. The binary data becomes available at the outputs 3.5ns after the second rising edge of the clock.

The SP97506 incorporates an output D-type latch. The data out from this latch is valid for over 70% of the clock cycle at 100MHz. This greatly simplifies data acquisition of the binary information, because timing is not so critical as with many other ADCs.




**NOTES**

1. Data appears at the O/P after one clock cycle delay.
2. The carry output is valid one clock cycle before the relevant data output.

*Fig. 3 Timing Diagram*

## CIRCUIT BOARD LAYOUT

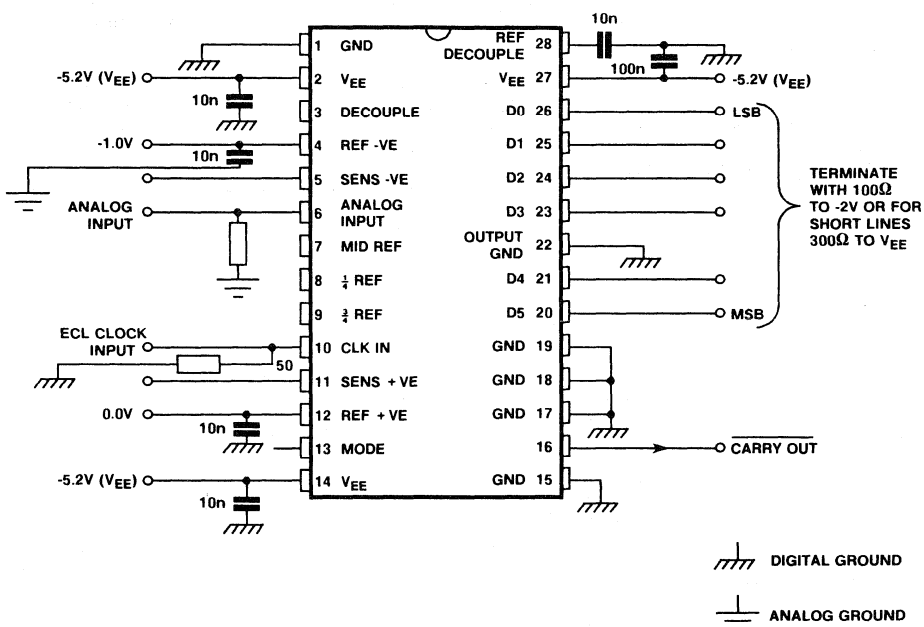
As with most PCB layouts for analog-to-digital conversion, the best performance from the SP97506 can be achieved by separating the ground plane into two sections, analog GND, and digital GND. This aids the device performance by reducing the amount of digital switching noise fed back into the analog section of the converter.

The digital noise is produced mainly by the ECL binary outputs, which ideally should be terminated through a 100Ω load to a -2V supply.

The device supplies are also a source of digital feedback, as they can be modulated by the digital output current. Therefore it is wise to decouple the SP97506 close to the device supply pins with good quality, high frequency capacitors. It is also advisable to direct the current returned from the output load towards pin 22 and away from other digital grounds. One way of achieving this is by creating a second digital ground plane which should connect to the main digital ground at pin 22 of the device, the ground connection between the ADC and the device acquiring the data is then made to this second ground plane.

The following should be referred to the digital GND: $V_{EE}$, REF decouple (pin 28), -2V supply for output termination, clock termination, device GND, pins 1, 15 and 22.

The following should be referred to the analog GND: REF +VE, REF -VE, input termination or buffer.




### NOTES ON APPLICATION

1. MODE drives output either 'all zeros' or 'all ones' on over - range.
2. Kelvin connections can be made to the referenced chain via SENS (+VE) and SENS (-VE).
3. O/C leave open circuit.
4. REF DECOUPLE (Pin 28) gives access to DC bias reference for logic. This gives the ability to eliminate possible crosstalk by allowing capacitor to remove edge noise.
5. Keep OUTPUT GROUND separate from GROUND.

*Fig. 4 Test and Application Circuit*

# SP97508

## 110MHz 8-BIT FLASH ADC

The SP97508 is an 8-bit flash ECL analog-to-digital converter. It incorporates 256 individual comparators, a reference chain and a full D-type output latch. The ADC is capable of sampling at 100MHz with full (Nyquist) analog bandwidth and has an excellent dynamic performance. A conventional unity mark/space ratio clock can be used and the output data can be programmed for true or inverse binary and twos' complement coding.

### FEATURES

- Pin Replacement for CX20116, ADC303, HADC77100 (DIL Package Only)
- Full Scale Input Bandwidth 120MHz (3dB)
- No Missing Codes
- Production Tested with 30MHz Analog Input
- Low Input Capacitance: 32pF (Max.)
- No External Sample and Hold Needed
- Low Power Consumption: 1.4W (Typ.)
- True/Inverse Binary and Twos' Complement Coding
- Operating Temperature Range: -40°C to +85°C

### APPLICATIONS

- Radar Video Digitising
- Instrumentation
- Nucleonics
- Studio Quality Video

### ORDERING INFORMATION

**SP97508B DC** (Industrial - Sidebrazed Ceramic DIL)
**SP97508BB DC** (Hi-Rel - Sidebrazed Ceramic DIL)
**SP97508B DG** (Industrial - Ceramic DIL)
**SP97508B HG** (Industrial - J-Lead Quad Cerpac)

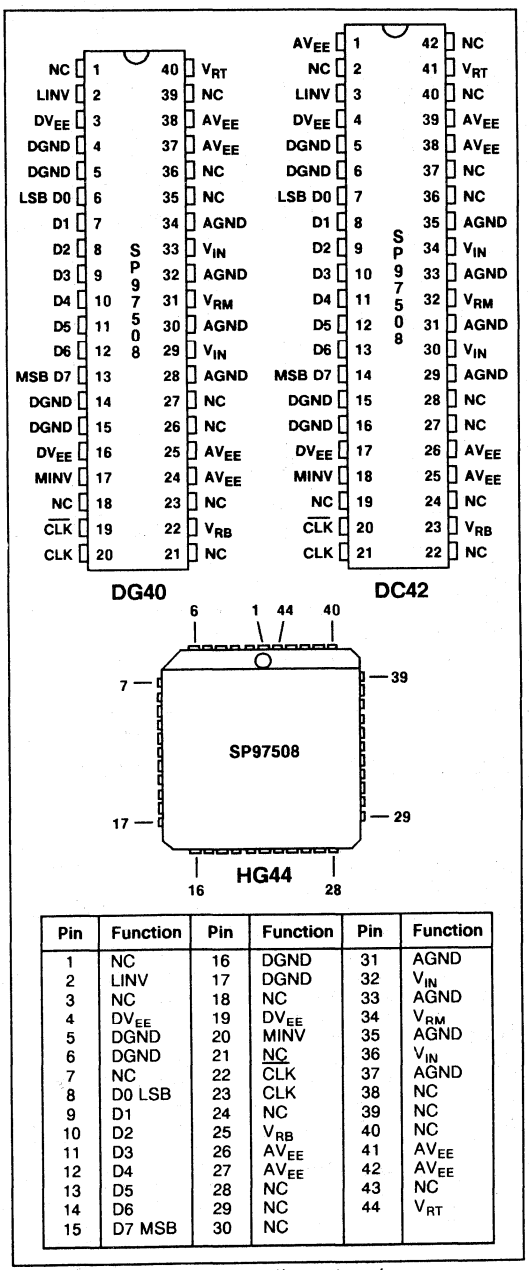
**Under Development:**
**SP97508AC DC** (Military - Sidebrazed Ceramic DIL)
**SP97508AC DG** (Military - Ceramic DIL)
**SP97508AC HG** (Military - J-Lead Quad Cerpac)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply $V_{EE}$ | 0V to -7V |
| Analog input $V_{IN}$ | +0.5V to $V_{EE}$ |
| Reference voltages $V_{RT}$, $V_{RM}$, $V_{RB}$ | +0.5V to $V_{EE}$ |
| Reference range $V_{RT} - V_{RB}$ | 2.5V |
| Digital inputs CLK, $\overline{CLK}$, MINV, LINV | +0.5V to -4V |
| MidRef input current $I_{VRM}$ | -10mA to +10mA |
| Digital output current $I_D$ | 0 to -20mA |
| Voltage between AGND and DGND | -50mV to +50mV |
| Voltage between $AV_{EE}$ and $DV_{EE}$ | -50mV to +50mV |

### THERMAL CHARACTERISTICS

| | | |
|---|---|---|
| Storage temperature range | | -65°C to +150°C |
| Max. junction operating temperature | | +175°C |
| Lead temperature (soldering 60s) | | 300°C |
| **SP97508B/BB DC** | $\theta_{JA}$ | 40°C/W |
| | $\theta_{JC}$ | 10°C/W |
| **SP97508B DG** | $\theta_{JA}$ | 42°C/W |
| | $\theta_{JC}$ | 10°C/W |
| **SP97508B HG** | $\theta_{JA}$ | 46°C/W |
| | $\theta_{JC}$ | 11°C/W |




| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | NC | 16 | DGND | 31 | AGND |
| 2 | LINV | 17 | DGND | 32 | $V_{IN}$ |
| 3 | NC | 18 | NC | 33 | AGND |
| 4 | $DV_{EE}$ | 19 | $DV_{EE}$ | 34 | $V_{RM}$ |
| 5 | DGND | 20 | MINV | 35 | AGND |
| 6 | DGND | 21 | NC | 36 | $V_{IN}$ |
| 7 | NC | 22 | CLK | 37 | AGND |
| 8 | D0 LSB | 23 | CLK | 38 | NC |
| 9 | D1 | 24 | NC | 39 | NC |
| 10 | D2 | 25 | $V_{RB}$ | 40 | NC |
| 11 | D3 | 26 | $AV_{EE}$ | 41 | $AV_{EE}$ |
| 12 | D4 | 27 | $AV_{EE}$ | 42 | $AV_{EE}$ |
| 13 | D5 | 28 | NC | 43 | NC |
| 14 | D6 | 29 | NC | 44 | $V_{RT}$ |
| 15 | D7 MSB | 30 | NC | | |

*Fig.1 Pin connections - top view*

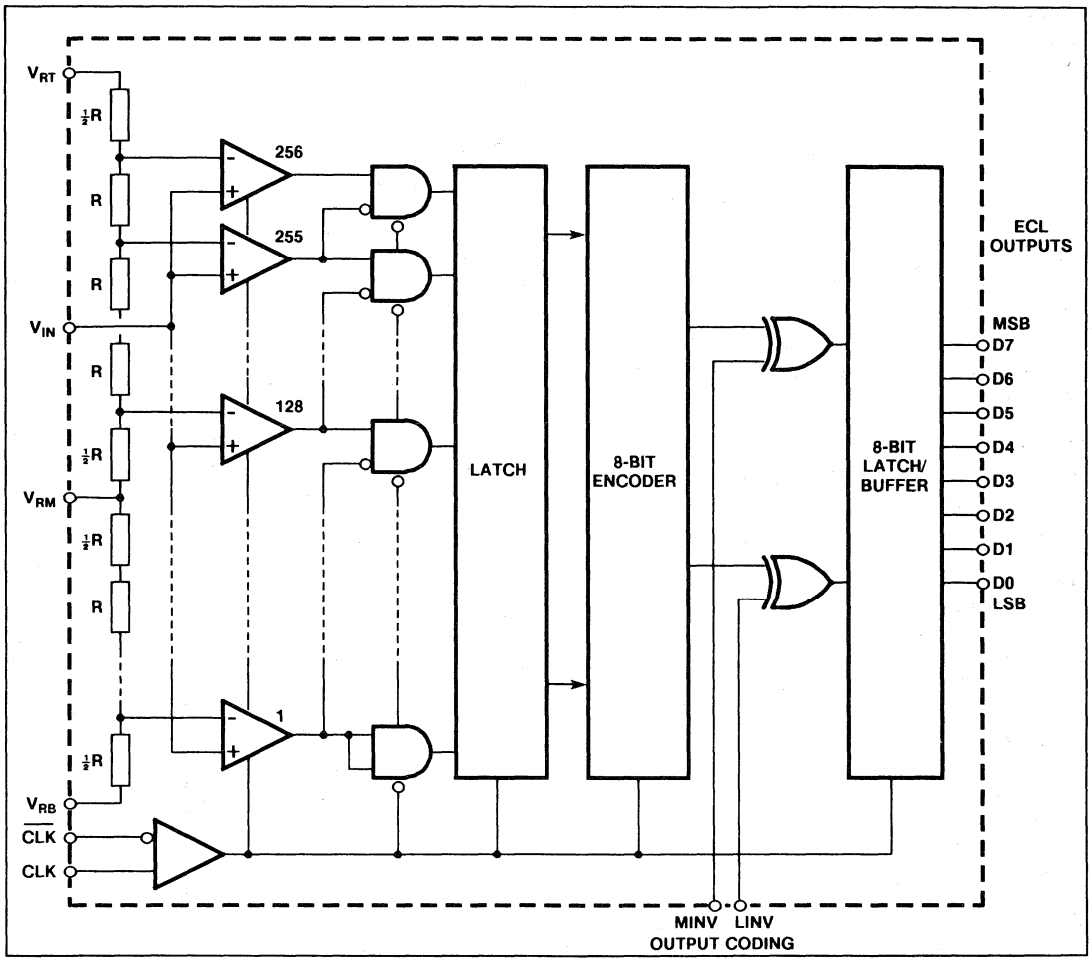



*Fig.2 SP97508 functional block diagram*

**PIN DESCRIPTIONS** (Pin numbers refer to DG40 package only)

| Pin name | Function |
|---|---|
| $AV_{EE}$ | Analog $V_{EE}$, –5.2V (typ.). |
| LINV | Input pin for polarity inversion of output data bits D0 to D6 (seeTable 1). |
| $DV_{EE}$ | Digital $V_{EE}$, –5.2V (typ.). |
| DGND | Digital ground, separated from the analog ground (AGND). |
| $D_0$-$D_7$ | Data output pins, ECL levels. D7 = MSB, D0 = LSB. External pulldown resistors are required ,e.g. 680Ω to DVEE. |
| MINV | Input pin for polarity inversion of D7 (MSB) (see Table1). ECL '0' level is held when MINV is open circuit. |
| CLK | Clock input pin, ECL levels. Analog input signal, $V_{IN}$, acquired on rising edge (see Fig.8). |
| $\overline{CLK}$ | Inverse clock input pin, ECL levels. |
| $V_{RB}$ | Reference voltage (bottom), –2V (typ.). |
| AGND | Analog ground. |
| $V_{IN}$ | Analog input, range ($V_{RT}$ – $V_{RB}$) p-p. |
| $V_{RM}$ | Midpoint of the reference voltage; can be used for linearity adjustment. |
| $V_{RT}$ | Reference voltage (top), 0V (typ.). |
| NC | Not Connected. Pins 1 and 18 should be connected to DGND, all others to AGND. |

**RECOMMENDED OPERATING CONDITIONS**

| | | | |
|---|---|---|---|
| Supply voltage | –5.2V ± 0.25V | AGND to DGND | 0mV ± 50mV |
| Reference ($V_{RT}$) | 0V ± 0.1V | Analog input | 2V p-p max. |
| Reference ($V_{RB}$) | –2.0V ± 0.2V | Output load | 680Ω to –5.2V |
| $AV_{EE}$ to $DV_{EE}$ | 0mV ± 50mV | | |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = 25°C, $V_{EE}$ = -5.2V, $V_{RT}$ = 0V. $V_{RB}$ = -2V, full temperature range = -40°C to +85°C

| Characteristic | Symbol | Temp (°C) | Test level | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| **Power Supply** | | | | | | | | |
| Supply current | $I_{EE}$ | 25 | 1 | 180 | 270 | 300 | mA | |
| | | Full | 4 | 165 | | 310 | mA | |
| **Analog Input** | | | | | | | | |
| Input bias current | $I_{IN}$ | 25 | 1 | 80 | 150 | 285 | µA | |
| | | Full | 4 | 50 | | 350 | µA | |
| Input bandwidth (3dB) | | 25 | 4 | | 120 | | MHz | |
| Input capacitance | $C_{IN}$ | 25 | 4 | | 29 | 32 | pF | $V_{IN}$ = 0V |
| Input resistance | $R_{IN}$ | 25 | 4 | | 75 | | kΩ | $V_{IN}$ = 0V |
| **Reference Chain** | | | | | | | | |
| Ladder resistance | $R_R$ | 25 | 1 | 90 | 105 | 135 | Ω | |
| | | Full | 4 | 70 | | 155 | Ω | |
| Ladder offset (top & bottom) | $V_{RT/B}$ | 25 | 3 | | 7.5 | | mV | |
| **Clock Input** | | | | | | | | I/P voltage swing = 1Vp-p |
| Logic '1' voltage | $V_{IH}$ | 25 | 4 | -3.05 | | DGND | V | |
| Logic '0' voltage | $V_{IL}$ | 25 | 4 | -3.85 | | -0.8 | V | |
| Logic '1' current | $I_{IH}$ | 25 | 1 | | | 380 | µA | $V_{IH}$ = -0.8V |
| | | Full | 4 | 310 | 360 | 390 | µA | $V_{IH}$ = -0.8V |
| Logic '0' current | $I_{IL}$ | 25 | 4 | | | 280 | µA | $V_{IL}$ = -1.8V |
| | | Full | 4 | 220 | 260 | 290 | µA | $V_{IL}$ = -1.8V |
| Min. pulse width (high) | | 25 | 4 | | 3 | | ns | |
| Min. pulse width (low) | | 25 | 4 | | 2.3 | | ns | |
| **Digital Outputs** | | | | | | | | |
| Logic '1' voltage | $V_{OH}$ | 25 | 1 | -0.90 | -0.83 | | V | $R_L$ = 680Ω to $DV_{EE}$ |
| | | Full | 4 | -1.00 | | | V | |
| Logic '0' voltage | $V_{OL}$ | 25 | 4 | | -1.80 | -1.90 | V | $R_L$ = 680Ω to $DV_{EE}$ |
| | | Full | 4 | | | -1.65 | V | |
| **Switching Performance** | | | | | | | | |
| Max. conversion rate | $f_C$ | 25 | 4 | 110 | | | MHz | $f_{IN}$ = 50MHz at FS |
| Aperture delay | $t_{ad}$ | 25 | 5 | | 1.9 | | ns | |
| Aperture uncertainty | $t_{au}$ | 25 | 4 | | 30 | | ps rms | |
| Output data delay | $t_d$ | 25 | 4 | | 2.9 | | ns | $R_L$ = 680Ω to $DV_{EE}$ |
| Output data rise time | $t_r$ | 25 | 4 | | 2.0 | | ns | $R_L$ = 680Ω to $DV_{EE}$ |
| Output data fall time | $t_f$ | 25 | 4 | | 1.6 | | ns | $R_L$ = 680Ω to $DV_{EE}$ |
| Output data time skew | $t_s$ | 25 | 4 | | 0.4 | | ns | $R_L$ = 680Ω to $DV_{EE}$ |
| **Static Performance** | | | | | | | | $f_C$ = 4MHz, $f_{IN}$ = 1kHz ramp |
| Differential non-linearity | DNL | 25 | 1 | -0.85 | ±0.5 | 0.85 | LSB | No missing codes |
| | | Full | 4 | -1.0 | | 1.0 | LSB | No missing codes |
| Integral non-linearity | INL | 25 | 1 | -1.4 | | 1.3 | LSB | |
| | | Full | 4 | -1.8 | | 1.6 | LSB | |
| Missing codes | | 25 | 1 | No missing codes | | | | Guaranteed |
| Gain error | | 25 | 1 | -1.5 | | 1.5 | %FS | |
| Offset error | | 25 | 1 | -15 | | 0 | mV | |
| **Dynamic Performance** | | | | | | | | $f_C$ = 100MHz |
| Transient response (rise) | | 25 | 4 | | 2.4 | | ns | $f_{IN}$ = 50MHz |
| Transient response (fall) | | 25 | 4 | | 2.1 | | ns | square wave at FS |
| Slew rate | | | 4 | | 1.0 | | V/ns | |
| Differential non-linearity | DNL | 25 | 1 | -0.9 | | 1.4 | LSB | $f_{IN}$ = 30MHz |
| Integral non-linearity | INL | 25 | 1 | -3.0 | | 3.0 | LSB | sinewave at FS |
| Signal-to-noise ratio | SNR | 25 | 4 | | 45.8 | | dB | $f_{IN}$ = 1MHz at FS |
| | | 25 | 1 | 41 | 44.5 | | dB | $f_{IN}$ = 10MHz at FS |
| | | 25 | 4 | | 39.0 | | dB | $f_{IN}$ = 30MHz at FS |
| Total harmonic distortion | THD | 25 | 4 | | 53.5 | | dBc | $f_{IN}$ = 1MHz at FS |
| | | 25 | 1 | 46 | 48.5 | | dBc | $f_{IN}$ = 10MHz at FS |
| | | 25 | 4 | | 40.4 | | dBc | $f_{IN}$ = 30MHz at FS |
| Effective number of bits | ENOB | 25 | 4 | | 7.3 | | bits | $f_{IN}$ = 1MHz at FS |
| | | 25 | 1 | 6.5 | 7.1 | | bits | $f_{IN}$ = 10MHz at FS |
| | | 25 | 4 | | 6.2 | | bits | $f_{IN}$ = 30MHz at FS |
| Bit error rate | BER | 25 | 4 | | 1 in $10^9$ | | | $f_{IN}$ = 50MHz at $\frac{3}{4}$FS |

## ELECTRICAL CHARACTERISTICS DEFINITIONS

**Analog Bandwidth**

The analog input frequency at which the spectral power of the fundamental frequency, as determined by Fast Fourier Transform analysis is 3dB down on the DC level.

**Aperture Delay**

The delay between the rising edge of the CLOCK signal and the instant at which the analog input is sampled.

**Aperture Jitter**

The sample- to- sample variation in aperture delay.

**Bit Error Rate (BER)**

The number of spurious code errors produced for any given input sinewave frequency at a given clock frequency. In this case it is the number of codes occuring outside the histogram cusp for a $\frac{3}{4}$ FS sinewave.

**Differential Non-Linearity (DNL)**

The deviation of any code width from ideal 1LSB step.

**Effective Number of Bits (ENOB)**

This is a measure of a device's dynamic performance and may be obtained from the SNR or from a sine wave curve fit test, according to the following expressions:

$$\text{ENOB} = \frac{\text{SNR}-1.76}{6.02} \quad \text{or} \quad \text{ENOB} = \text{N}-\text{Log}_2 \frac{\text{rms error (actual)}}{\text{rms error (ideal)}}$$

where N is the conversion resolution and the rms error is the deviation of the output from an input sine wave.

**Integral Non-Linearity (INL)**

The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

**Output Delay**

The delay between the 50% point of the rising edge of the clock signal and the 50% point of any data output change.

**Reference Ladder Offset**

The voltage error at the ends of the resistor chain caused by the end terminations, the lead frame and the bond wire.

**Signal-to-Noise Ratio (SNR)**

The ratio of the rms signal amplitude to the rms value of 'noise' which is defined as the sum of all other spectral components, including harmonics but excluding DC with a full scale analog input signal.

**Total Harmonic Distortion (THD)**

The RMS value of all the harmonics compared with the RMS value of the fundamental.

**Transient Response**

The time required by the outputs to move from 10(90)% to 90(10)% of the full scale range.

**Test Levels**

**Level 1** - 100% production tested at 25°C

**Level 2** - 100% production tested at 25°C and sample tested at specified temperatures

**Level 3** - Sample tested only

**Level 4** - Parameter is guaranteed by characterisation or design

**Level 5** - Parameter is a typical value only

## APPLICATION NOTES

**Analog Input (Figs. 3, 4 and 5)**

The maximum amplitude and offset of the input is defined by the reference voltages ($V_{RB}$ to $V_{RT}$). The optimum input is 2V p-p with a DC offset of -1V. The analog input circuit of the SP97508 consists of 256 buffered comparator inputs, as shown in Fig. 3.

The internal buffering to the device results in the typical input characteristics of Figs. 4 and 5. The dependence of input capacitance on voltage level is typical of flash converters and so requires that the analog input is driven from a low impedance source such as the SL9999.

Failure to drive the input capacitance properly causes increased levels of harmonic distortion, most noticeable in the second harmonic.

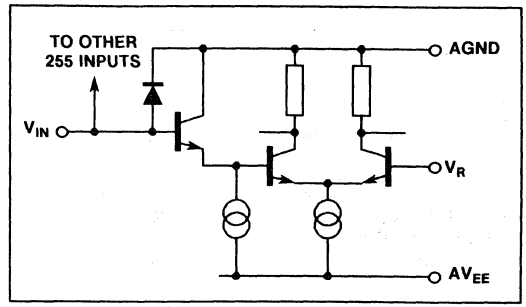



*Fig.3 Analog input*

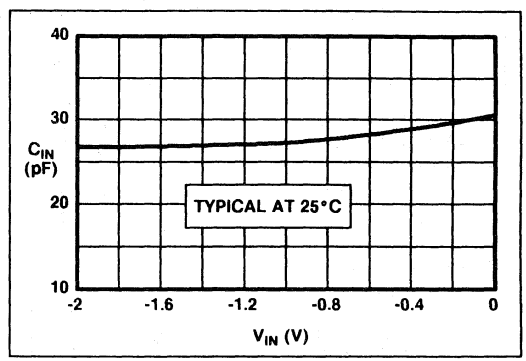



*Fig.4 Analog input capacitance*

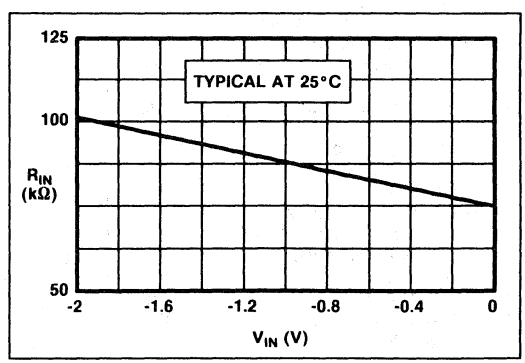



*Fig.5 Analog input resistance (AC)*

**Reference Pins (Fig. 6)**

Between $V_{RT}$ and $V_{RB}$ there are 256 series resistors forming the reference chain. The total resistance may be between 90Ω and 120Ω. A mid-reference pin ($V_{RM}$) is also provided as an option for precision setting of integral linearity. Both $V_{RM}$ and $V_{RB}$ should be adequately decoupled to analog ground. For optimum performance, $V_{RT}$ is connected directly to analog ground and $V_{RB}$ is driven from a -2V DC supply. For precise reference setting, this supply should be adjustable by ± 0.2V.

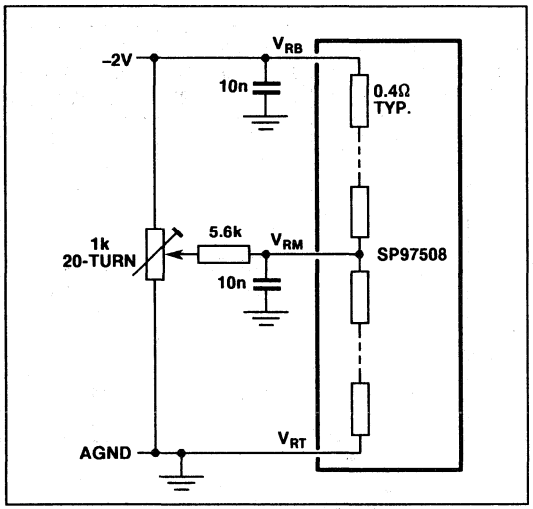



*Fig.6 Reference connections*

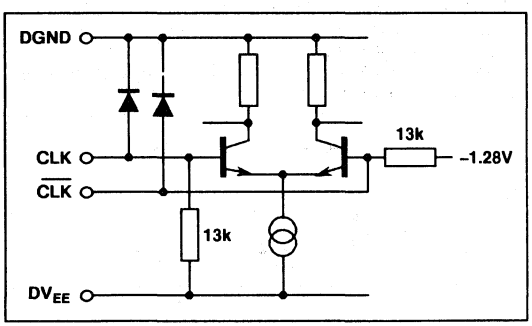



*Fig.7 Clock inputs*

**Clock Inputs CLK and $\overline{CLK}$ (Figs. 7 and 8)**

The SP97508 can be driven from either differential or single-ended ECL clocks. In either mode, the clock lines should be terminated with the line's characteristic impedance close to the device clock pins. Clock signals can be improved by incorporating the SP92701 line receiver into the circuit between the clock source and the SP97508. For full 110MHz operation, a conventional unity mark/space ratio clock can be used.

Single-ended drive can be simply provided by adding a 1nF chip or encapsulated chip capacitor from the $\overline{CLK}$ pin to DGND. The $\overline{CLK}$ pin will then self-bias at -1.28V, which is the mid-threshold for ECL. The device can then be clocked by an ECL signal into the CLK input.

**Timing (Fig.8)**

The analog input is acquired by the device shortly after the rising edge of the CLK signal. The internal latch causes a one cycle delay, hence the output data is valid one clock cycle after the acquisition of the analog signal.

The output data is further delayed by the clock-to-output delay ($t_D$ = 2.9ns typ.). This gives the advantage that the same timing and phase of the SP97508 CLK signal can be used to acquire the output data.

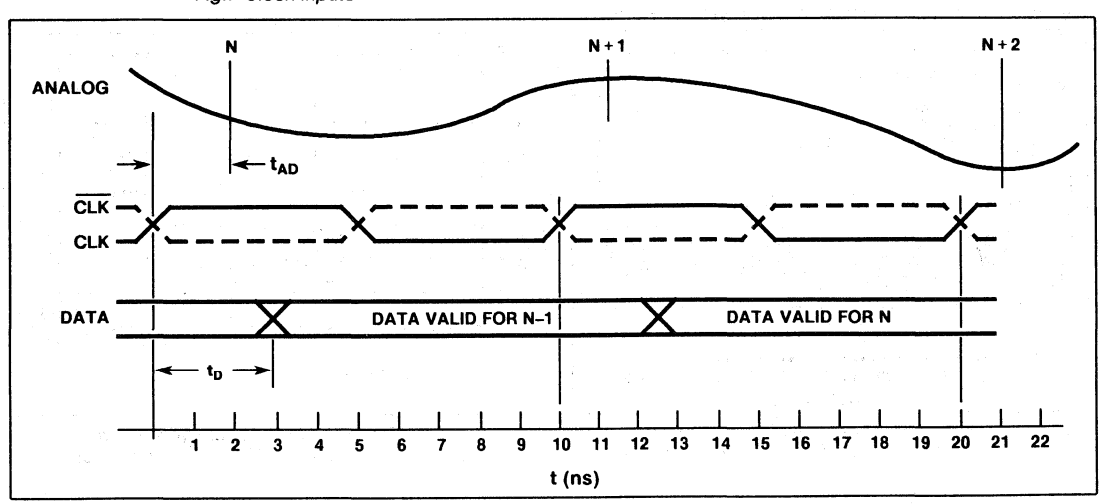



*Fig.8 Timing at 100MHz (typ.)*

**Output Coding (Table 1 and Fig. 9)**

With MINV and LINV left open circuit, the output will be coded in standard binary with all 1s code corresponding to the most positive input $V_{IN} = V_{RT} = 0V$.

An inverse binary output can be provided by connecting both MINV and LINV to ground.

Twos' complement coding (inverted MSB) can be provided by connecting only the MINV pin to ground and inverse twos' complement coding can be achieved by connected only the LINV pin to ground.

| $V_{IN}$ | Binary<br>MINV = O/C (0)<br>LINV = O/C (0) | Inv 2s' comp.<br>MINV = O/C (0)<br>LINV = GND (1) | 2s' comp.<br>MINV = GND(1)<br>LINV = O/C (0) | Inv binary<br>MINV = GND(1)<br>LINV = GND (1) |
|---|---|---|---|---|
| 0V | 111 11 | 100 00 | 011 11 | 000 00 |
| | 111 10 | 100 01 | 011 10 | 000 01 |
| | - | - | - | - |
| | - | - | - | - |
| | - | - | - | - |
| | 100 00 | 111 11 | 000 00 | 011 11 |
| | 011 11 | 000 00 | 111 11 | 100 00 |
| | - | - | - | - |
| | - | - | - | - |
| | - | - | - | - |
| | 000 01 | 011 10 | 100 01 | 111 10 |
| -2V | 000 00 | 011 11 | 100 00 | 111 11 |

*Table 1*

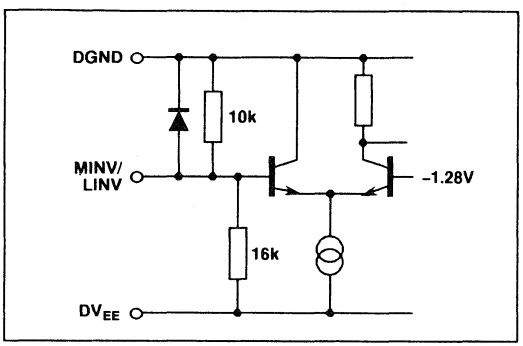



*Fig.9 MINV/LINV input*

**8-Bit ECL Outputs (Fig. 10)**

The outputs are standard ECL open emitters and therefore require pull-down resistors connected from the outputs to –5.2V or –2V digital supply. Single in-line resistors of value 680Ω to 1kΩ are recommended for termination to $DV_{EE}$. The outputs are capable of driving 200Ω terminations connected to a –2V supply.

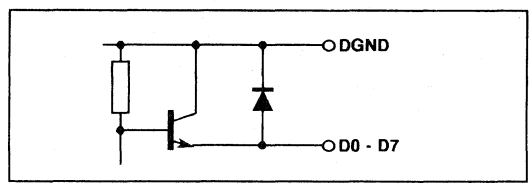



*Fig.10 Digital output*

## TYPICAL PERFORMANCE CHARACTERISTICS

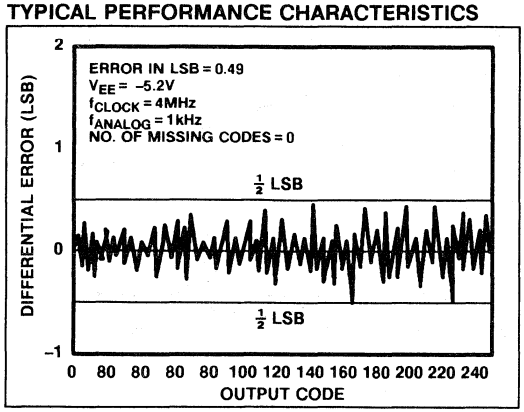



*Fig.11 Static differential linearity in LSB: typical production device*

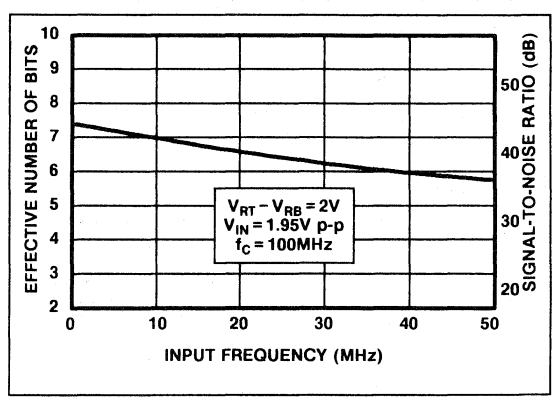



*Fig.12 Effective number of bits (ENOB) and signal-to-noise ratio (SNR) v. input frequency*

## CIRCUIT BOARD CONSTRUCTION

As with most PCB construction for analog to digital conversion, the best performance from the P97508 can be achieved by separating the ground plane into two sections: analog ground (AGND) and digital ground (DGND). This aids the device performance by reducing the degree of noise due to digital switching fed back to the analog section of the converter.

The digital noise is produced mainly by the ECL binary outputs, which, ideally, should be terminated by a 680Ω load to the –5.2V digital supply, $DV_{EE}$.

The device supplies are also a source of digital feedback, as they can be modulated by the digital output current. It is wise, therefore, to decouple ths SP97508 close to the device supply pins with good quality, high frequency capacitors.

### Notes on Construction (Pin Numbers refer to DG40 Package)

1. Use split analog and digital ground planes connected together close to the device. do not run the analog input next to the clock or data lines.
2. All NC pins must be grounded: connect pins 1 and 18 to DGND, all others to AGND.
3. Connect digital and analog supplies together at a point on the PCB away from the device.
4. Use 10nF capacitors for supply decoupling.
5. Use stripline techniques for signal paths longer than 5cm (2 inches).
6. Use 4.7μF electrolytic capacitors to decouple the –5.2V $V_{EE}$ supplies.

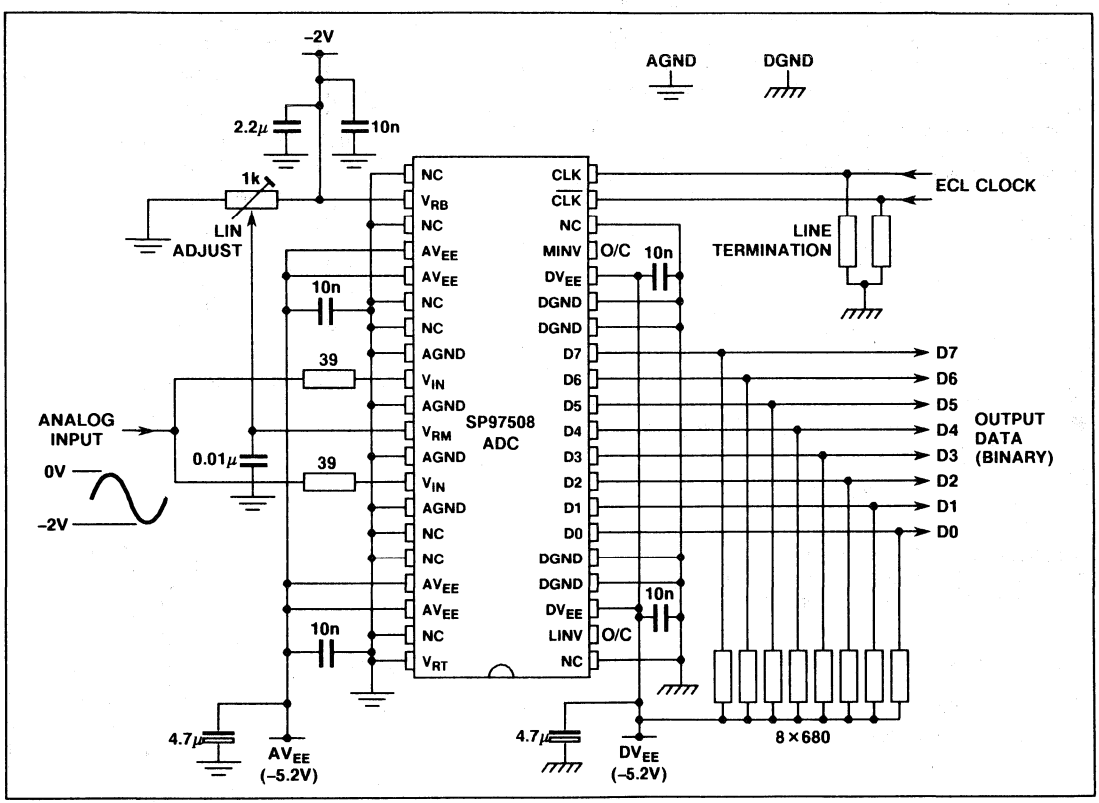



*Fig.13 Test and application circuit*

# SP98608

## 8-BIT LATCHED 450MHz MULTIPLYING D-A CONVERTER

The SP98608 is an ECL 10K compatible 8-bit latched DAC. The 2.2nsec settling time allows a 450 megasample per second conversion rate. An inherently low glitch design is used and the complementary current outputs are suitable for direct transmission line drive. The SP98608 design includes a high performance band-gap voltage reference and reference amplifier.

Both current and voltage multiplying modes are available. The input latch can be switched into transparent mode for applications that require low through delay.

### FEATURES

- Latched Inputs
- 2.2ns Settling Time ½ LSB Typically
- 8 Bits ±½ LSB Integral and Differential Linearity
- Operating Temperature Range -40°C to +85°C
- ECL 10K Standard Inputs
- Complementary Current Outputs, 40mA Full Scale
- Reference Temperature Coefficient Typically $<40$ppm/°C
- Single -5.2V Supply

### ORDERING INFORMATION

**SP98608 B DG** (Industrial - ceramic DIL package)
**SP98608 B LC** (Industrial - ceramic LCC package)

### APPLICATIONS

- Data Conversion
- Video Graphic Displays
- Instrumentation
- Waveform Generators
- High Speed Modems
- ADC Evaluation

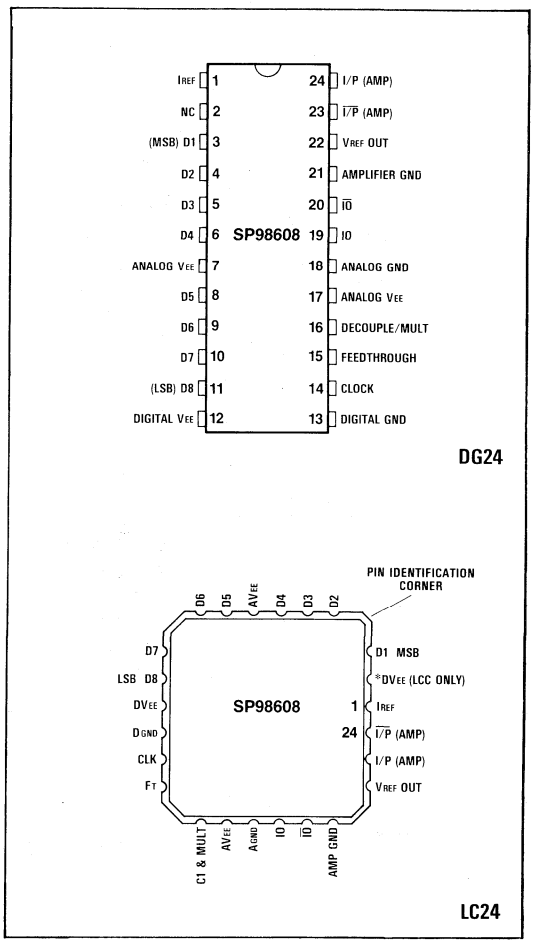



*Fig.1 Pin connections - top view*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | -5.7V |
| Digital input voltage | 0 to -4.5V |
| Maximum RSET | 2.5kΩ |
| Output reference supply (VL) | 0 to +3V |
| Reference input | ±2V |
| Storage temperature range | -55°C to 150°C |
| Operating junction temperature | <175°C |
| Lead temperature (soldering 60 sec) | 300°C |

### THERMAL CHARACTERISTICS

$\theta JC = 28°C/W$
$\theta JA = 90°C/W$

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = 25° C; $V_{EE}$ = -5.2V ± 5 %; $R_{SET}$ = 240Ω; Input voltage: High = -0.81V, Low = -1.85V

| Characteristic | Value | | | Unit | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Supply current $I_{EE}$ | | 135 | 154 | mA | All inputs at -1.8V |
| **Digital inputs** | | | | | |
| Input High voltage, $V_{IH}$ | -0.96 | | -0.81 | V | Standard ECL |
| Input Low voltage, $V_{IL}$ | -1.85 | | -1.65 | V | 10K compatible |
| Input High current, $I_{IH}$ | | 115 | 200 | μA | All inputs HI |
| Reference voltage $V_{REF}$ | | -1.280 | | V | |
| Reference voltage temp. coeff. | | 0 | ±80 | ppm/°C | -30°C to +85°C |
| Output current - full scale | 2 | | 44 | mA | $R_{SET}$ 1.3kΩ to 85Ω |
| Output current - full scale | 38 | 42 | | mA | $R_{SET}$ = 130Ω |
| Output compliance | -1.2 | | +1.0 | V | $T_{amb}$ = 25°C Note 3 |
| | -1.0 | | +1.0 | V | $T_{amb}$ = 85°C Note 3 |
| Bit size (LSB) | 158 | 166 | 175 | μA | Current output, $R_{SET}$ = 130Ω |
| Resolution | 8 | | | Bits | |
| **Accuracy** | | | | | |
| Integral non-linearity | | | ±0.5 | LSB | |
| Differential non-linearity | | | ±0.5 | LSB | |
| **Output dynamic parameters (see Note 1)** | | | | | |
| Rise time $t_r$ | | 600 | | ps | 10 to 90 % |
| Glitch energy (latched) | | 20 | | psV | Mid-point |
| Glitch energy (transparent) | | 140 | | psV | transition |
| Noise output | | -90 | -83 | dBm | See Note 2 |
| Power supply rejection ratio (output WRT supply) | 45 | 80 | | dB | ±0.3V at 20kHz |
| **Multiplying mode - voltage** | | | | | |
| Multiplying input voltage range | -2 | | 0 | V | |
| Reference input resistance | | 10 | | kΩ | |
| Multiplying input bandwidth | | 30 | | MHz | -3dB |
| Transfer function non-linearity | | 0.2 | 1.0 | %FS | DC |
| **Multiplying mode - current** | | | | | |
| Multiplying input current range | 1 | | 15 | mA | |
| Set current input resistance | | 400 | | Ohms | |
| Multiplying input bandwidth | | 300 | | MHz | -3dB |
| Transfer function non-linearity | | 1.0 | 3.0 | %FS | DC |

NOTES

1. Dynamic parameters guaranteed but not 100% tested.
2. Noise in any 10kHz band in the range 0.1 to 500MHz, for any digital input.
3. The output positive compliance can be increased beyond +1.0V at the expense of linearity. See Fig.4 for circuit configuration.
4. Analog and digital grounds should be connected together at the device pins.

| Dynamic characteristic (Note 1) | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Update rate | $F_{CLK}$ | | 450 | | MHz | |
| Latch setup time | $t_s$ | | 0.9 | | ns | |
| Latch hold time | $t_h$ | 0 | | | ns | |
| Settling time full scale | $t_{st}$ | | 2 | | ns | ½ LSB |
| Internal clock delay | $t_c$ | | 500 | | ps | |
| Initial time to 10 % | $t_i$ | | 50 | | ps | |

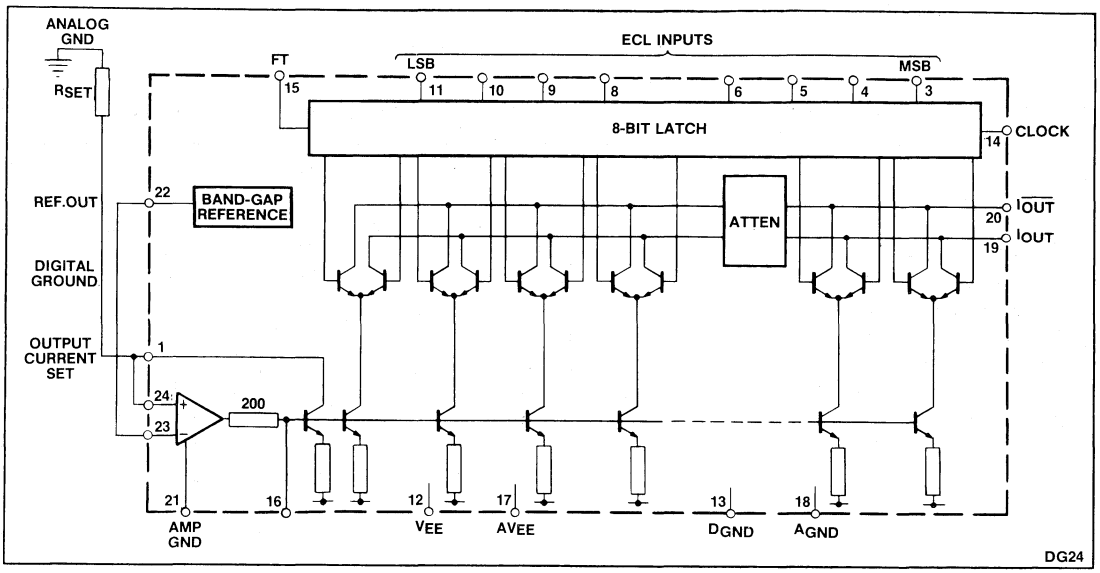



*Fig.2 SP98608 block diagram*

## OPERATING NOTES

The pinout of the SP98608 is shown in Fig. 1. External components are the current-setting resistor and decoupling capacitors.

The DAC has current outputs, with a nominal full-scale of 40mA, corresponding to a 1V drop across a 25Ω load.

The actual output current is determined by the on-chip reference voltage and an off-chip current-setting resistor.

Output current, $I_{OUT}$, is given by:

$$I_{OUT} = \frac{1600}{400 + R_{LOAD}} \times \frac{V_{REF}}{R_{SET}} \quad \text{at full scale}$$

A complementery $I_{OUT}$ is also provided. If single-ended output operation is employed, it must be ensured that the complementary output is terminated in an identical manner to the used output. The setting resistor, $R_{SET}$, is typically 130Ω, giving a full-scale output current of 37mA and should have a temperature coefficient similar to that of the output load resistor.

### Reference

The reference supply is internally compensated; however, to reduce the possibility of instability in some circuits, it has been bonded out to pin 16, it can therfore be decoupled to $AV_{EE}$ if required.

### Clock

The clock input is ECL 10K compatible. Data at the device inputs is acquired by the latch on the rising edge of the clock pulse.

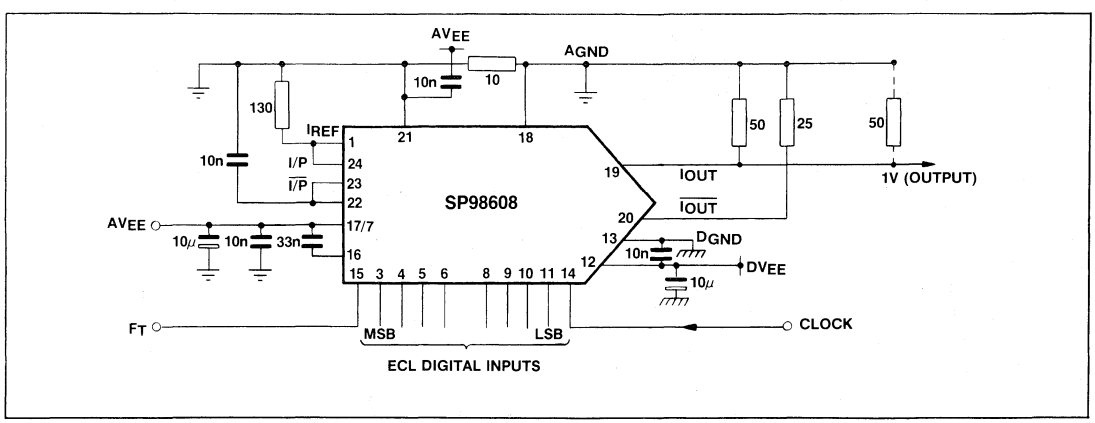



*Fig.3 Test/application circuit*

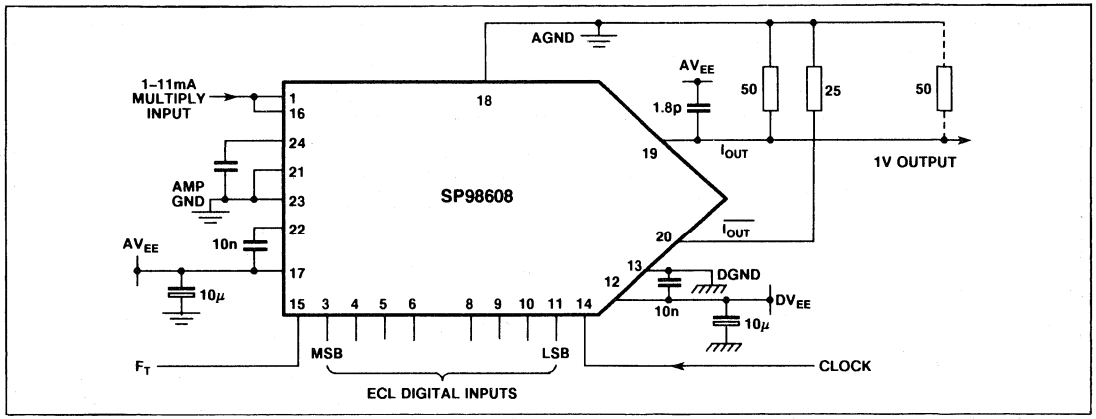



*Fig.4 Current multiplying mode*

## $F_T$ (Feedthrough)

The $F_T$ input allows both transparent or latched data inputs. When open circuits this pin will self bias to -2V and the data will be retained by the input latch for one half clock cycle.

When the $F_T$ input is connected to 0V the input latch will be transparent. In this mode, it is essential that the input data has low time skew (<100ps) to avoid output glitches.

## Multiplying Mode

Multiplying operation of the DAC is available in two modes: either a voltage applied in place of the internal reference, or a current supplied via the current set pin.

**Voltage Multiplying.** The transfer function is approximately: $I_{OUT}$ (Full Scale) = 4 x $V_{IN}/R_{SET}$. While this mode offers the best linearity of operation, the frequency response limitations mean that the maximumusable bandwidth is limited to approximately 50MHz.

**Current Multiplying.** A circuit for using the DAC in current multiplying mode is shown in Fig.4. The transfer function is approximately: $I_{OUT}$ (Full Scale) = 4 X $I_{IN}$. In this mode the current setting loop amplifier is not used.

The operational bandwidth of the current input to -3dB is at least 320MHz.

A 1V output is obtained into 25 ohm when a current of approximately 11mA is fed into pin 1 and the input code is selected for full output current.

## Output Compliance

Using the SP98608 with a load resistor not referred to ground, allows a larger output swing than the conventional connection of Fig. 3. Connecting analog ground and the current-setting resistor $R_{SET}$ to the load return supply ensures that the scale factor of the output is independent of the load .

Extending the compliance beyond +1V may cause slight degradation of linearity; +3V should be considered an absolute maximum.

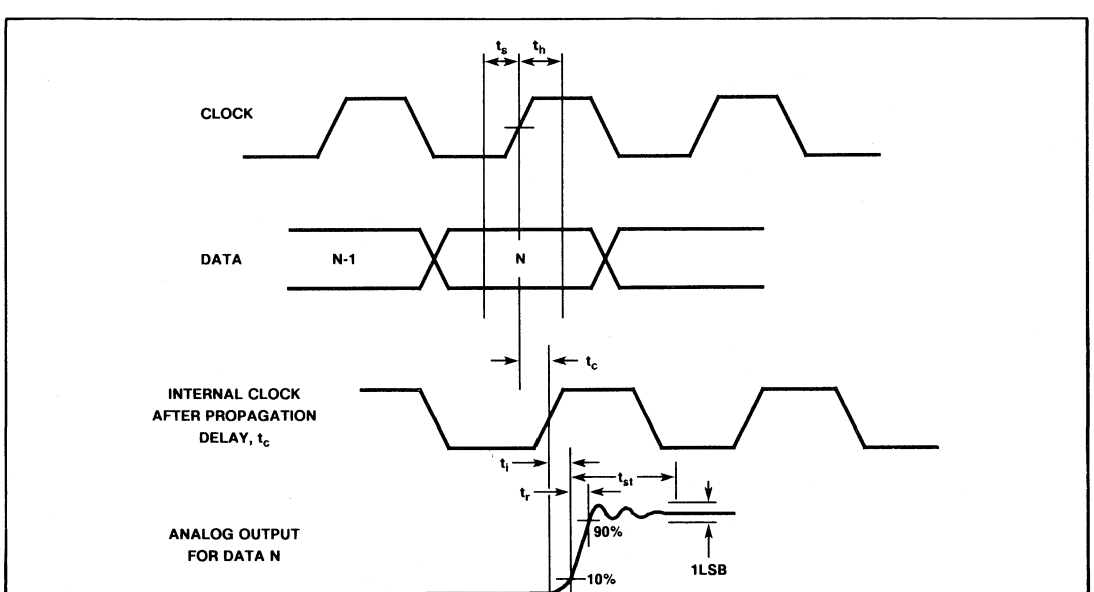



*Fig.5 Timing diagram - latched mode*

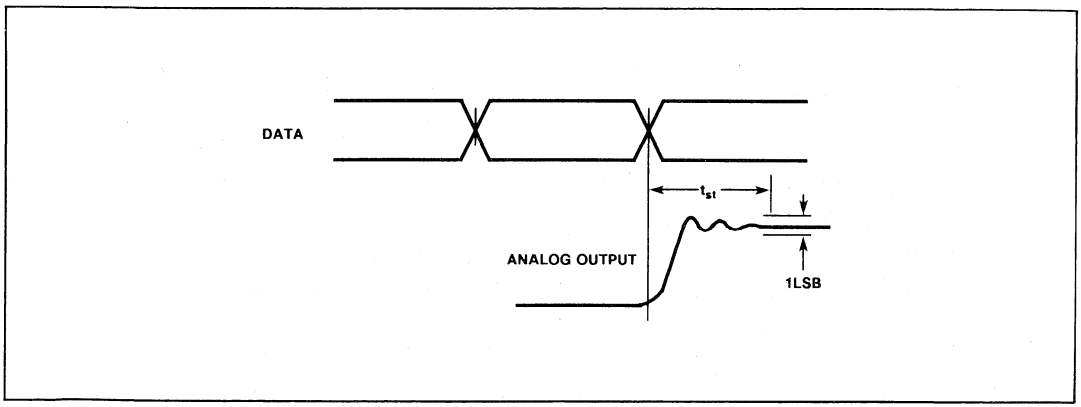



*Fig.6 Timing diagram - transparent mode*

# VP101

## 30/50MHz TRIPLE 8-BIT CMOS VIDEO DAC

The VP101 is a CMOS triple 8-bit video DAC designed for use in high performance, high resolution colour graphics applications.

The device uses video control inputs ($\overline{BLANK}$, $\overline{SYNC}$ and REF WHITE) to provide the VP101 with the video pedestal levels required to generate RS-343A compatible video signals into a doubly-terminated 75Ω load, or alternatively to produce RS-170 video signals across a singly-terminated 75Ω load.

Data and control inputs are fully pipelined to maintain synchronisation between the DAC outputs.

The full scale output current is defined by a 1.2V reference and a single resistor. The reference voltage is included on-chip in the VP101, but may be supplied externally if required (see Fig. 2).

Differential and integral linearity errors of the D-A converters are guaranteed to be a maximum of ±1LSB over the full operating temperature range.

### FEATURES

- 30/50MHz Pipeline Operation
- Triple 8-Bit D-A Converters
- ±1LSB Differential Linearity Error
- ±1LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A/RS-170 Compatible Levels
- Drives Doubly-Terminated 75Ω Load
- Single 5V Power Supply
- Typical Power Dissipation 500mW
- Direct Replacement for Bt101
- On-Chip Reference Available

### APPLICATIONS

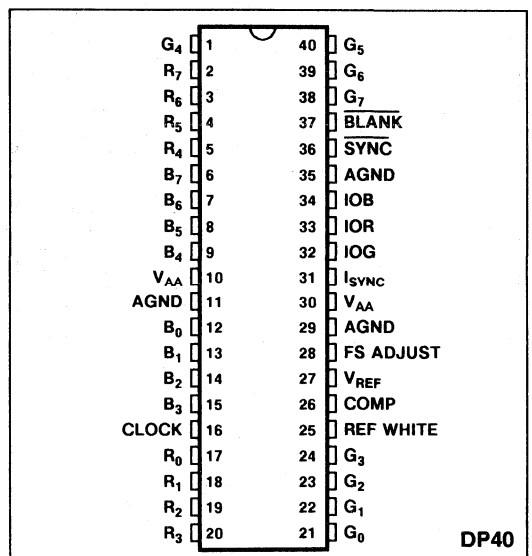
- High Resolution Colour Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

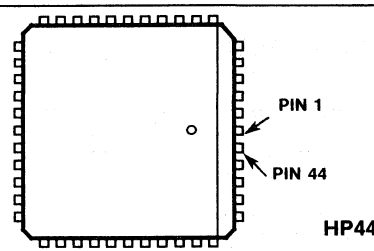
### ORDERING INFORMATION

**VP101-3 BA DP** (Commercial - Plastic DIL package)
**VP101-3 BA HP** (Commercial - Plastic J-lead package)
**VP101-5 BA DP** (Commercial - Plastic DIL package)
**VP101-5 BA HP** (Commercial - Plastic J-lead package)

### ABSOLUTE MAXIMUM RATINGS (Referenced to AGND)

| | |
|---|---|
| DC supply voltage, $V_{AA}$ | -0.3V to +7V |
| Digital input voltage | -0.3V to $V_{AA}$ +0.3V |
| Analog output short circuit duration | Indefinite |
| Ambient operating temperature | 0°C to +70°C |
| Storage temperature range | -55°C to +125°C |




| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | AGND | 16 | REF WHITE | 31 | $G_7$ |
| 2 | AGND | 17 | COMP | 32 | $G_6$ |
| 3 | $B_0$ | 18 | $V_{REF}$ | 33 | $G_5$ |
| 4 | $B_1$ | 19 | FS ADJUST | 34 | $G_4$ |
| 5 | $B_2$ | 20 | AGND | 35 | $R_7$ |
| 6 | $B_3$ | 21 | AGND | 36 | $R_6$ |
| 7 | CLOCK | 22 | $V_{AA}$ | 37 | $R_5$ |
| 8 | $R_0$ | 23 | $V_{AA}$ | 38 | $R_4$ |
| 9 | $R_1$ | 24 | $I_{SYNC}$ | 39 | $B_7$ |
| 10 | $R_2$ | 25 | IOG | 40 | $B_6$ |
| 11 | $R_3$ | 26 | IOR | 41 | $B_5$ |
| 12 | $G_0$ | 27 | IOB | 42 | $B_4$ |
| 13 | $G_1$ | 28 | AGND | 43 | $V_{AA}$ |
| 14 | $G_2$ | 29 | SYNC | 44 | $V_{AA}$ |
| 15 | $G_3$ | 30 | BLANK | | |

*Fig.1 Pin connections (not to scale) - top view.*

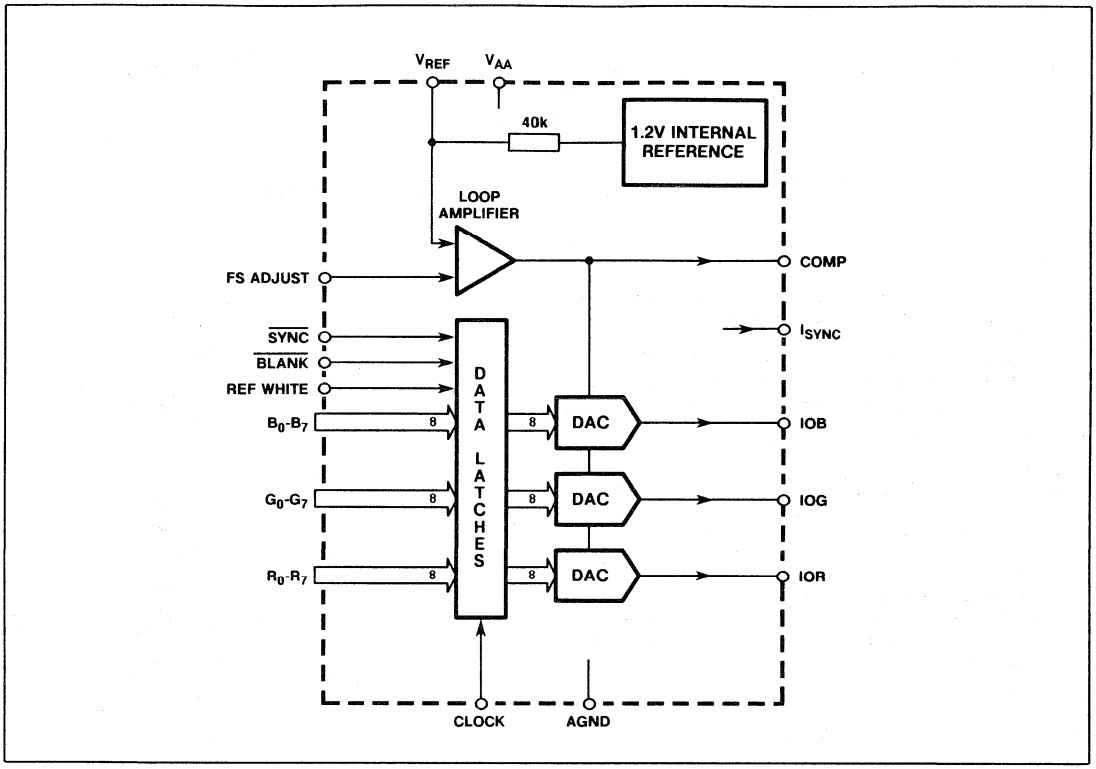



*Fig.2 Functional block diagram of VP101*

## RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply voltage | $V_{AA}$ | 4.75 | 5.00 | 5.25 | V | |
| Ambient operating temperature | $T_{amb}$ | 0 | | +70 | °C | |
| Output load | $R_L$ | | 37.5 | | Ω | For RS-343A compatible output levels |
| Reference voltage (internal or external) | $V_{REF}$ | 1.14 | 1.20 | 1.26 | V | |
| FS ADJUST resistor | $R_{SET}$ | | 542 | | Ω | |

## THERMAL CHARACTERISTICS

| | DP | HP | |
|---|---|---|---|
| Thermal resistance, chip-to-case $\theta_{jc}$ | 12 | 17 | °C/W |
| Thermal resistance, chip-to-ambient $\theta_{jA}$ | 45 | 50 | °C/W |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
As specified in Recommended Operating Conditions

### DC CHARACTERISTICS

| Parameter | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Resolution (each DAC) | | 8 | | | Bits | |
| **Accuracy (each DAC)** | | | | | | |
| Integral linearity error | INL | | ±0.3 | ±1 | LSB | |
| Differential linearity error | DNL | | ±0.3 | ±1 | LSB | |
| Grey scale error | | | ±1 | ±5 | % grey scale | |
| Monotonicity | | | Guaranteed | | | |
| **Digital Inputs** | | | | | | |
| Input high voltage | $V_{IH}$ | 3.0 | | $V_{AA}$ + 0.3 | V | Binary coding |
| Input low voltage | $V_{IL}$ | AGND-0.3 | | 1.2 | V | |
| Input high current | $I_{IH}$ | | | 1 | μA | |
| Input low current | $I_{IL}$ | | | -1 | μA | |
| **Analog Outputs** | | | | | | |
| Grey scale current range | | 15 | | 20 | mA | |
| | | | 255 | | LSB | |
| **Output currents** | | | | | | |
| White level relative to blank level | | 17.69 | 19.06 | 20.40 | mA | RS-343A tolerances assumed |
| | | | 276 | | LSB | |
| White level relative to black level | | 16.74 | 17.62 | 18.50 | mA | |
| | | | 255 | | LSB | |
| Black level relative to blank level | | 0.95 | 1.44 | 1.90 | mA | |
| | | | 21 | | LSB | |
| Blank level on IOR, IOB | | 0 | 5 | 50 | μA | |
| | | | 0 | | LSB | |
| Blank level on IOG | | 6.29 | 7.62 | 8.96 | mA | |
| | | | 111 | | LSB | |
| Sync level on IOG | | 0 | 5 | 50 | μA | |
| | | | 0 | | LSB | |
| LSB size | LSB | | 69.1 | | μA | |
| DAC to DAC matching | | | 2 | | % | |
| Output compliance | $V_{OC}$ | -0.5 | | +1.4 | V | |
| External $V_{REF}$ input current | $I_{REF}$ | | | 10 | μA | |
| Internal reference voltage | $V_{REF}$ | 1.14 | 1.20 | 1.26 | V | |
| Internal $V_{REF}$ temperature coefficient | | | 40 | | ppm/°C | |

### AC CHARACTERISTICS

| Parameter | Symbol | VP101-5 | | | VP101-3 | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Max clock rate | $f_{max}$ | 50 | | | 30 | | | MHz | |
| Data and control setup time | $t_{SU}$ | 6 | | | 8 | | | ns | |
| Data and control hold time | $t_H$ | 2 | | | 2 | | | ns | |
| Clock cycle time | $t_{CYC}$ | 20 | | | 33.3 | | | ns | |
| Clock pulse width high time | $t_{CLKH}$ | 8 | | | 10 | | | ns | |
| Clock pulse width low time | $t_{CLKL}$ | 8 | | | 10 | | | ns | |
| Analog output delay | $t_{DLY}$ | | 10 | | | 10 | | ns | |
| Analog output rise/fall time | $t_{VRF}$ | | | 8 | | | 9 | ns | |
| Analog output settling time | $t_S$ | | 12 | | | 15 | | ns | |
| Glitch impulse | | | 100 | | | 100 | | pV-sec | |
| Analog output skew | | | 0 | 3 | | 0 | 3 | ns | |
| Pipeline delay | | 1 | 1 | 1 | 1 | 1 | 1 | Clock | |
| $V_{AA}$ supply current | $I_{AA}$ | | 120 | 175 | | 100 | 140 | mA | At $f_{max}$, $V_{AA}$ = 5V |

## CIRCUIT DESCRIPTION

As shown in Fig. 2, the VP101 contains three 8-bit D-A converters, input latches, and a loop amplifier.

On the rising edge of each clock cycle (see Fig. 4), 24 bits of colour information ($R_0$-$R_7$, $G_0$-$G_7$, and $B_0$-$B_7$) are latched into the device and presented to the three 8-bit D-A converters. The REF WHITE input, also latched on the rising edge of each clock cycle, and will force the inputs of each D-A converter to $FF.

$\overline{SYNC}$ and $\overline{BLANK}$ are latched on the rising edge of the clock to maintain synchronisation with the colour data. These inputs add appropriately weighted currents to the analog outputs, producing the specific output levels required for video applications as shown in Fig. 3. Table 1 details how the $\overline{SYNC}$, $\overline{BLANK}$ and REF WHITE inputs modify the output levels.

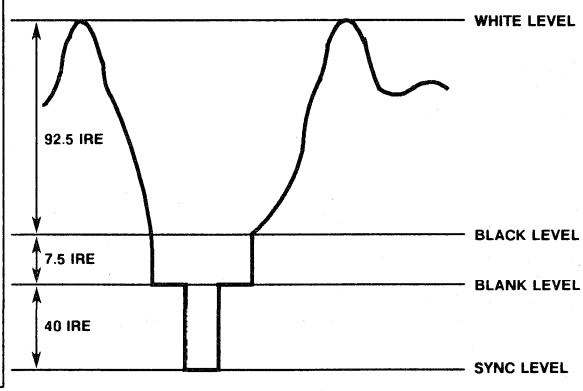
The $I_{SYNC}$ current output is typically connected directly to the IOG output and is used to encode sync information onto the IOG output. If $I_{SYNC}$ is not connected to the IOG output, sync information will not be encoded on the green channel, and the IOR, IOG and IOB outputs will have the same full scale output current.

Full Scale output current is set by an external resistor ($R_{SET}$) between the FS ADJUST pin and AGND. $R_{SET}$ has a typical value of 542Ω for generation of RS-343A video into a 37.5Ω load. The VP101 may be used in applications where an external 1.2V (typical) reference is provided, in which case the external reference should be temperature compensated and provide a low impedance output.

The D-A converters on the VP101 use a segmented architecture in which bit currents are routed to either the output or AGND by a sophisticated decoding scheme. This architecture eliminates the need for precision component ratios and greatly reduces the switching transients associated with turning current sources on or off. Monotonicity and low glitch energy are guaranteed by using identical current sources and current steering their outputs. An on-chip operational amplifer stabilizes the full scale output current against temperature and power supply variations.

The analog outputs of the VP101 are capable of directly driving a 37.5Ω load, such as a doubly terminated 75Ω co-axial cable or interpolation filters.

| Red/Blue | | Green | |
|---|---|---|---|
| mA | V | mA | V |
| 19.06 | 0.714 | 26.68 | 1.000 |
| 1.44 | 0.054 | 9.06 | 0.340 |
| 0.00 | 0.000 | 7.62 | 0.286 |
| | | 0.000 | 0.000 |




NOTE : 75Ω doubly terminated load, $R_{SET}$ = 542Ω, $V_{REF}$ = 1.2V, $I_{SYNC}$ connected to IOG, RS-343A levels assumed

*Fig.3 Composite video output waveform*

| Description | IOG (mA) | IOR/IOB (mA) | REF WHITE | $\overline{SYNC}$ | $\overline{BLANK}$ | DAC I/P Data |
|---|---|---|---|---|---|---|
| White Level | 26.68 | 19.06 | 1 | 1 | 1 | $XX |
| White Level | 26.68 | 19.06 | 0 | 1 | 1 | $FF |
| Data | Data + 9.06 | Data + 1.44 | 0 | 1 | 1 | Data |
| Data-Sync | Data + 1.44 | Data + 1.44 | 0 | 0 | 1 | Data |
| Black Level | 9.06 | 1.44 | 0 | 1 | 1 | $00 |
| Black-Sync | 1.44 | 1.44 | 0 | 0 | 1 | $00 |
| Blank Level | 7.62 | 0 | X | 1 | 0 | $XX |
| Sync Level | 0 | 0 | X | 0 | 0 | $XX |

NOTE : Typical with full scale IOG = 26.68mA, $R_{SET}$ = 542Ω, $V_{REF}$ = 1.2V, $I_{SYNC}$ connected to IOG

*Table 1 Video output truth table*

## PIN DESCRIPTIONS

| Pin name | Description |
|---|---|
| $\overline{\text{BLANK}}$ | Composite blank control input. A logic '0' forces the IOR, IOG and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the rising edge of CLOCK. When $\overline{\text{BLANK}}$ is a logic zero, the $R_0$-$R_7$, $G_0$-$G_7$, $B_0$-$B_7$, and REF WHITE inputs are ignored. |
| $\overline{\text{SYNC}}$ | Composite sync control input. A logic '0' on this input switches off a 40 IRE current source on the $I_{SYNC}$ output. $\overline{\text{SYNC}}$ does not override any other control or data input, as shown in Table 1; therefore it should be asserted only during the blanking interval. It is latched on the rising edge of CLOCK. |
| REF WHITE | Reference white control input. A logic '1' on this input forces the IOR, IOG, and IOB outputs to the white level, regardless of the $R_0$-$R_7$, $G_0$-$G_7$ and $B_0$-$B_7$ inputs. It is latched on the rising edge of CLOCK. See Table 1. |
| $R_0$-$R_7$<br>$G_0$-$G_7$<br>$B_0$-$B_7$ | Red, Green, and Blue data inputs. $R_0$, $G_0$, and $B_0$ are the least significant data bits. They are latched on the rising edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane. |
| CLOCK | Clock input. The rising edge of CLOCK latches the $R_0$-$R_7$, $G_0$-$G_7$, $B_0$-$B_7$ $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$, and REF WHITE inputs. It is typically the pixel clock rate of the video system. It is recommended that the CLOCK input be driven by a dedicated CMOS buffer. |
| IOR, IOG, IOB | Red, Green and Blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω co-axial cable. All outputs, whether used or not, should have the same output load. (Note: A DC path to ground must be maintained) |
| $I_{SYNC}$ | Sync current output. Typically this current output is directly wired to the IOG output, and enables sync information to be encoded onto the green channel. A logic '0' on the $\overline{\text{SYNC}}$ input results in no current being output onto this pin, while a logic '1' results in the following current being output:<br>$I_{SYNC}\,(mA) = 3468 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} \equiv 111$ LSBs<br>If sync information is not required on the green channel, this output may be connected to $V_{AA}$ and the $\overline{\text{SYNC}}$ input tied high, causing the $I_{SYNC}$ current source to be turned off, reducing the power consumption. |
| FS ADJUST | Full scale adjust control. A resistor ($R_{SET}$) connected between this pin and AGND controls the magnitude of the full video signal (Fig. 3). The current flowing in the $R_{SET}$ resistor is equal to 32 LSBs. Note that the IRE relationships in Fig. 3 are maintained, regardless of the full scale output current.<br>The relationship between $R_{SET}$ and the full scale current on IOG (assuming $I_{SYNC}$ is connected to IOG) is:<br>$IOG\,(mA) = 12082 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} \equiv 387$ LSBs<br>The full scale output current on IOR and IOB for a given $R_{SET}$ is defined as:<br>$IOR, IOB\,(mA) = 8624 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} \equiv 276$ LSBs |
| COMP | Compensation pin. This pin provides compensation for the internal loop amplifier. A 0.01μF ceramic capacitor must be connected between this pin and the nearest $V_{AA}$ pin.<br>Connecting the capacitor to $V_{AA}$ rather than to AGND provides the highest possible power supply noise rejection. |
| $V_{REF}$ | Voltage reference output. The output from an internal reference circuit, providing 1.2V (typical) reference. A 0.1μF ceramic capacitor must be used to decouple this output to $V_{AA}$. |
| AGND | Analog ground. All AGND pins must be connected. |
| $V_{AA}$ | Analog power. All $V_{AA}$ pins must be connected. |

## APPLICATION NOTES

### RS-343A and RS-170 Video Generation

For the generation of RS-343A compatible video levels it is recommended that a doubly terminated 75Ω load be used with an $R_{SET}$ resistor value of approximately 542Ω.

Similarly for the generation of RS-170-compatible video, it is recommended that a singly terminated 75Ω load be used with an $R_{SET}$ value of about 774Ω. If the VP101 is not driving a large capacitive load, there will be negligible difference in video quality between doubly terminated 75Ω and singly terminated 75Ω loads.

If driving a large capacitive load (load $RC > 1/20\Pi f_C$) it is recommended that an output buffer with an unloaded gain > 2 be used to drive a doubly terminated 75Ω load.

### COMP Resistor

To optimise the settling time of the VP101, a resistor may be added in series between the COMP capacitor and COMP pin. The series resistor damps inductive ringing on COMP, thus improving settling time.

### Non-Video Applications

The VP101 may be used in non-video applications by disabling the video specific control inputs. REF WHITE should be a logic '0' while $\overline{BLANK}$ and $\overline{SYNC}$ should be a logic '1'. $I_{SYNC}$ should be connected to $V_{AA}$ or AGND. All three outputs will have the same full scale output current.

The relationship between $R_{SET}$ and full scale output current ($I_{out}$) in this configuration is as follows:

$$I_{out}\,(mA) = 7968 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} = 255 \text{ LSBs}$$

$$\text{Note that 1 LSB} \equiv \frac{V_{REF}\,(V)}{32 \times R_{SET}\,(\Omega)}$$

With the data inputs at $00, there is a DC offset current ($I_{min}$) defined as follows:

$$I_{min}\,(mA) = 656 \times \frac{V_{REF}\,(V)}{R_{SET}\,(\Omega)} = 21 \text{ LSBs}$$

Therefore, the total full scale output current will be $I_{out} + I_{min}$. The REF WHITE input may optionally be used as a 'force to full scale' control.

## TIMING WAVEFORMS

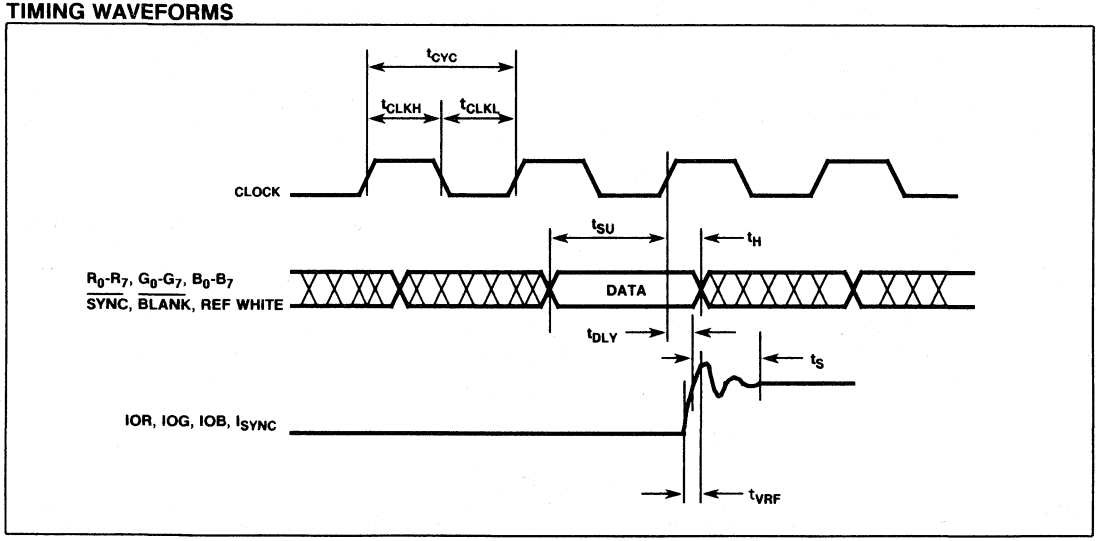



*Fig.4 Input/output timing*

NOTES

1. Output delay, $t_{DLY}$, measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
2. Settling time, $t_S$, measured from the 50% point of full scale transition to the output remaining within ±1 LSB.
3. Output rise/fall time , $t_{VRF}$, measured between the 10% and 90% points of full scale transition.

## PCB LAYOUT CONSIDERATIONS

To obtain the optimum performance from the VP101 great care must be taken in the PCB layout to ensure low noise power and ground lines. This can be achieved by shielding the digital inputs and providing good decoupling.

### Power and Ground Planes

The VP101 and its associated circuitry should have its own separate power/ground planes, which should be connected at a single point through a ferrite bead. It is important that the regular PCB power and ground planes do not overlay portions of the analog power or ground planes to minimise plane-to-plane noise coupling.

### Digital Signal Interconnect

The digital signal lines to the VP101 should be isolated as much as possible from the analog circuitry. Due to the high clock rates used, the clock lines to the VP101 should be as short as possible to minimise noise pickup.

Any pull-up resistors used on the digital inputs should be connected to the regular PCB power plane, not to the analog power plane.

### Supply Decoupling

Noise on the analog power plane will be further reduced by the use of multiple decoupling capacitors (See Fig. 5.)

Optimum performance is obtained with 0.1$\mu$F chip ceramic capacitors placed as close as possible to the $V_{AA}$ pins, with the shortest leads possible to reduce lead inductance.

It should be noted that while the loop amplifier circuitry of the VP101 will reject power supply noise, this rejection decreases with frequency. Any high frequency noise on the regular supply (such as produced by a switch mode power supplies) must be adequately suppressed, else the designer should consider using a three terminal regulator to supply the analog power plane.

### Analog Signal Interconnect

For optimum performance the analog output connectors and source termination resistors should be as close as possible to the VP101 to minimise noise pickup and reflections due to impedance mismatch. The video output signals should overlay the ground plane and not the analog power plane, to maximise the high frequency power supply rejection.

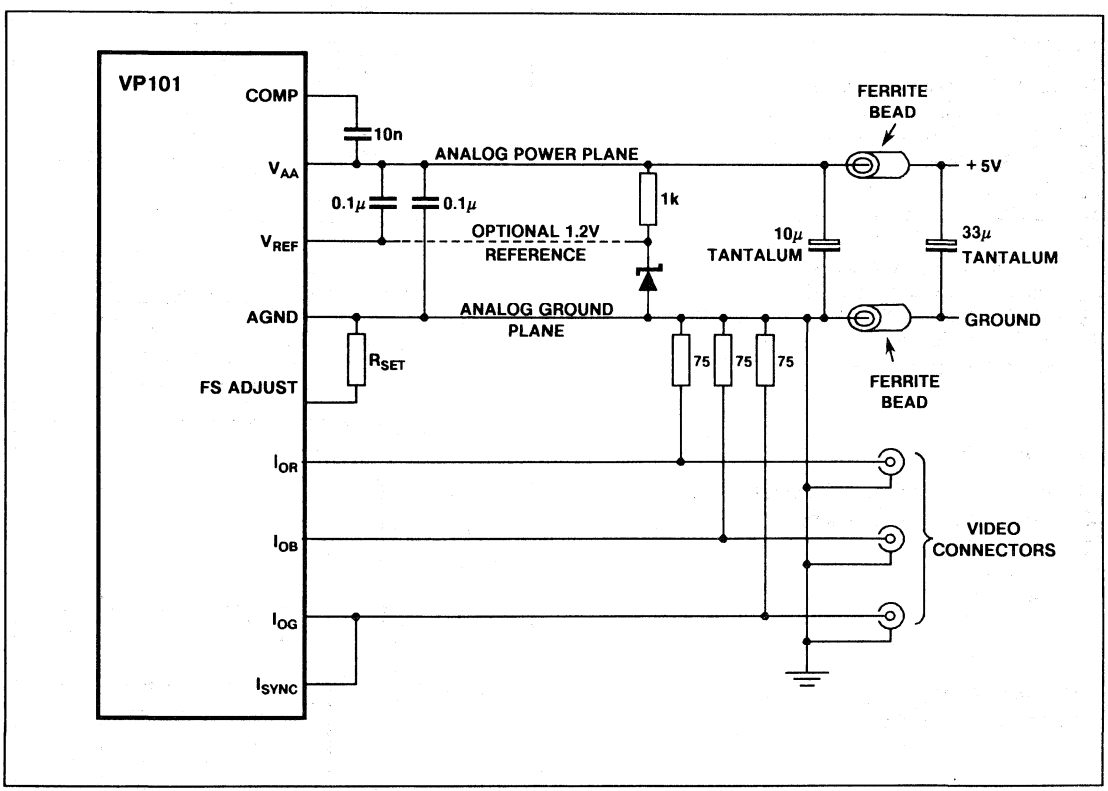



*Fig.5 VP101 typical connections*

# VP109

## 250MHz, TRIPLE 8 BIT VIDEO DAC

The VP109 is a triple 8-bit video DAC designed for use in high performance, high resolution colour graphics applications.

The device uses video control inputs, (BLANK, SYNC and OVERLAY) to provide the VP109 with the video pedestal levels required to generate RS-343A compatible video signals into a doubly-terminated 75Ω load.

Data and control inputs are fully pipelined to maintain synchronisation between the DAC outputs.

The full scale output current is defined by a 1.2V reference and a single resistor. The reference voltage is included on-chip in the VP109.

Differential and integral linearity errors of the D-A converters are guaranteed to be a maximum of ±½LSB over the full operating temperature range.

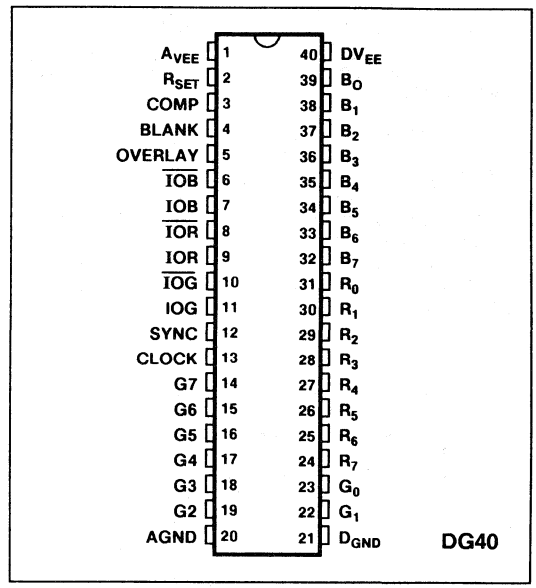



*Fig.1 Pin connections - top view*

### FEATURES

- 250MHz Pipeline Operation
- Triple 8-Bit D-A Converters
- ±½LSB Differential Linearity Error
- ±½LSB Integral Linearity Error
- Guaranteed Monotonic
- RS-343A Compatible Levels
- Drives Doubly-Terminated 75Ω Load
- 10KH ECL Compatible Inputs
- Typical Power Dissipation 2W
- Pin Compatible with Bt109 and TDC 1318
- On-Chip Reference
- 40 Pin Cerdip Package

### APPLICATIONS

- High Resolution Colour Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

### ORDERING INFORMATION

**VP109J** (Commercial Ceramic DIL Package)

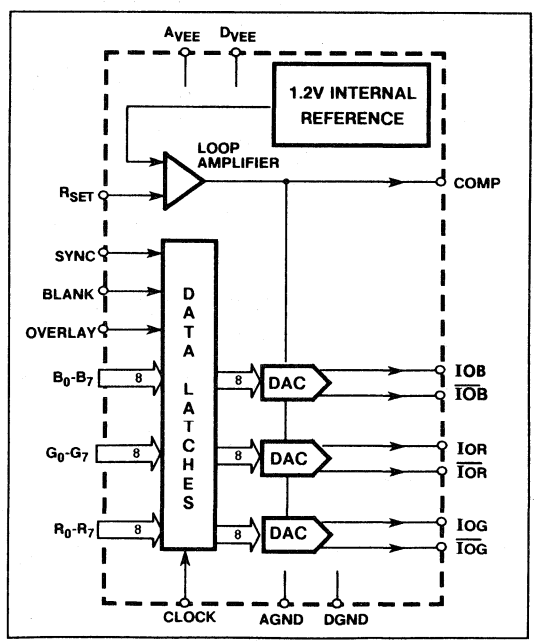



*Fig.2 Functional block diagram of VP109*

# VP1058

## 8-BIT, 25MHz, VIDEO FLASH ADC ( SINGLE + 5V SUPPLY)

The VP1058 is a low power analog-to-digital flash converter which requires no preceding sample and hold stage. Operating from a single +5V supply, it is capable of digitising analog signals with frequencies up to the Nyquist limit.

Output data is available in four possible 8-bit formats, selectable via two digital control inputs, giving either true or inverted code in binary or offset twos' complement.

### FEATURES

- 8-Bit Resolution
- 25MHz Conversion Rate
- 60MHz 3dB Analog Input Bandwidth
- Single +5V Supply Operation
- Low Power Consumption (Typically 600mW)
- +3V to +5V Analog Input Range
- Selectable Data Format
- TTL Compatible
- Direct Replacement For TDC 1058 or CXA 1096P
- Low Cost
- No Missing Codes - Guaranteed

### APPLICATIONS

- Digital Television
- Computing
- Radar
- Medical Imaging
- Nucleonics
- Low-Cost, High-Speed Data Conversion

### OPERATING TEMPERATURE RANGE

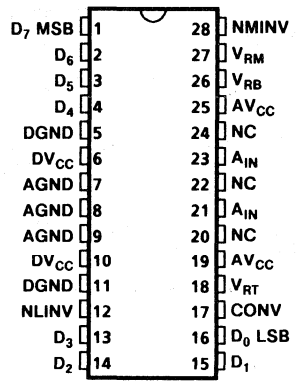
Commercial 0°C to 70°C

### ORDERING INFORMATION

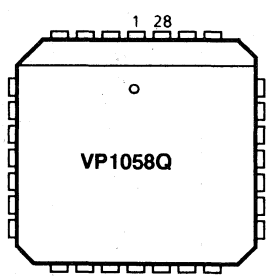
**VP1058 E** (Commercial - Plastic DIL Package, DP28)
**VP1058 Q** (Commercial - Quad Plastic J Lead Package, HP28)
**VP1058 J** (Commercial - Ceramic DIL Package, DG28)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | +7V |
| Analog input, $A_{IN}$ | $V_{CC}$ +0.5 |
| Reference voltage $V_{RT}$, $V_{RB}$ | $V_{CC}$ +0.5 |
| Reference range, $V_{RT}$, $V_{RB}$ | 2.5V |
| Digital inputs | $V_{CC}$ |
| Mid-ref input current | -50mA to +50mA |
| Digital output current | -20mA to +20mA |
| Voltage between AGND and DGND | -0.5V to +0.5V |
| Voltage between $AV_{CC}$ and $DV_{CC}$ | -0.5V to +0.5V |




VP1058E - DP28
VP1058J - DG28




HP28

| Pin | Function | Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|---|---|
| 1 | $D_7$ MSB | 8 | AGND | 15 | $D_1$ | 22 | NC |
| 2 | $D_6$ | 9 | AGND | 16 | $D_0$ LSB | 23 | $A_{IN}$ |
| 3 | $D_5$ | 10 | $DV_{CC}$ | 17 | CONV | 24 | NC |
| 4 | $D_4$ | 11 | DGND | 18 | $V_{RT}$ | 25 | $AV_{CC}$ |
| 5 | DGND | 12 | NLINV | 19 | $AV_{CC}$ | 26 | $V_{RB}$ |
| 6 | $DV_{CC}$ | 13 | $D_3$ | 20 | NC | 27 | $V_{RM}$ |
| 7 | AGND | 14 | $D_2$ | 21 | $A_{IN}$ | 28 | NMINV |

*Fig.1 Pin Connections (Top View)*

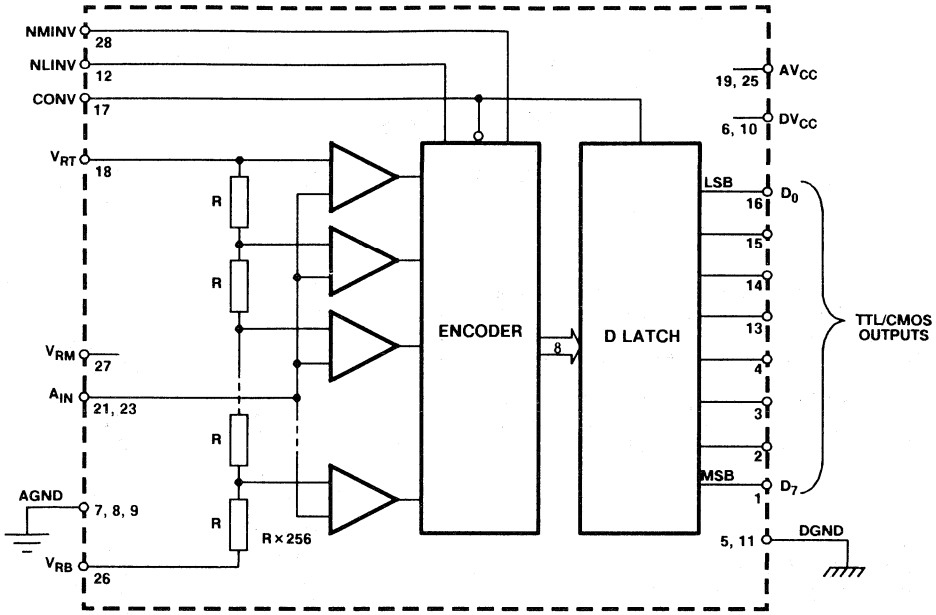



*Fig.2 Internal block diagram*

## PIN DESCRIPTIONS

| Pin No. | Function | Description |
|---|---|---|
| 1 | $D_7$ | Most significant bit (output data bit 7) |
| 2 - 4 | $D_6$ - $D_4$ | Output data bits 6 to 4 |
| 5, 11 | DGND | Digital ground |
| 6, 10 | $DV_{CC}$ | Digital supply pin (+5V) |
| 7-9 | AGND | Analog ground |
| 12 | NLINV | Not Least significant bits INvert - inverts data bits $D_0$ to $D_6$ when taken low |
| 13-15 | $D_3$ - $D_1$ | Output data bits 3 to 1 |
| 16 | $D_0$ | Least significant bit (output data bit 0) |
| 17 | CONV | Clock input - the rate of input (CONVert) clock signal determines the ADC sampling rate |
| 18 | $V_{RT}$ | Top of reference resistor chain |
| 19, 25 | $AV_{CC}$ | Analog supply pin |
| 20, 22, 24 | NC | Not connected |
| 21, 23 | $A_{IN}$ | Analog input pin |
| 26 | $V_{RB}$ | Bottom of reference resistor chain |
| 27 | $V_{RM}$ | Midpoint of reference resistor - can be used for linearity adjustment |
| 28 | NMINV | Not Most significant bit INvert - inverts data bit $D_7$ when taken low |

## THERMAL CHARACTERISTICS

| | |
|---|---|
| Storage Temperature Range | -65°C to +150°C |
| Maximum Junction Operating Temperature | +175°C |
| Lead Temperature (soldering 60 seconds) | 300°C |

| | DP | HP | DG | |
|---|---|---|---|---|
| Junction to Ambient $\theta jA$ | 55 | 57 | 44 | °C/W |
| Junction to Case $\theta jc$ | 14 | 15 | 9 | °C/W |

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply Voltage | 5V -0.25V, +0.5V |
| Reference $V_{RT}$ | 5V ±0.1V |
| Reference $V_{RB}$ | 3V ±0.1V |
| $AV_{CC}$ to $DV_{CC}$ | 0V ±50mV |
| Analog Input | 4V ±1V |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):** $V_{CC}$ = +5V ±0.25V, $T_{amb}$ = 25°C

### DC CHARACTERISTICS

| Characteristic | Symbol | Temp | Test level | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| **Power Supply** | | | | | | | | |
| Supply voltage | $AV_{CC}/DV_{CC}$ | Full | 4 | 4.75 | | 5.25 | V | AGND/DGND = 0V |
| Supply current | $I_{CC}$ | Full | 4 | 80 | 120 | 180 | mA | |
| | | 25 | 1 | 100 | 120 | 150 | mA | |
| Power dissipation | P | Full | 4 | 400 | 600 | 900 | mW | |
| | | 25 | 1 | 500 | 600 | 750 | mW | |
| **Analog Input** | | | | | | | | |
| Input range | $A_{IN}$ | Full | 4 | $V_{RB}$ | | $V_{RT}$ | V | |
| Input bias current | $I_{IN}$ | Full | 4 | 60 | 150 | 500 | µA | |
| 3dB bandwidth | $f_{3dB}$ | 25 | 4 | | 60 | | MHz | |
| Input capacitance | $C_{IN}$ | 25 | 4 | | 30 | | pF | |
| **Reference Ladder** | | | | | | | | |
| Ladder resistance | $R_D$ | Full | 4 | 50 | 90 | 125 | Ω | |
| | | 25 | 1 | 75 | 90 | 105 | Ω | |
| Ladder voltage (top) | $V_{RT}$ | Full | 4 | | 5.0 | $AV_{CC}$ + 0.1 | V | $V_{RT} > V_{RB}$ |
| Ladder voltage (bottom) | $V_{RB}$ | Full | 4 | 2.5 | 3.0 | | V | |
| Ladder offset (top) | $V_{RTO}$ | 25 | 5 | | | | mV | |
| Ladder offset (bottom) | $V_{RBO}$ | 25 | 5 | | | | mV | |
| Ladder temp. coeff. | $R_{TC}$ | Full | 5 | | 0.33 | | Ω/°C | |
| **Digital Inputs** | | | | | | | | |
| Logic '1' voltage | $V_{IH}$ | Full | 4 | 2.0 | | | V | |
| Logic '0' current | $V_{IL}$ | Full | 4 | | | 0.8 | V | |
| Logic '1' current | $I_{IH}$ | Full | 4 | | | 350 | µA | $V_I = V_{CC}$ = MAX |
| Logic '1' current | $I_{IH}$ | Full | 4 | | | 75 | µA | $V_I$ = 2.4V, $V_{CC}$ = MAX |
| Logic '0' current | $I_{IL}$ | Full | 4 | | | -100 | µA | $V_I$ = 0V, $V_{CC}$ = MAX |
| **Digital Outputs** | | | | | | | | |
| Logic '1' voltage | $V_{OH}$ | Full | 4 | 2.4 | | | V | Into a standard LSTTL load |
| | | 25 | 1 | 2.4 | | | V | |
| Logic '0' voltage | $V_{OL}$ | Full | 4 | | | 0.4 | V | |
| | | 25 | 1 | | | 0.4 | V | |
| **Static performance** | | | | | | | | |
| Differential non-linearity | DNL | Full | 4 | | ±0.5 | | LSB | |
| | | 25 | 4 | | ±0.5 | | LSB | |
| Integral non-linearity | INL | Full | 4 | | ±0.5 | | LSB | |
| | | 25 | 4 | | ±0.5 | | LSB | |

### AC CHARACTERISTICS

| Characteristic | Symbol | Temp | Test level | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | | |
| Clock min. high | $t_{PW1}$ | Full | 4 | 15 | | | ns | |
| Clock min. low | $t_{PW0}$ | Full | 4 | 15 | | | ns | |
| Max. conversion rate | $f_{MAX}$ | Full | 4 | 25 | | | MHz | $A_{IN}$ at FS & 12.5MHz |
| Aperture delay | $t_{AD}$ | 25 | 5 | | 3 | | ns | |
| Output data delay | $t_D$ | 25 | 4 | | 25 | | ns | With standard LSTTL load |
| | | Full | 4 | | 30 | | ns | |
| Output hold time | $t_{HO}$ | 25 | 4 | 5 | | | ns | |
| | | Full | 4 | 5 | | | ns | |
| Aperture Jitter | | 25 | 5 | | 50 | | ps | |
| **Dynamic Performance** | | | | | | | | $f_{CLK}$ = 25MHz |
| Differential non-linearity | DNL | 25 | 1 | -0.85 | ±0.5 | +1 | LSB | $A_{IN}$ at FS & 10MHz |
| Integral non-linearity | INL | 25 | 1 | | ±1 | ±2 | LSB | |
| S/N ratio | SNR | 25 | 4 | | 45 | | dB | $A_{IN}$ = 1.248MHz |
| | | Full | 4 | | 44.5 | | dB | $A_{IN}$ = 1.248MHz |
| | | 25 | 4 | | 44.0 | | dB | $A_{IN}$ = 2.438MHz |
| | | Full | 4 | | 43.5 | | dB | $A_{IN}$ = 2.438MHz |
| | | 25 | 1 | | 43.5 | | dB | $A_{IN}$ = 4.43MHz |
| | | Full | 4 | | 43.0 | | dB | $A_{IN}$ = 4.43MHz |
| Effective No. of bits | ENOB | 25 | 4 | | 7.2 | | bits | $A_{IN}$ = 1.248MHz |
| | | | 4 | | 7.1 | | bits | $A_{IN}$ = 2.438MHz |
| | | | 1 | | 7.0 | | bits | $A_{IN}$ = 4.43MHz |

## ELECTRICAL CHARACTERISTICS DEFINITIONS

### Analog Bandwidth
The analog input frequency, at which the spectral power of the fundamental frequency as determined by Fast Fourier Transform analysis, is 3dB down on the DC level.

### Aperture Delay
The delay between the falling edge of the CONV signal and the instant at which the analog input is sampled.

### Aperture Jitter
The variation between successive samples of the aperture delay.

### Conversion Rate
The maximum rate at which the converter will run.

### Differential Non-Linearity (DNL)
The deviation of any code width from an ideal LSB step.

### Effective Number of Bits (ENOB)
This is a measure of the dynamic performance which is calculated from the following expression.:

$$\text{ENOB} = \frac{\text{SNR-1.76}}{6.02}$$

SNR is the signal-to-noise ratio, in decibels, at the test frequency.

### Integral Non-Linearity (INL)
The deviation of the centre of each code from a reference line which has been determined by a least squares curve fit.

### Output Data Delay
The delay between the 50% point of the rising edge of the CONV signal and the 50% point of any data output change.

### Reference Ladder Offset
The voltage error at the ends of the resistor chain caused by the lead frame and bond wire.

### Signal-to-Noise Ratio (SNR)
The ratio of the RMS signal amplitude to the RMS value of 'noise' which is defined as the sum of all other spectral components including harmonics but excluding DC with a full scale analog input signal.

### Test Levels
**Level 1** - 100% production tested
**Level 2** - 100% production tested at 25°C and sample tested at specified temperatures
**Level 3** - Sample tested only
**Level 4** - Parameter is guaranteed by design and characteristics testing
**Level 5** - Parameter is a typical value only

## CONVERSION TIMING

Operation of the VP1058 requires that an external clock be applied to the CONV (convert) pin. This CONV signal synchronises the sampling, conversion, and output stages of the device as shown in the timing diagram.

The analog input is sampled when the comparator array is latched after a rising edge on the CONV pin. This rising edge also causes the result of the previous sample to be transferred to the outputs. Data at the outputs is latched at the same time as the 255 to 8 encoding of the current sample. Both these operations are performed on the falling edge of the CONV signal. This results in a 'pipeline' delay which means that the digital result of sample 'N' is available for acquisition by external circuitry whilst sample 'N+2' is being taken.

The time interval between a rising edge on the CONV pin and the comparators latching is the aperture delay time ($t_{AD}$). This time may be subject to small variations mainly due to temperature and component matching. The short term uncertainty in the aperture delay time is specified by the aperture jitter (or aperture error). Output data will remain valid for a minimum time after the rising edge of CONV, specified by the output data delay ($t_D$).

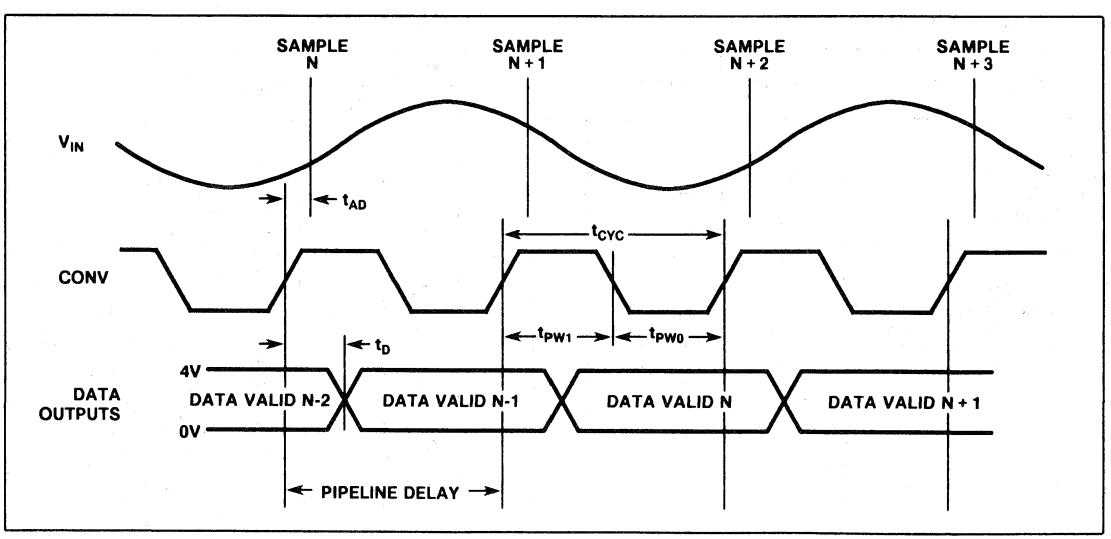



*Fig.3 Timing diagram*

## GENERAL CIRCUIT DESCRIPTION

The VP1058 employs a 'flash' architecture consisting of a reference resistor chain, an array of 256 comparators, encoding logic, and a full 8-bit D-type output latch. The 255 reference levels generated by the resistor chain are compared with the analog input signal by the comparator array. This produces a thermometer code which the encoding logic converts into an 8-bit word. The D-type latch accepts this data and holds the outputs until the next conversion. The format of the output data is determined by the NLINV and NMINV control lines.

### Analog Input

The maximum amplitude and offset of the input is defined by the setting of the two reference voltages $V_{RB}$ and $V_{RT}$. A signal outside this range will cause the output to be either full-scale positive or full-scale negative, depending on whether the signal is off scale in the positive or negative direction.

For optimum performance, the input signal should be biased at +4.0V with a 2V peak-to-peak amplitude. The necessary gain, offset and low impedance drive required for the input signal can be provided by use of a high slew rate ADC driver.

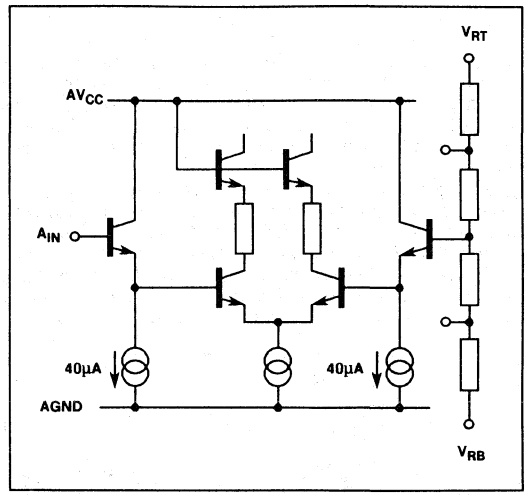



*Fig.4 Analog input*

### Reference Voltage

The reference chain between pins $V_{RB}$ & $V_{RT}$ is formed of 256 series resistors and has a total resistance of approximately 90Ω. A mid-reference pin, $V_{RM}$, is provided for precise setting of the integral linearity, although adjustment is not necessary to meet the data sheet specification.

The VP1058 will convert analog signals in the range $V_{RB} \leq A_{IN} \leq V_{RT}$, where $V_{RB}$ and $V_{RT}$ are in the range +3V to +5V. (The design of the VP1058 has been optimised for $V_{RB}$ = 3V and $V_{RT}$ = 5V.) All reference pins should be adequately decoupled close to the device.

### Output Format

The output data format is controlled by the logic levels at the NLINV and NMINV pins as shown on the output coding table. These inputs are active low and may be tied to $DV_{CC}$ for logic '1' or DGND for logic '0'. Both inputs are considered DC controls and as such should only be altered while the converter is in the steady state.

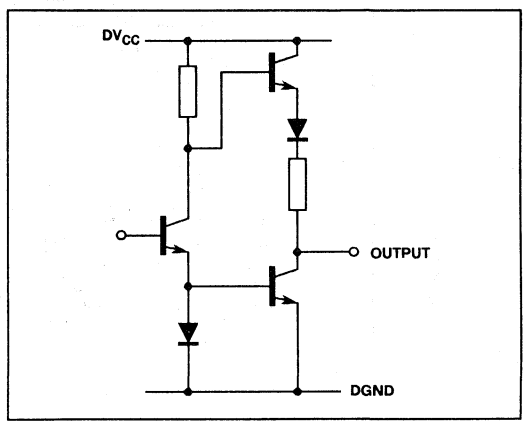



*Fig.5 TTL output stage*

| Code | Input voltage | | Binary | | Offset 2s' complement | |
|---|---|---|---|---|---|---|
| | | | True | Inverted | True | Inverted |
| | 2.0V Full Scale<br>7.8431mV Step | 2.048V Full Scale<br>8.0mV Step | NMINV = 1<br>NLINV = 1 | 0<br>0 | 0<br>1 | 1<br>0 |
| 000 | 5.0V | 5.0V | 0000 0000 | 1111 1111 | 1000 0000 | 0111 1111 |
| 001 | 4.9922V | 4.9920V | 0000 0001 | 1111 1110 | 1000 0001 | 0111 1110 |
| • | • | • | • | • | • | • |
| 127 | 4.0039V | 3.9840V | 0111 1111 | 1000 0000 | 1111 1111 | 0000 0000 |
| 128 | 3.9961V | 3.9760V | 1000 0000 | 0111 1111 | 0000 0000 | 1111 1111 |
| 129 | 3.9882V | 3.9680V | 1000 0001 | 0111 1110 | 0000 0001 | 1111 1110 |
| • | • | • | • | • | • | • |
| 254 | 3.0079V | 2.9680V | 1111 1110 | 0000 0001 | 0111 1110 | 1000 0001 |
| 255 | 3.0V | 2.960V | 1111 1111 | 0000 0000 | 0111 1111 | 1000 0000 |

*Table 1 Output coding*

## APPLICATION NOTES

As with all high speed analog-to-digital converters, careful consideration must be given to circuit layout. The best performance from the VP1058 can be achieved by use of separate analog and digital ground planes. Ideally these should be connected at a point close to the device. This will reduce the amount of digital switching noise fed back into the analog section of the converter, so aiding device performance.

Supply line decoupling is important when dealing with mixed analog and digital signals, as they can provide a feedback path from the digital output currents. Therefore, the VP1058 should be decoupled close to the device supply pins with good quality high frequency, low inductance capacitors. Due to the high clock rates, long clock lines to the device should be avoided to reduce noise pick up.

A typical applications circuit is shown below. The analog input amplifier should be a wideband, high slew rate op-amp used to drive the input directly. A stable reference is needed for both input offset and gain control (e.g. REF12Z micropower voltage reference as shown in Fig. 6). Both analog input pins should be connected close to the device with the input amplifiers feedback loop closed at that point. The reference inputs should be adequately decoupled to ground so as to limit the effects of system noise on conversion accuracy. A capacitor at the mid-reference point (as shown) may be useful in correcting any inherent reference ladder skew.

The circuit will accept a 1V p-p video signal and level shift and multiply it to provide the recommended 2V p-p signal to drive the VP1058.

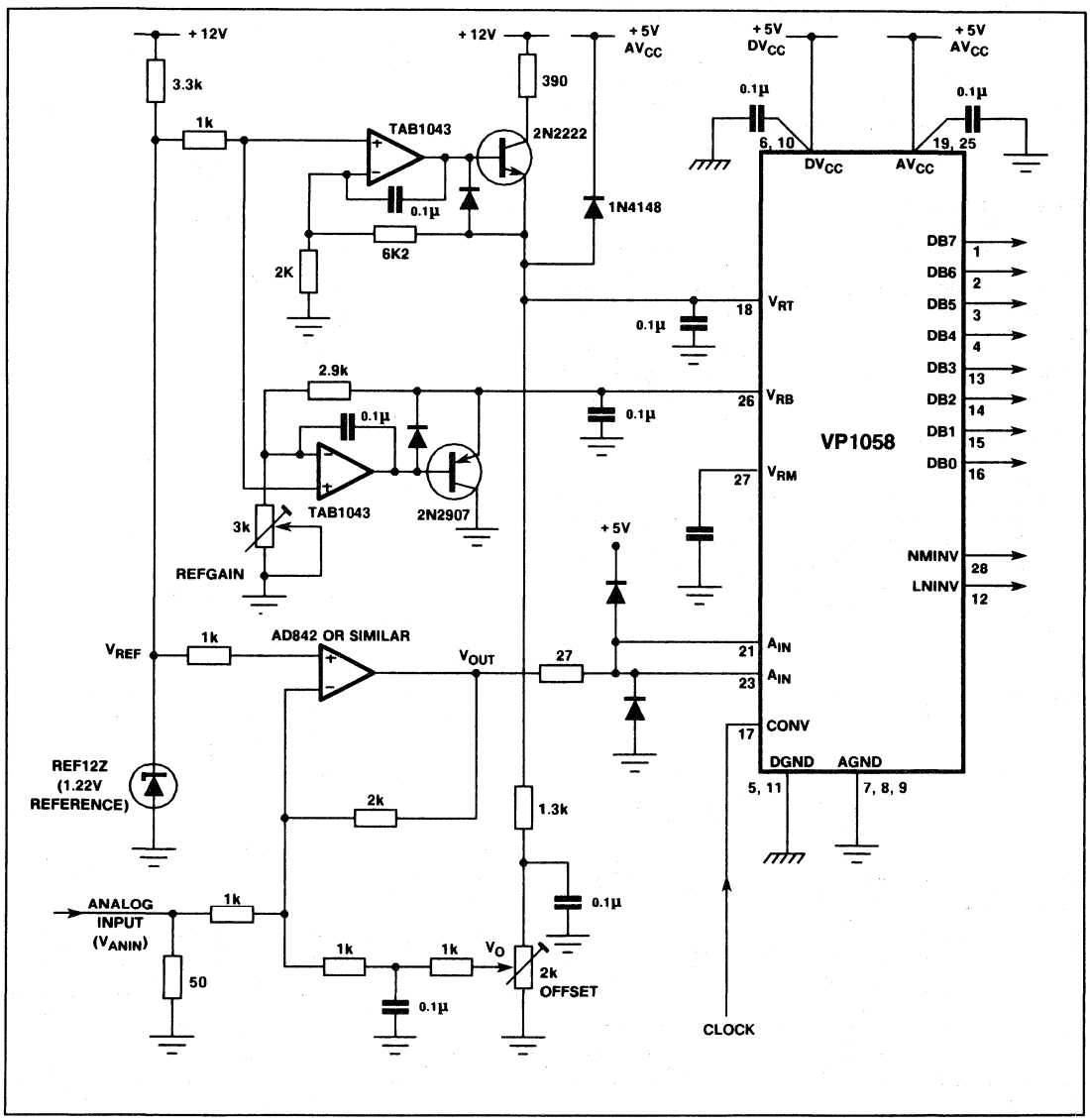



*Fig.6 Typical applications circuit*

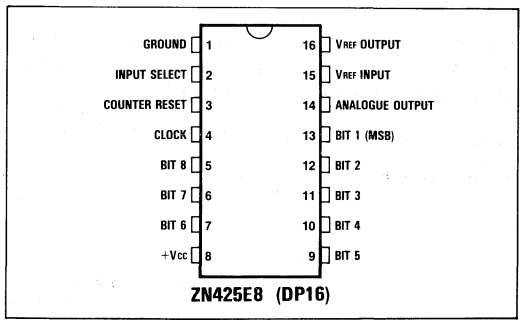
# ZN425E8

## 8-BIT D-A/A-D CONVERTER

The ZN425 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches, and in addition a counter and a 2.5V precision voltage reference. The counter is a powerful addition which allows a precision staircase to be generated very simply by clocking the counter.

### FEATURES

- ±½ LSB Linearity Error
- 0°C to +70°C
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time (D-A) 1µs Typical
- Conversion Time (A-D) 1ms Typical, using Ramp and Compare Technique
- Extra Components Required
  D-A:Reference Capacitor (Direct Voltage Output Through 10kohms Typ.)
  A-D:Comparator, Gate, Clock and Reference Capacitor




**Pin connections - top view**

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| ZN425E 8 | 0°C to +70°C | DP16 |

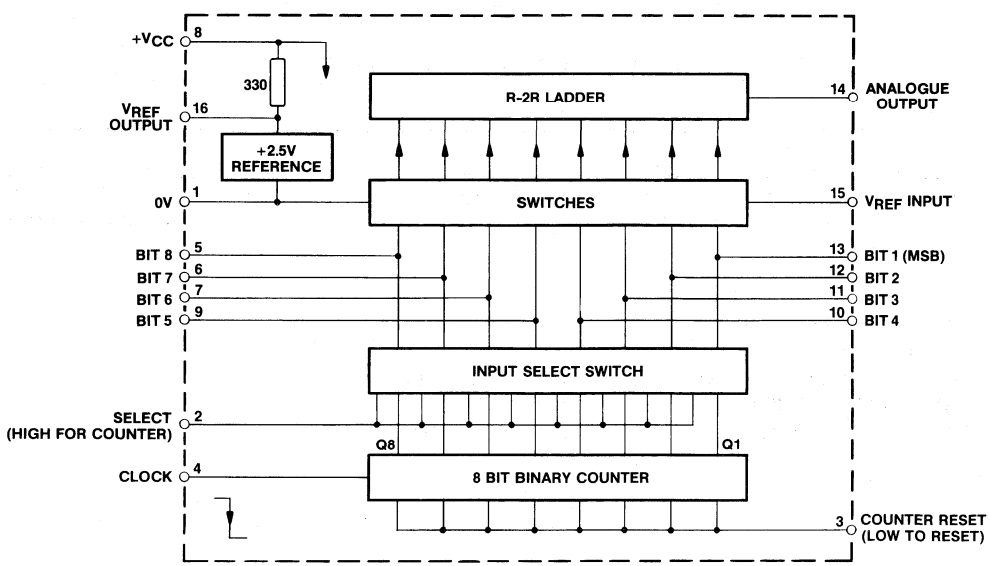



**Fig.1 System diagram**

## INTRODUCTION

The ZN425 is an 8-bit dual mode D-A/A-D converter. It contains an 8-bit D-A converter using an advanced design of R-2R ladder network and an array of precision bipolar switches plus an 8-bit binary counter and a 2.5V precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

By including on the chip an 8-bit binary counter, A-D conversion can be obtained simply by adding an external comparator (ZN424P) and clock inhibit gating (7400).

By simply clocking the counter the ZN425 can be used as a self-contained precision ramp generator.

A logic input select switch is incorporated which determines whether the precision switches accept the outputs from the binary counter or external digital inputs depending upon whether the control signal is respectively high or low.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

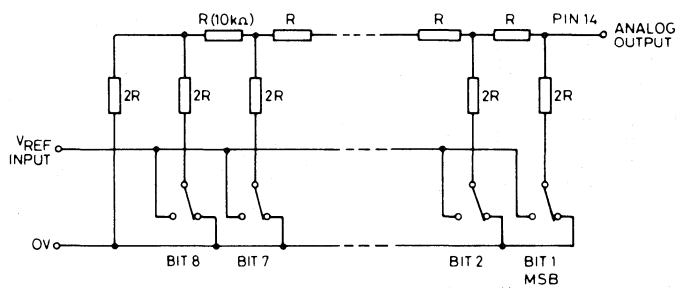



**Fig. 2 The R-2R ladder network**

Each 2R element is connected either to 0V or $V_{REF}$ by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | +7.0V |
| Max. voltage, logic and $V_{REF}$ inputs | +5.5V See note 3 |
| Operating temperature range | 0°C to 70°C |
| Storage temperature range | -55°C to +125°C |

**CHARACTERISTICS** (at $T_{amb} = 25°C$ and $V_{CC} = +5V$ unless otherwise specified)

**Internal voltage reference**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Output voltage | $V_{REF}$ | 2.4 | 2.55 | 2.7 | V | I = 7.5mA (internal) |
| Slope resistance | $R_S$ | – | 2 | 4 | Ω | I = 7.5mA (internal) |
| $V_{REF}$ temperature coefficient | | – | 40 | – | ppm/°C | I = 7.5mA (internal) |

Note: The internal reference requires a 0.22μF stabilising capacitor between pins 1 and 16.

**8-Bit D-A converter and counter**

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Resolution | | 8 | – | – | bits | |
| Non-linearity | | – | – | ±0.5 | LSB | See note 3 |
| Differential non-linearity | | – | ±0.5 | – | LSB | See note 6 |
| Settling time | | – | 1.0 | – | μs | 1LSB step |
| Settling time to 0.5LSB | | – | 1.5 | 2.5 | μs | All bits ON to OFF or OFF to ON |
| Offset voltage ZN425E8 | $V_{OS}$ | – | 3 | 8 | mV | All bits OFF See note 3 |
| Full-scale output | | 2.545 | 2.550 | 2.555 | V | All bits ON Ext. $V_{REF} = 2.56V$ |
| Full-scale temp. coefficient | | – | 3 | – | ppm/°C | Ext. $V_{REF} = 2.56V$ |
| Linearity error temp. coeff. | | – | 7.5 | – | ppm/°C | Relative to F.S.R. |
| Analogue output resistance | $R_o$ | – | 10 | – | kΩ | |
| External reference voltage | | 0 | – | 3.0 | V | |
| Supply voltage | $V_{CC}$ | 4.5 | – | 5.5 | V | See note 3 |
| Supply current | $I_s$ | – | 25 | 35 | mA | |
| High level input voltage | $V_{IH}$ | 2.0 | – | – | V | See notes 1 and 2 |
| Low level input voltage | $V_{IL}$ | – | – | 0.7 | V | |

**CHARACTERISTICS** (cont.)

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| High level input current | $I_{IH}$ | – | – | 10 | μA | $V_{CC}$ = max. $V_I$ = 2.4V |
| | | – | – | 100 | μA | $V_{CC}$ = max. $V_I$ = 5.5V |
| Low level input current bit inputs | $I_{IL}$ | – | – | −0.68 | mA | $V_{CC}$ = max. $V_I$ = 0.3V |
| Low level input current, clock reset and input select | $I_L$ | – | – | −0.18 | mA | |
| High level output current | $I_{OH}$ | – | – | −40 | μA | |
| Low level output current | $I_{OL}$ | – | – | 1.6 | mA | |
| High level output voltage | $V_{OH}$ | 2.4 | – | – | V | $V_{CC}$ = min. Q = 1 $I_{load}$ = −40μA |
| Low level output voltage | $V_{OL}$ | – | – | 0.4 | V | $V_{CC}$ = min., Q = 0 $I_{load}$ = 1.6mA |
| Maximum counter clock frequency | $f_c$ | 3 | 5 | – | MHz | See note 5 |
| Reset pulse width | $t_R$ | 200 | – | – | ns | See note 4 |

Notes:

1. The input select pin (2) must be held low when the bit pins (5, 6, 7, 9, 10, 11, 12 and 13) are driven externally.
2. To obtain counter outputs on bit pins the input select pin (2) should be taken to $+V_{CC}$ via a 1kΩ resistor.
3. (a) Maximum operating voltage. Between 70°C and 125°C the maximum supply voltage is reduced to 5.0V.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
4. The device may be reset by gating from its own counter.
5. $F_{max}$ in A-D mode is 300kHz, see Operating Note 2.
6. Monotonic over full operating temperature range.

If pin 2 is high then the output equals the Q output of the corresponding counter.

If pin 2 is low then the output transistor, Tr1 is held off.

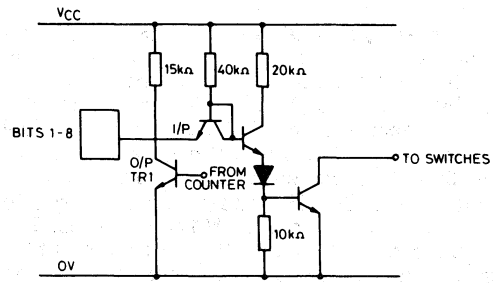



**Fig. 3 Bit inputs/outputs**

## OPERATING NOTES

### 1. 8-bit D-A converter

The ZN425 gives an analogue voltage output directly from pin 14 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the analogue output resistance $R_o$, will be less than 0.004% per °C (or 1LSB/100°C) if $R_L$ is chosen to be $\geqslant 650k\Omega$.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 4 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust $R_2$ until $V_{OUT} = 0.000V$.
ii. Set all bits to ON (high) and adjust $R_1$ until $V_{OUT}$ = Nominal full-scale reading - 1LSB.
iii. Repeat i. and ii.

e.g. Set F.S.R. to +3.840V − 1LSB
= 3.825V

$$(1LSB = \frac{3.84}{256} = 15.0mV)$$

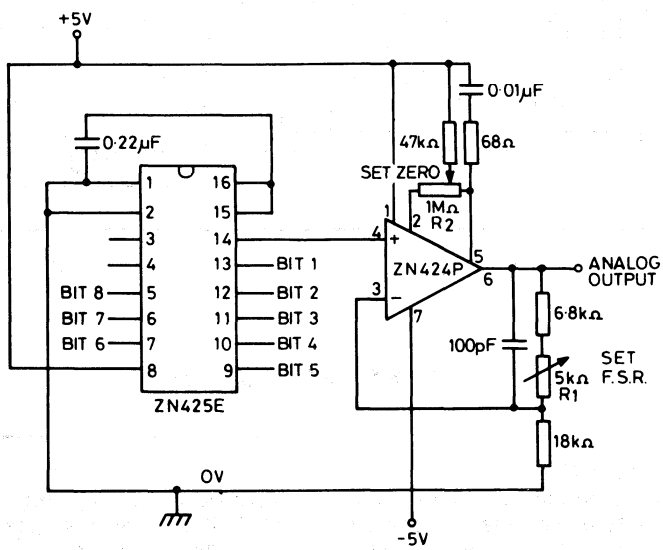



**Fig. 4 8-bit D-A converter**

## 2. 8-bit A-D converter

A counter type ADC can be constructed by adding a voltage comparator and a latch as in Fig. 5. On the negative edge of the CONVERT COMMAND pulse (15$\mu$s minimum) the counter is set to zero and the STATUS latch to logical 1. On the positive edge the gate is opened, enabling clock pulses to be fed to the counter input of the ZN425. The minimum negative clock pulse width to the ZN425 is 100ns. The analogue output of the ZN425 ramps until it equals the voltage on the other input of the comparator. At this point the comparator output goes low and resets the STATUS latch to inhibit further clock pulses. The logical 0 from the status latch indicates that the 8-bit digital output is a valid representation of the analogue input voltage.

A small capacitor of 47pF is added to the ZN425 output to stop any positive going glitches prematurely resetting the status latch. This capacitance is in parallel with the ZN425 output capacitance (20-30pF) and they form a time constant with the ZN425 output resistance (10k$\Omega$). This time constant is the main limit to the maximum clock frequency. With a fast comparator the clock frequency can be up to 300kHz. Using the ZN424P as a comparator the clock frequency should be restricted to 100kHz. The conversion time varies with the input being a maximum for full-scale input.

Maximum conversion time =

$$\frac{256}{\text{clock frequency in Hz}} \text{ seconds}$$

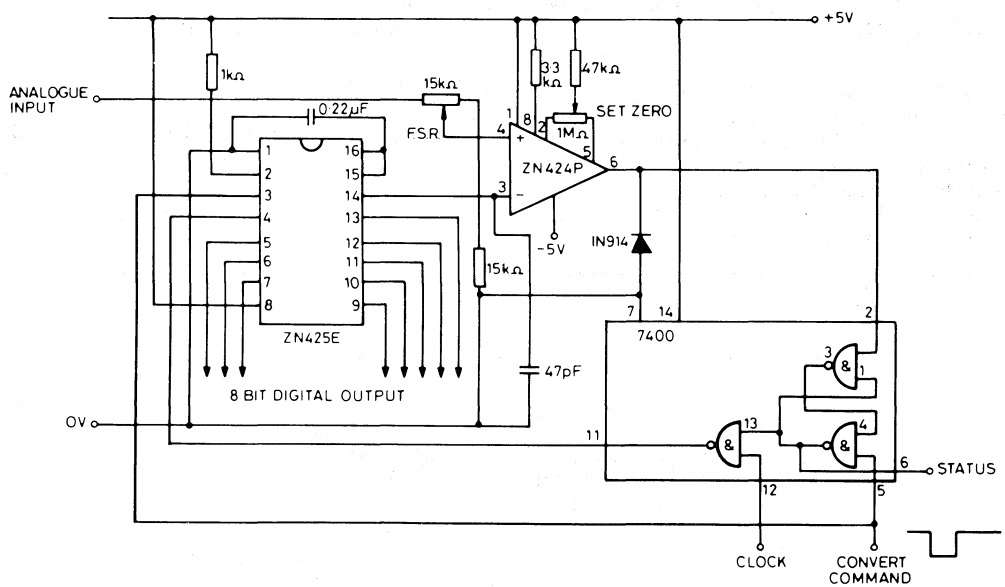



**Fig. 5 8-bit A-D converter**

## 3. Precision ramp generator

The inclusion of an 8-bit binary counter on the chip gives the ZN425 a useful ramp generator function. The circuit, Fig. 6, uses the same buffer stages as the D-A converter. The calibration procedure is also the same. Holding pin 2 low will set all bits to ON and if RESET is taken low with pin 2 high all the bits are turned OFF. If the end voltages of the ramp are not required to be set accurately then the buffer stage could be omitted and the voltage ramp will appear directly at pin 14.

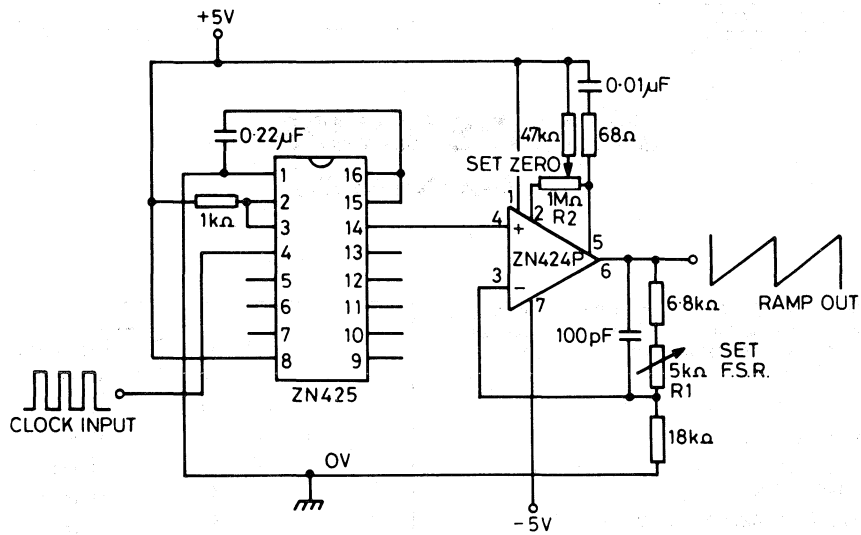



Fig. 6 Precision ramp generator

## 4. Alternative output buffer using the 741

The following circuit, employing the 741 operational amplifier, may be used as the output buffer for both the 8-bit D-A converter (Fig.4) and the precision ramp generator (Fig.6).

## 5. Further applications

Details of a wide range of additional applications, described in the Application Notes section.

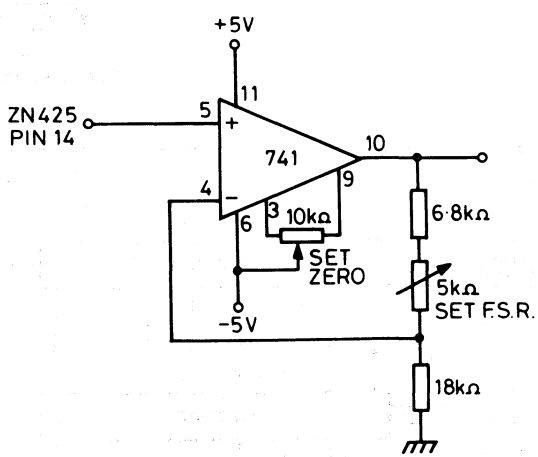



Fig. 7 The ZLD741 as output buffer

# ZN426E8/ZN426D

## 8-BIT D-A CONVERTER

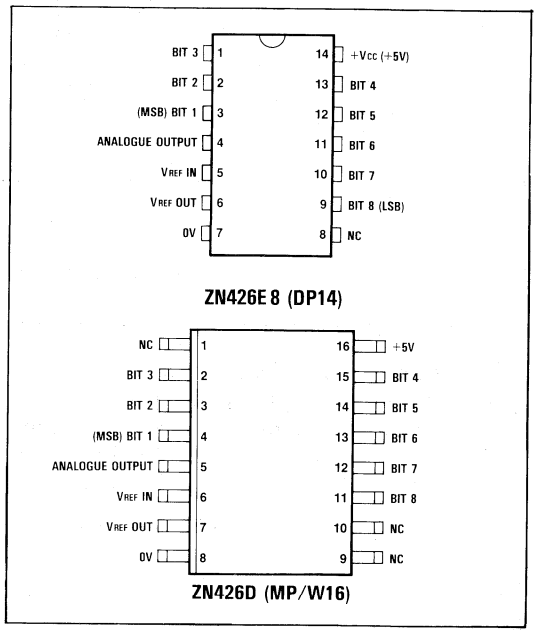
The ZN426 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches and a 2.5V precision voltage reference.

### FEATURES

- ±½ LSB Linearity Error
- Guaranteed Monotonic over the Full Operating Temperature Range
- 0°C to +70°C (ZN426E8. ZN426D)
- TTL and 5V CMOS Compatible
- Single +5V Supply
- Settling Time 1 microsecond Typical
- Only Reference Capacitor and Resistor Required

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| ZN426D | 0°C to +70°C | MP16W |
| ZN426E-8 | 0°C to +70°C | DP14 |




**Pin connections - top view**

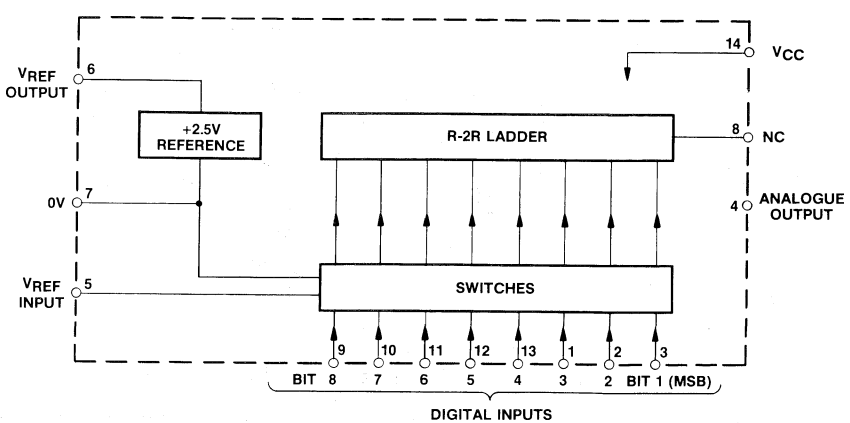



**Fig.1 System diagram**

## INTRODUCTION

The ZN426 is an 8-bit D-A converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches plus a 2.5V precision voltage reference all on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The use of the on-chip reference voltage is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. In this case there is no need to supply power to the internal reference so $R_{REF}$ and $C_{REF}$ can be omitted

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

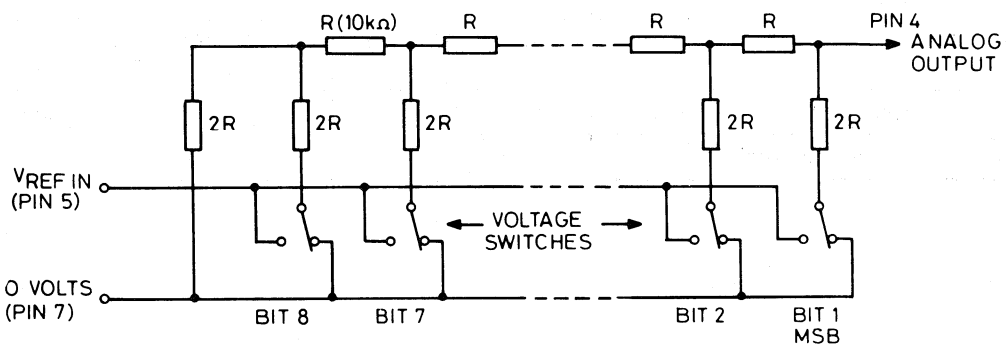



**Fig. 2 The R-2R ladder network**

Each 2R element is connected either to 0V or $V_{REF}$ by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | +7.0V |
| Max. voltage, logic and $V_{REF}$ inputs | +5.5V |
| Operating temperature range | 0°C to 70°C (ZN426E 8, ZN426D) |
| Storage temperature range | -55°C to +125°C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5V, $T_{amb}$ = 25°C unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Converter** Resolution | | 8 | – | – | bits | |
| Non-linearity | | – | – | ±0.5 | LSB | |
| Differential non-linearity | | – | ±0.5 | – | LSB | Note 1 |
| Settling time to 0.5LSB | | – | 1.0 | – | μs | 1LSB step |
| Settling time to 0.5LSB | | – | 2.0 | – | μs | All bits ON to OFF or OFF to ON |
| Offset voltage ZN426E8 and D | $V_{OS}$ | – | 3.0 | 5.0 | mV | All bits OFF |
| $V_{OS}$ temperature coefficient | | – | 5 | – | μV/°C | |
| Full-scale output | | 2.545 | 2.550 | 2.555 | V | All bits ON Ext. $V_{REF}$ = 2.560V |
| Full-scale temp. coefficient | | – | 3 | – | ppm/°C | Ext. $V_{REF}$ = 2.560V |
| Non-linearity temp. coefficient | | – | 7.5 | – | ppm/°C | Relative to F.S.R. |

Notes

1. Monotonic over full temperature range.

**ELECTRICAL CHARACTERISTICS** (cont.)

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Analogue output resistance | $R_o$ | – | 10 | – | kΩ | |
| External reference voltage | | 0 | – | 3.0 | V | |
| Supply voltage | $V_{CC}$ | 4.5 | – | 5.5 | V | |
| Supply current | $I_s$ | – | 5 | 9 | mA | |
| High level input voltage | $V_{IH}$ | 2.0 | – | – | V | |
| Low level input voltage | $V_{IL}$ | – | – | 0.7 | V | |
| High level input current | $I_{IH}$ | – | – | 10 | μA | $V_{CC}$ = max. $V_I$ = 2.4V |
| | | – | – | 100 | μA | $V_{CC}$ = max. $V_I$ = 5.5V |
| Low level input current | $I_{IL}$ | – | – | −0.18 | mA | $V_{CC}$ = max. $V_I$ = 0.3V |
| **Internal voltage reference** Output voltage | $V_{REF}$ | 2.475 | 2.55 | 2.626 | V | Note* $R_{REF}$ = 390Ω |
| Slope resistance | $R_s$ | – | 1 | 2 | Ω | $R_{REF}$ = 390Ω |
| $V_{REF}$ temperature coefficient | | – | 40 | – | ppm/°C | $R_{REF}$ = 390Ω |

NOTE*
The internal reference requires a 1μF stabilising capacitor between $V_{REF\ OUT}$ and 0V and a 390Ω resistor, $R_{REF}$, between $V_{CC}$ and $V_{REF\ OUT}$.

## APPLICATIONS

### 8-bit D-A converter

The ZN426 gives an analogue voltage output directly from pin 4 therefore the usual current to voltage converting amplifier is not required. The output voltage drift, due to the temperature coefficient of the analogue output resistance $R_o$, will be less than 0.004% per °C (or 1LSB/100°C) if $R_L$ is chosen to be ⩾650kΩ.

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Fig. 3 shows a typical scheme using the internal reference voltage. To minimise temperature drift in this and similar applications the source resistance to the inverting input of the operational amplifier should be approximately 6kΩ. The calibration procedure is as follows:

i. Set all bits to OFF (low) and adjust $R_2$ until $V_{OUT}$ = 0.000V.

ii. Set all bits to ON (high) and adjust $R_1$ until $V_{OUT}$ = Nominal full-scale reading - 1LSB.

iii. Repeat i. and ii.

e.g.

Set F.S.R. to +3.840V − 1LSB = 3.825V

$$(1LSB = \frac{3.84}{256} = 15.0mV)$$

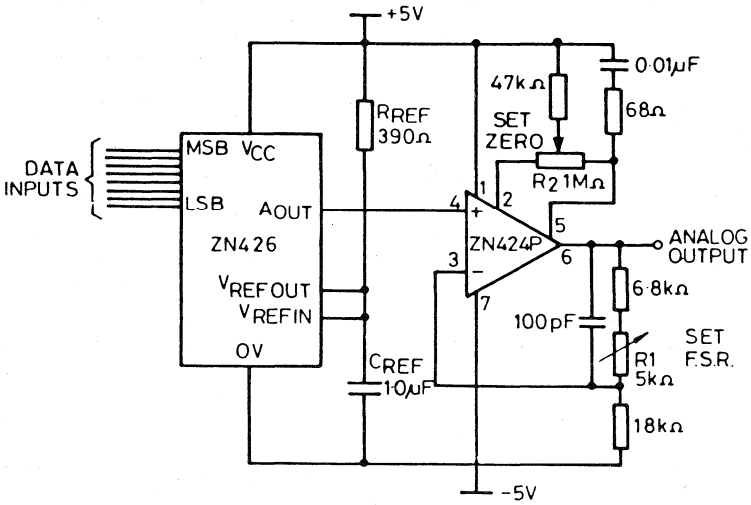



Fig. 3 8-bit D-A converter

**Alternative output buffer using the 741**

The circuit of Fig.4, employing the 741 operational amplifier, may be used as the output buffer.

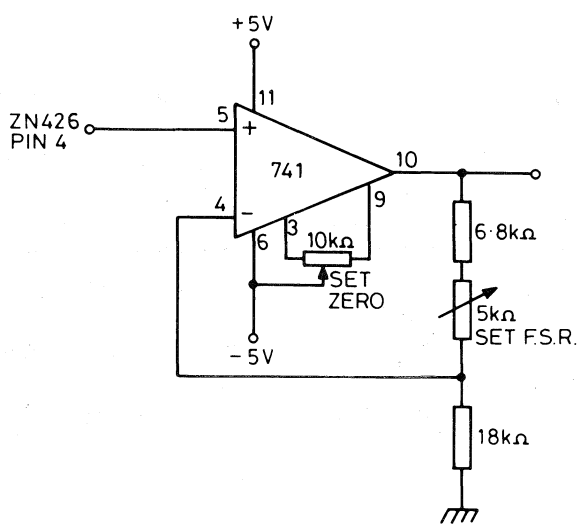



Fig.4 The 741 as output buffer

3006-1.0

# ZN427E8 / ZN427J8

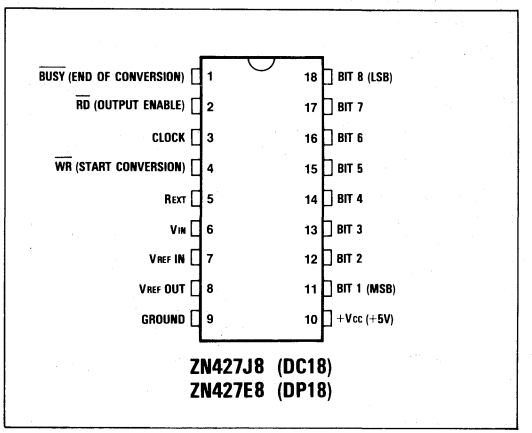
## MICROPROCESSOR COMPATIBLE 8-BIT SUCCESSIVE APPROXIMATION A-D CONVERTER

The ZN427 is an 8-bit successive approximation converter with three-state outputs to permit easy interfacing to a common data bus. The IC contains a voltage switching DAC, a fast comparator, successive approximation logic and a 2.56V precision bandgap reference, the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted, thus allowing ratiometric operation.

Only passive external components are required for operation of the converter.

### FEATURES

- Easy Interfacing to Microprocessor, or Operates as a 'Stand-Alone' Converter
- Fast: 10 microseconds Conversion Time Guaranteed
- No Missing Codes over Operating Temperature Range
- Data Outputs Three-State TTL Compatible, other Logic Inputs and Outputs TTL and CMOS Compatible
- Choice of On-Chip or External Voltage Reference
- Ratiometric Operation
- Unipolar and Bipolar Input Ranges
- Complementary to ZN428 DAC
- Commerical or Military Temperature Ranges




**Pin connections - top view**

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| ZN427E-8 | 0°C to +70°C | DP18 |
| ZN427J-8 | -55°C to +125°C | DC18 |

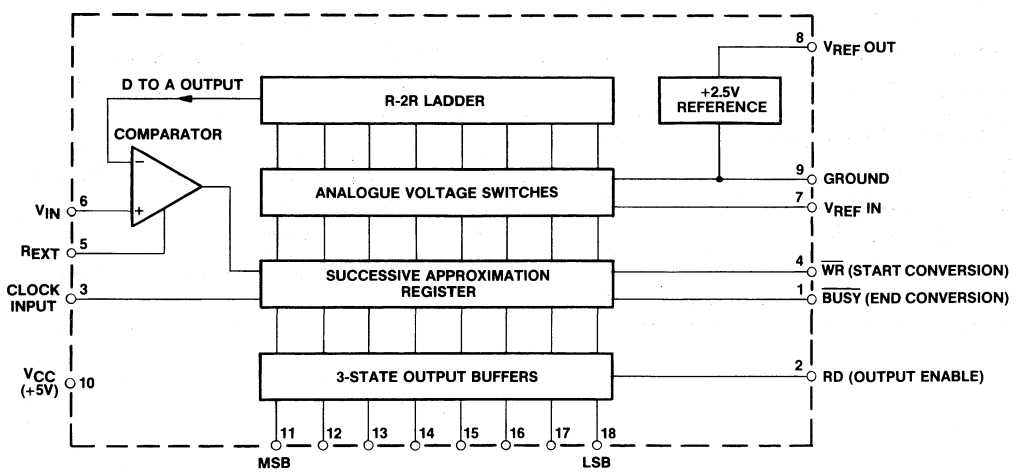



**Fig.1 System diagram**

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | +7.0V |
| Max. voltage, logic and $V_{REF}$ inputs | $+V_{CC}$ |
| Operating temperature range | 0°C to 70°C (ZN427E8)<br>-55°C to +125°C (ZN427J8) |
| Storage temperature range | -55°C to +125°C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = 5V, $T_{amb}$ = 25°C unless otherwise specified).

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **Converter** | | | | | |
| Resolution | 8 | – | – | Bits | |
| Linearity error | – | – | ±0.5 | LSB | |
| Differential non-linearity | – | ±0.5 | – | LSB | |
| Linearity error T.C. | – | ±3 | – | ppm/°C | |
| Differential non-linearity T.C. | – | ±6 | – | ppm/°C | |
| Full-scale (gain) T.C. | – | ±2.5 | – | ppm/°C | External Ref. 2.5V |
| Zero T.C. | – | ±8 | – | µV/°C | |
| Zero transition 00000000 to 00000001 | 12 | 15 | 18 | mV | $V_{REF\ IN}$ = 2.560V |
| F.S. transition 11111110 to 11111111 | 2.545 | 2.550 | 2.555 | V | $V_{REF\ IN}$ = 2.560V |
| Conversion time | – | – | 10 | µs | See note 1 |
| External reference voltage | 1.5 | – | 3.0 | V | |
| Supply voltage ($V_{CC}$) | 4.5 | – | 5.5 | V | |
| Supply current | – | 25 | 40 | mA | |
| Power consumption | – | 125 | – | mW | |
| **Comparator** | | | | | |
| Input current | – | 1 | – | µA | $V_{IN}$ = 3V, $R_{EXT}$ = 82kΩ |
| Input resistance | – | 100 | – | kΩ | $V_-$ = −5V |
| Tail current, $I_{EXT}$ | 25 | – | 150 | µA | |
| Negative supply, V− | −3.0 | – | −30.0 | V | See comparator |
| Input voltage | −0.5 | – | 3.5 | V | (page 2-26) |
| **Internal voltage reference** | | | | | |
| Output voltage | 2.475 | 2.560 | 2.625 | V | $R_{REF}$ = 390Ω, $C_{REF}$ = 4µ7 |
| Slope resistance | – | 0.5 | 2 | Ω | |
| $V_{REF}$ temperature coefficient | – | 50 | – | ppm/°C | |
| Reference current | 4 | – | 15 | mA | See reference (page 2-25) |

**ELECTRICAL CHARACTERISTICS** (Cont.)

| | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **Logic** (over specified operating temperature range) | | | | | |
| High level input voltage $V_{IH}$ | 2.0 | – | – | V | |
| Low level input voltage $V_{IL}$ | – | – | 0.8 | V | |
| High level input current, | – | – | 50 | μA | $V_{IN} = 5.5V$, $V_{CC} = max.$ |
| $\overline{WR}$ and RD inputs $I_{IH}$ | – | – | 15 | μA | $V_{IN} = 2.4V$, $V_{CC} = max.$ |
| High level input current, | – | – | 100 | μA | $V_{IN} = 5.5V$, $V_{CC} = max.$ |
| Clock input $I_{IH}$ | – | – | 30 | μA | $V_{IN} = 2.4V$, $V_{CC} = max.$ |
| Low level input current $I_{IL}$ | – | – | −5 | μA | $V_{IN} = 0.4V$, $V_{CC} = max.$ |
| High level output current $I_{OL}$ | – | – | −100 | μA | |
| Low level output current $I_{OL}$ | – | – | 1.6 | mA | |
| High level output voltage $V_{OH}$ | 2.4 | – | – | V | $I_{OH} = max.$, $V_{CC} = min.$ |
| Low level output voltage $V_{OL}$ | – | – | 0.4 | V | $I_{OL} = max.$, $V_{CC} = min.$ |
| Disabled output leakage | – | – | 2 | μA | $V_O = 2.4V$ |
| Input clamp diode voltage | – | – | −1.5 | V | |
| Read input to data output | – | – | 250 | ns | See Fig. 8 |
| Enable/disable delay time $t_{RD}$ | – | 180 | 250 | ns | |
| Start pulse width $t_{WR}$ | 250 | 160 | – | ns | See Fig. 8 |
| $\overline{WR}$ to $\overline{BUSY}$ propagation delay $t_{BD}$ | – | – | 250 | ns | |
| Clock pulse width | 500 | – | – | ns | |
| Maximum clock frequency | 900 | 1000 | – | kHz | See note 1 |

Note 1 A 900kHz clock gives a conversion time of 10μs (9 clock periods).

## GENERAL CIRCUIT OPERATION

The ZN427 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF/2}$ from the DAC. This is compared to the input voltage $V_{IN}$; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2} > V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$. Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to $V_{IN}$ and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the ninth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the RD input will normally be held low to keep the three-state buffers in their high impedance state. Data can be read out by taking RD high, thus enabling the three-state outputs. Readout is non-destructive. The $\overline{BUSY}$ output may be tied to the RD input to automatically enable the outputs when the data is valid.

For reliable operation of the converter the start pulse applied to the $\overline{WR}$ input must meet certain timing criteria with respect to the converter clock. These are detailed in the timing diagram of Fig. 2.

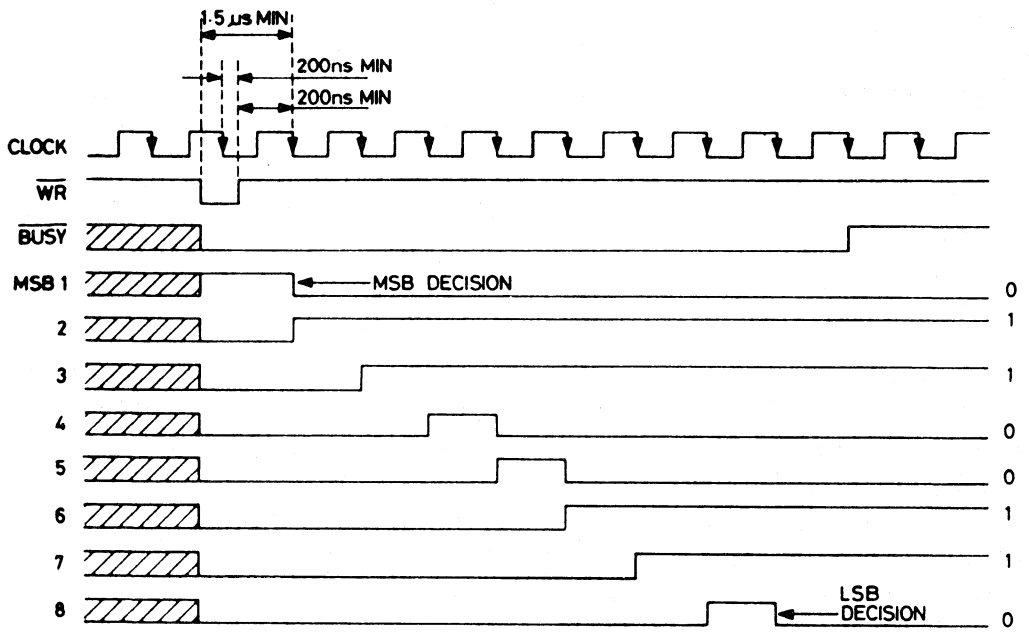



Fig. 2 Timing diagram

## NOTES ON TIMING DIAGRAM

1. A conversion sequence is shown for the digital word 01100110. For clarity the three-state outputs are shown as being enabled during the conversion, but normal practice would be to disable them until the conversion was complete.

2. The $\overline{BUSY}$ output goes low during a conversion. When $\overline{BUSY}$ goes high at the end of a conversion the output data is valid. In a microprocessor system the $\overline{BUSY}$ output can be used to generate an interrupt request when the conversion is complete.

3. In the timing diagram cross hatching indicates a 'don't care' condition.

4. The start pulse operates as an asynchronous (independent of clock) reset that sets the MSB output to 1 and sets all other outputs and the end of conversion flag to 0. This resetting occurs on the low-going edge of the start pulse and as long as $\overline{WR}$ is low the converter is inhibited. Conversion commences on the first active (negative going) clock edge after the $\overline{WR}$ input has gone high again, when the MSB decision is made. A number of timing constraints thus apply to the start pulse.

(a) The minimum duration of the start pulse is 250ns, to allow reliable resetting of the converter logic circuits.

(b) There is no limit to the maximum duration of the start pulse.

(c) To allow the MSB to settle at least 1.5μs must elapse between the negative going edge of the start pulse and the first active clock edge that indicates the MSB desicion.

(d) To ensure reliable clocking the positive-going edge of the start pulse should not occur within 200ns of an active (negative-going) clock edge. The ideal place for the positive-going edge of the start pulse is coincident with a positive-going clock edge. As a special case of the above conditions the start pulse may be synchronous with a negative-going clock pulse.

## PRACTICAL CLOCK AND SYNCHRONISING CIRCUITS

The actual method of generating the clock signal and synchronising it to the start conversion pulse (or vice versa) will depend on the system in which the ZN427 is incorporated.

When used with a microprocessor the ZN427 can be treated as RAM and can be assigned a memory address using an address decoder. If the μP clock is used to drive the ZN427 and the μP write pulse meets the ZN427 timing criteria with respect to the μP clock then generating the start pulse is simply a matter of gating the decoded address with the microprocessor write pulse. Whilst the conversion is being performed the microprocessor can perform other instructions or No operation (NOP). When the conversion is complete the outputs can be enabled onto the bus by gating the decoded address with the read pulse. A timing diagram for this sequence of operation is given in Fig. 3.

An advantage of using the microprocessor clock is that the conversion time is known precisely in terms of machine cycles. The data outputs may therefore be read after a fixed delay of at least nine clock cycles after the end of the $\overline{WR}$ pulse, when the conversion will be complete.

Alternatively the read operation may be initiated by using the $\overline{BUSY}$ output to generate an interrupt request.

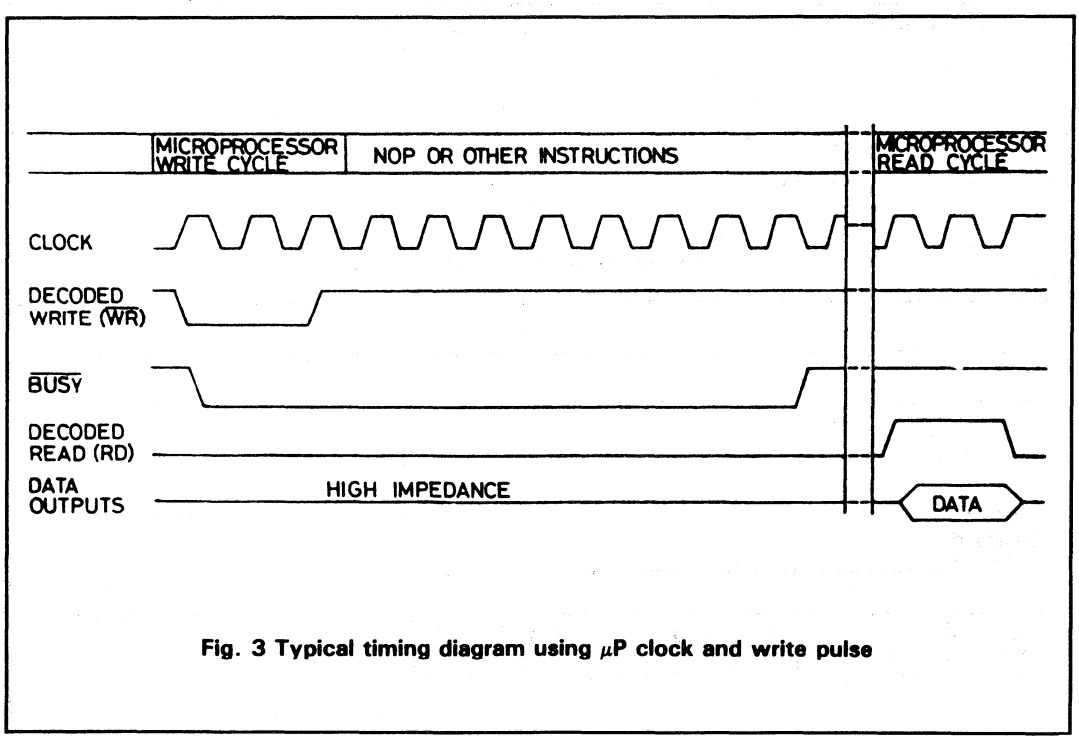



**Fig. 3 Typical timing diagram using μP clock and write pulse**

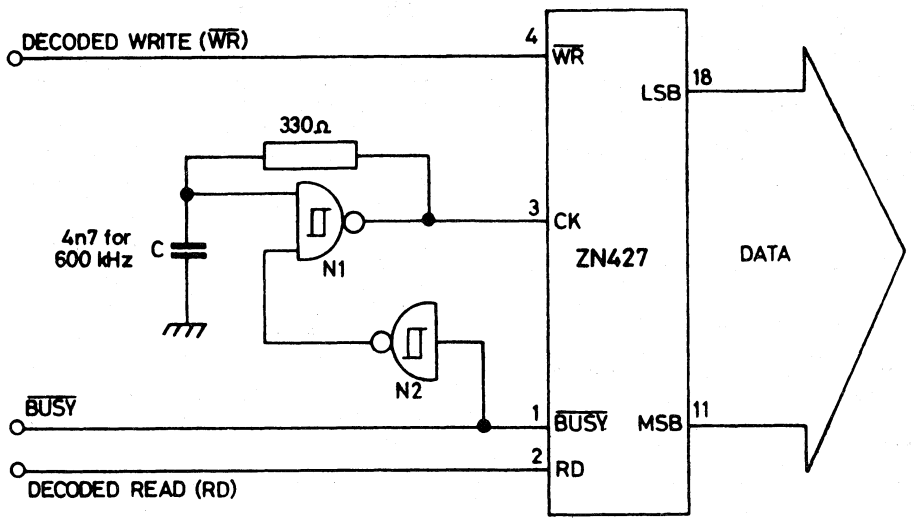
In some systems, for example single-chip microcomputers such as the 8048, this simple method may not be feasible for one or more of the following reasons:

(a) The MPU clock is not available externally.

(b) The clock frequency is too high.

(c) The write pulse timing criteria make it unsuitable for direct use as a start conversion pulse.

If any of these conditions apply then the self-synchronising clock circuit of Fig. 4a is recommended.




N1 N2 = 7413 or ½ 74132 Schmitt trigger

$f_{CK} = \frac{1}{360.C}$ (Hz, F)

Fig. 4a Self-synchronising clock circuit

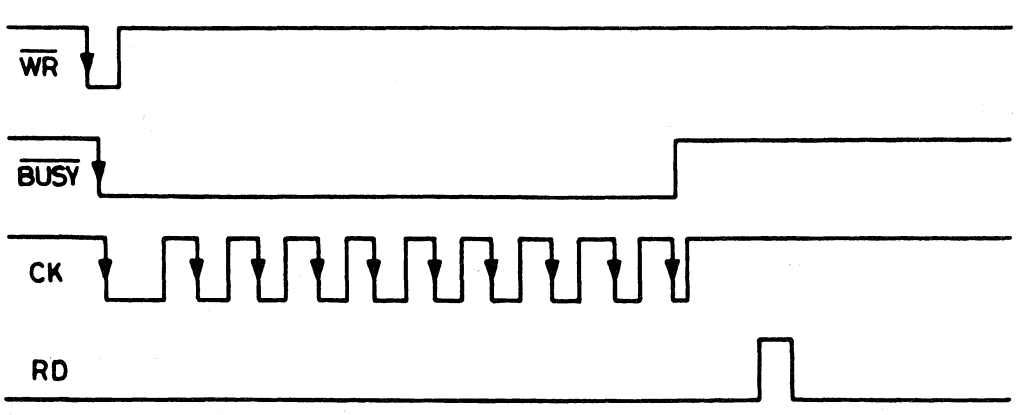



Fig. 4b Timing diagram for circuit of Fig. 4a

N1 is connected as an astable multivibrator which, when the $\overline{BUSY}$ output is high, is inhibited by the output of N2 holding one of its inputs low. The start conversion pulse resets the $\overline{BUSY}$ flag and N1 begins to oscillate. When the conversion is complete $\overline{BUSY}$ goes high and the clock is inhibited.

Since the start pulse starts the clock it may occur at any time. The only constraints on the start pulse are that it must be longer than 250ns but at least 200ns shorter than the first clock pulse. The first clock pulse is in fact longer than the rest since C1 starts from a fully charged condition whereas on subsequent cycles it changes between the upper and lower thresholds ($V_{T+}$ and $V_{T-}$) of the Schmitt trigger.

## LOGIC INPUTS AND OUTPUTS

The logic inputs of the ZN427 utilise the emitter-follower configuration shown in Fig. 5. This gives extremely low input currents for CMOS as well as TTL compatibility.

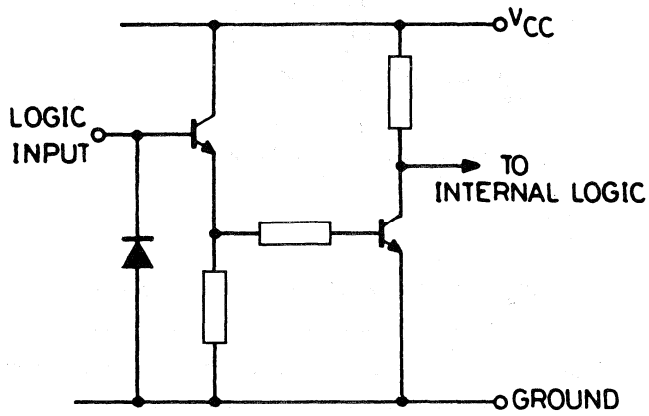
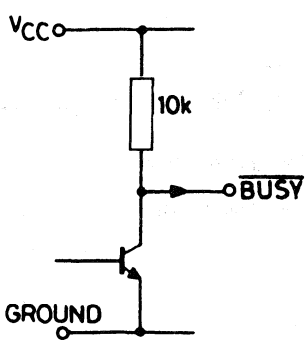



**Fig. 5 Equivalent circuit of all inputs**

The $\overline{BUSY}$ output, shown in Fig. 6, utilises a passive pullup for CMOS/TTL compatibility.




The data outputs have three-state buffers, an equivalent circuit of which is shown in Fig. 7. Whilst the RD input is low both output transistors are turned off and the output is in a high impedance state. When RD is high the data output will assume the appropriate logic state (0 or 1).

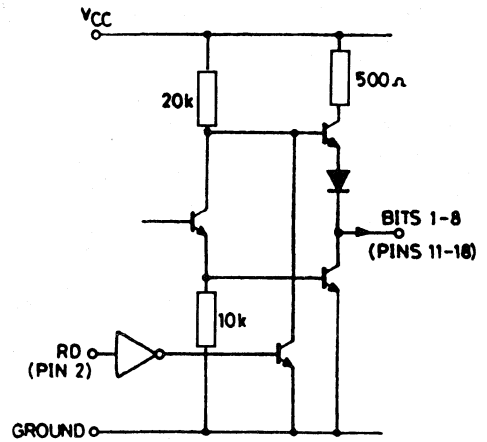



Fig. 7 Equivalent circuit of data outputs

A test circuit and timing diagram for the output enable/disable delays are given in Fig. 8.

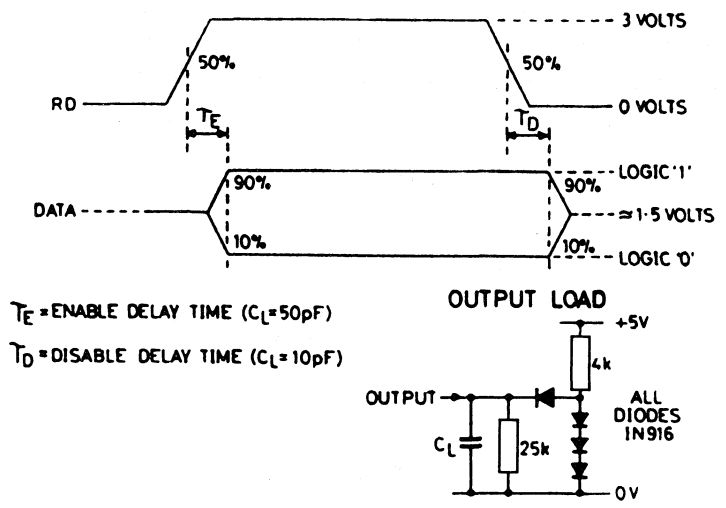



Fig. 8 Output enable/disable waveforms

## ANALOG CIRCUITS

### D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 9. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (< 1mV).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D-A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the successive approximation register.

$V_{OS}$ is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of $V_{OS}$ is typically 2mV for the ZN427E8 and 4mV for the ZN427J8.

This offset will normally be removed by the setting-up procedure and, since the offset temperature coefficient is low (8μV/°C), the effect on accuracy will be negligible.

The D-A output range can be considered to be 8-$V_{REF}$IN through an output resistance R (4kΩ).

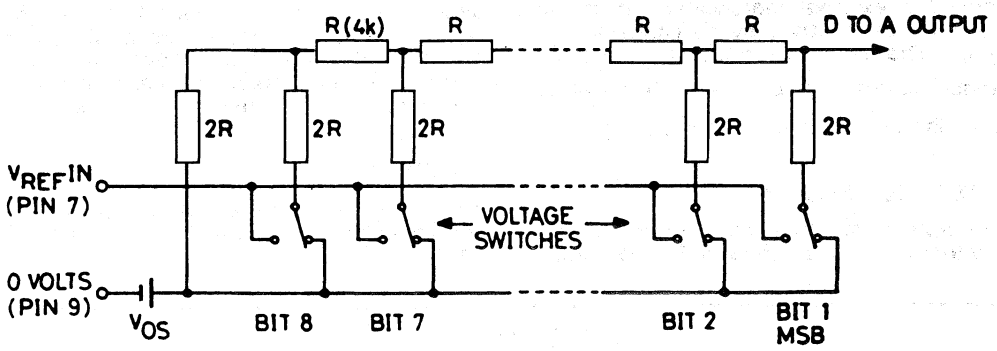



**Fig. 9 R-2R ladder network**

### REFERENCE

#### (a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 10). A resistor ($R_{REF}$), should be connected between pins 8 and 10. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor $C_{REF}$(4μ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (pin 8) is connected to $V_{REF\ IN}$ (pin 7).

Up to five ZN427's may be driven from one internal reference, there being no need to reduce $R_{REF}$. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

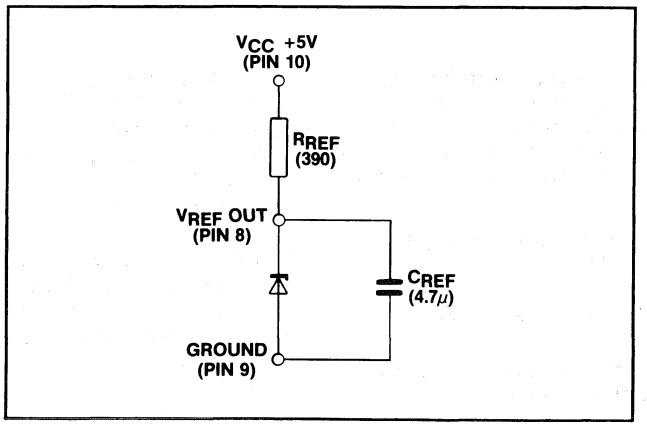



Fig.10 Internal voltage reference

**(b) External reference**

If required an external reference voltage in the range +1.5 to +3.0V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5}{n}\ \Omega$, where n is the number of converters supplied.

## RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN427 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN427 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

## COMPARATOR

The ZN427 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 11.

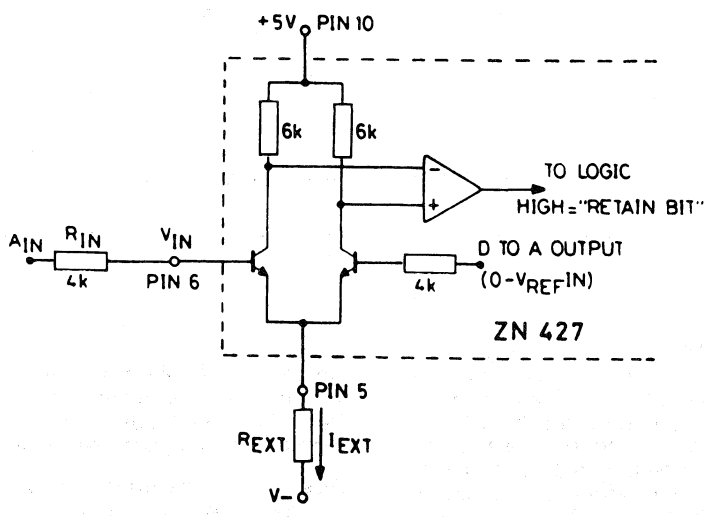



Fig. 11 Comparator equivalent circuit

The comparator derives the tail current, $I_{EXT}$, for its first stage from an external resistor, $R_{EXT}$, which is taken to a negative supply V−.

This arrangement allows the ZN427 to work with any negative supply in the range −3 to −30 volts. The ZN427 is designed to be insensitive to changes in $I_{EXT}$ from 25μA to 150μA. The suggested nominal value of $I_{EXT}$ is 65μA and a suitable value for $R_{EXT}$ is given by $R_{EXT} = |V_-|15k\Omega$.

| V_ (volts) | $R_{EXT}$ (±10%) |
|---|---|
| −3 | 47kΩ |
| −5 | 82kΩ |
| −10 | 150kΩ |
| −12 | 180kΩ |
| −15 | 220kΩ |
| −20 | 330kΩ |
| −25 | 390kΩ |
| −30 | 470kΩ |

The output from the D-A converter is connected through the 4kΩ ladder resistance to one side of the comparator. The analogue input to be converted could be connected directly to the other comparator input ($V_{IN}$, pin 6) but for optimum stability with temperature the analogue input should be applied through a source resistance ($R_{IN} = 4k\Omega$) to match the ladder resistance.

## ANALOGUE INPUT RANGES

The basic connection of the ZN427 shown in Fig. 12 has an analogue input range 0 to $V_{REF\ IN}$, which, in some applications, may be made available from previous signal conditioning/scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analogue input range so that the comparator always sees a positive input voltage.

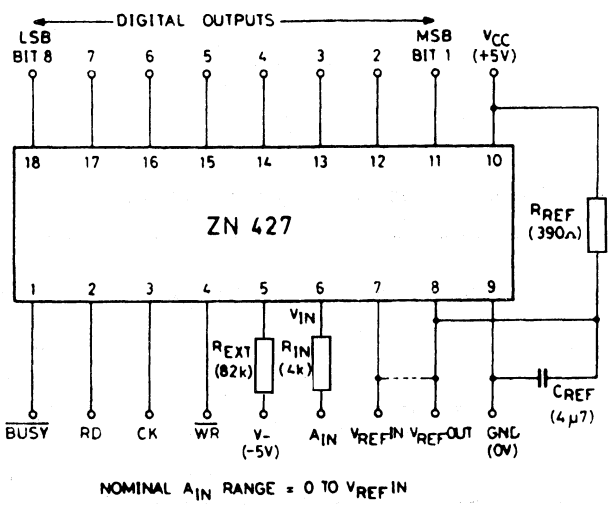



**Fig. 12 External components for basic operation**

## UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig. 13.

The values of $R_1$ and $R_2$ are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input ($A_{IN}$) is at full-scale. The resulting full-scale range is given by

$$A_{IN}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

To match the ladder resistance R1//R2 ($\approx R_{IN}$) = 4kΩ.

The required nominal values of $R_1$ and $R_2$ are given by $R_1 = 4G$ kΩ, $R_2 = \frac{4G}{G-1}$ kΩ

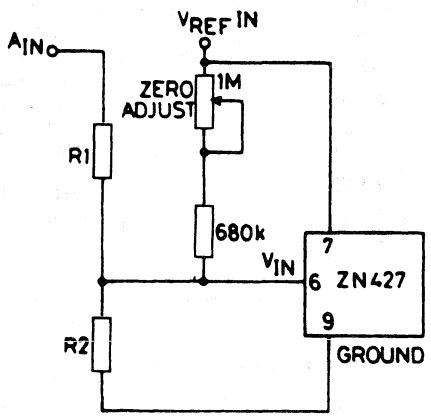



Fig. 13 Unipolar operation - general connection

Using these relationships a table of nominal values of $R_1$ and $R_2$ can be constructed for $V_{REF\ IN} = 2.5$ volts.

| Input range | G | $R_1$ | $R_2$ |
|---|---|---|---|
| + 5V | 2 | 8kΩ | 8kΩ |
| + 10V | 4 | 16kΩ | 5.33kΩ |

## GAIN ADJUSTMENT

Due to tolerances in $R_1$ and $R_2$, tolerances in $V_{REF}$ and the gain (full-scale) error of the DAC, some adjustment should be incorporated into $R_1$ to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting $R_1$ by at least + 5% of its nominal value is suggested.

## ZERO ADJUSTMENT

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which corresponds to + 1½LSB with a 2.56V reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of + ½LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1½ times $V_{REF\ IN}$.

Practical circuit values for + 5 and + 10V input ranges are given in Fig. 14, which incorporate both zero and gain adjustments.

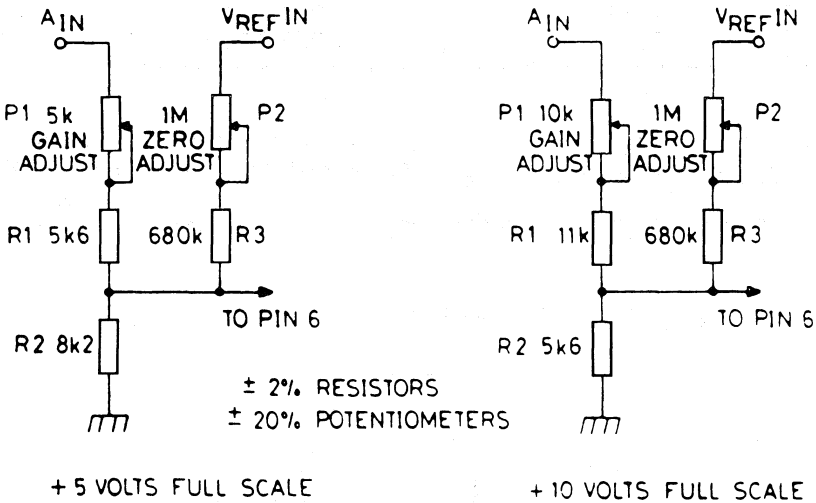



**Fig. 14 Unipolar operation - component values**

## UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous SC pulses at intervals long enough to allow complete conversion and monitor the digital outputs.

(ii) Apply full-scale minus 1½LSB to $A_{IN}$ and adjust gain until bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply ½LSB to $A_{IN}$ and adjust zero until bit 8 just flickers between 0 and 1 with all other bits at 0.

## UNIPOLAR SETTING UP POINTS

| Input range, + FS | ½LSB | FS - 1½LSB |
|---|---|---|
| + 5V | 9.8mV | 4.9707V |
| + 10V | 19.5mV | 9.9414V |

$$1LSB = \frac{FS}{256}$$

## UNIPOLAR LOGIC CODING

| Analogue input ($A_{IN}$) (Nominal code centre value) | Output code (Binary) |
|---|---|
| FS - 1LSB | 11111111 |
| FS - 2LSB | 11111110 |
| ¾FS | 11000000 |
| ½ FS + 1LSB | 10000001 |
| ½FS | 10000000 |
| ½FS - 1LSB | 01111111 |
| ¼FS | 01000000 |
| 1LSB | 00000001 |
| 0 | 00000000 |

## BIPOLAR OPERATION

For bipolar operation the input to the ZN427 is offset by half full-scale by connecting a resistor $R_3$ between $V_{REF\ IN}$ and $V_{IN}$ (Fig. 15).

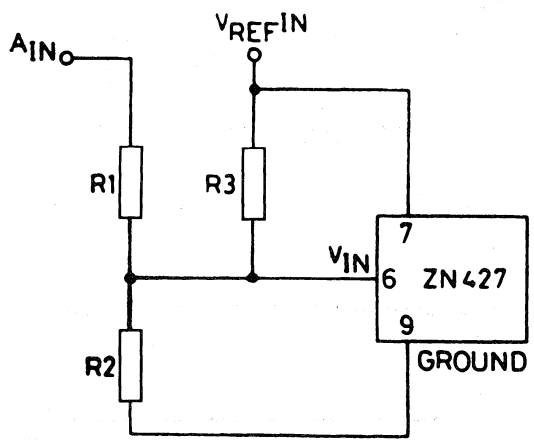



**Fig. 15 Bipolar operation - general connection**

When $A_{IN} = -FS$, $V_{IN}$ needs to be equal to zero.

When $A_{IN} = +FS$, $V_{IN}$ needs to be equal to $V_{REF\ IN}$.

If full-scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G - 1)$. $R_2$ and $R_1 = G$. $R_3$ fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ $(= R_{IN}) = 4k\Omega$.

Thus the nominal values of $R_1$, $R_2$, $R_3$ are given by $R_1 = 8\ Gk\Omega$, $R_2 = 8G/(G - 1)k\Omega$, $R_3 = 8k\Omega$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\ IN}$) results if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5$ volts the nominal values of resistors for $\pm 5$ and $\pm 10$V input ranges are given in the following table.

| Input range | G | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|---|
| ±5V | 2 | 16kΩ | 16kΩ | 8kΩ |
| ±10V | 4 | 32kΩ | 10.66kΩ | 8kΩ |

Minus full-scale (offset) is set by adjusting $R_1$ about its nominal value relative to $R_3$. Plus full-scale (gain) is set by adjusting $R_2$ relative to $R_1$.

Practical circuit realisations are given in Fig. 16.

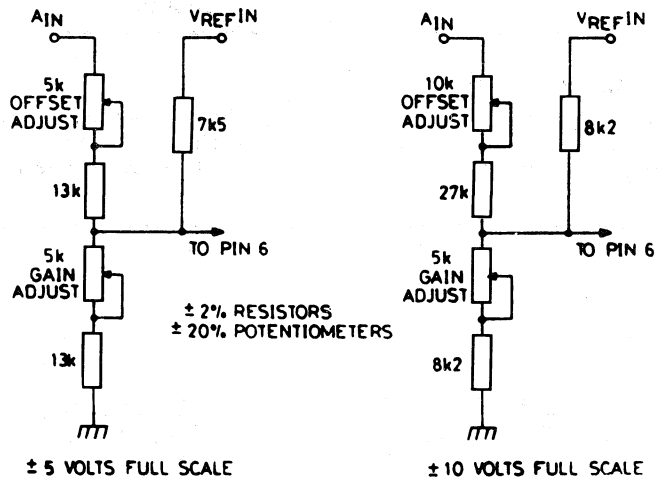



**Fig. 16 Bipolar operation - component values**

Note that in the ±5V case $R_3$ has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers.

**BIPOLAR ADJUSTMENT PROCEDURE**

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply −(FS - ½LSB) to $A_{IN}$ and adjust offset until the bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply +(FS - 1½LSB) to $A_{IN}$ and adjust gain until bit 8 just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

**BIPOLAR SETTING-UP POINTS**

| Input range, ±FS | −(FS − ½LSB) | +(FS − 1½LSB) |
|---|---|---|
| ±5V | −4.9805V | +4.9414V |
| ±10V | −9.9609V | +9.8828V |

$$1LSB = \frac{2FS}{265}$$

## BIPOLAR LOGIC CODING

| Analogue input ($A_{IN}$) (Nominal code centre value) | Output code (Offset binary) |
|---|---|
| + (FS - 1LSB) | 11111111 |
| + (FS - 2LSB) | 11111110 |
| + ½FS | 11000000 |
| + 1LSB | 10000001 |
| 0 | 10000000 |
| − 1LSB | 01111111 |
| − ½FS | 01000000 |
| − (FS - 1LSB) | 00000001 |
| − FS | 00000000 |

## SINGLE 5V SUPPLY RAIL OPERATION

The ZN427 takes very little power from the negative rail and so a suitable negative supply can be generated very easily using a 'diode pump' circuit. The circuit shown in Fig. 17 works with any clock frequency from 10kHz to 1MHz and can supply up to five ZN427's.

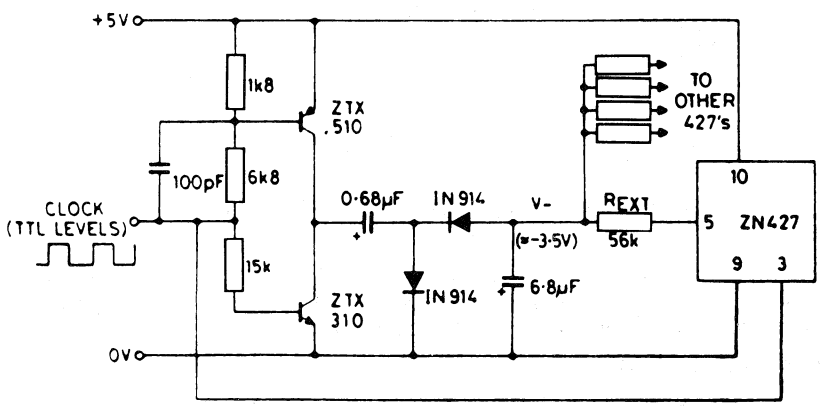



Fig. 17 Single 5V supply operation

# ZN428E8 / ZN428J8 / ZN428D

## 8-BIT LATCHED INPUT D-A CONVERTER

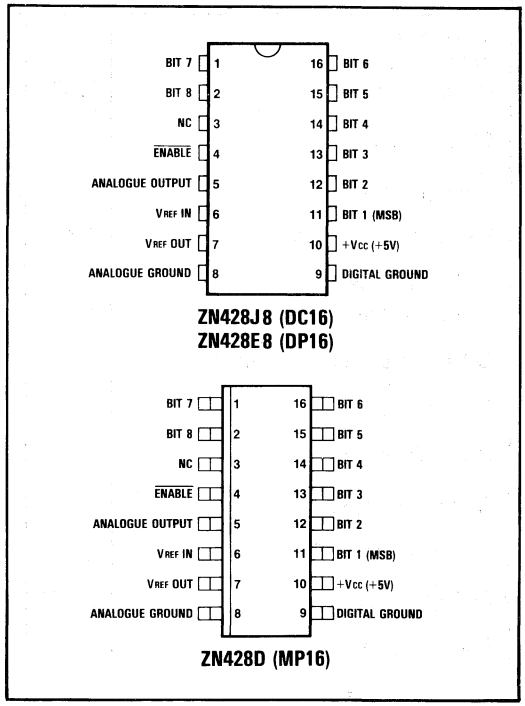
The ZN428 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when enable is LOW and the data is held when enable is taken HIGH. The ZN428 also contains a 2.5V reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

### FEATURES

- Contains DAC with Data Latch and On-Chip Reference
- Guaranteed Monotonic over the Full Operating Temperature Range
- Single +5V Supply
- Microprocessor Compatible
- TTL and 5V CMOS Compatible
- 800ns Settling Time
- Complementary to ZN427 A to D Series
- Commercial or Military Temperature Ranges

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| ZN428D | 0°C to +70°C | MP16 |
| ZN428E8 | 0°C to +70°C | DP16 |
| ZN428J8 | -55°C to +125°C | DC16 |




Pin connections - top view

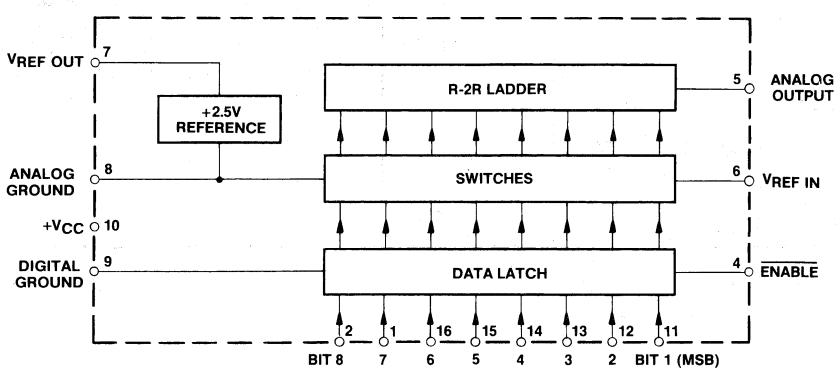



Fig.1 System diagram

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | +7.0V |
| Max. voltage, logic and $V_{REF}$ inputs | $+V_{CC}$ |
| Operating temperature range | 0°C to 70°C (ZN428E8, ZN428D)<br>−55°C to +125°C (ZN428J8) |
| Storage temperature range | −55°C to +125°C |
| Analogue ground to digital ground | ±200mV |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5V, $T_{amb}$ = 25°C unless otherwise specified).

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **Internal voltage Reference** | | | | | |
| Output voltage | 2.475 | 2.550 | 2.625 | V | $R_{REF}$ = 390Ω, $C_{REF}$ = 1μF |
| Slope resistance | | 0.5 | 2 | Ω | |
| $V_{REF\ OUT}$ T.C. | | 50 | | ppm/°C | |
| Reference current | 4 | | 15 | mA | Note 1 |
| **D-A converter** | | | | | |
| Linearity error | | | ±0.5 | LSB | 2.0V ≤ $V_{REF\ IN}$ ≤ 3.0V |
| Differential non-linearity | | ±0.5 | | LSB | |
| Linearity error T.C. | | ±3 | | ppm/°C | |
| Differential non-linearity T.C. | | ±6 | | ppm/°C | |
| Offset voltage | | 2 | 5 | mV | All bits OFF |
| Offset voltage T.C. | | ±6 | | μV/°C | |
| Full scale output | 2.545 | 2.550 | 2.555 | | External reference $V_{REF\ IN}$ = 2.560V, all bits ON |
| Full scale output T.C. | | 2 | | ppm/°C | |
| Analogue output resistance | | 4 | | kΩ | |
| External reference voltage | 0 | | 3.0 | V | |
| Settling time to 0.5 LSB | | 800 | | ns | 1 LSB major transition (note 2) |
| | | 1.25 | | μs | All bits ON to OFF or OFF to ON (note 2) |
| Operating temperature range: | | | | | |
| ZN428D and ZN428E8 | 0 | | 70 | C | |
| ZN428J8 | −55 | | 125 | C | |
| Supply voltage ($V_{CC}$) | 4.5 | 5.0 | 5.5 | V | |

Note 1 See REFERENCE

Note 2 $R_L$ = 10MΩ, $C_L$ = 10pF

**ELECTRICAL CHARACTERISTICS** (cont.)

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| Supply current | | 20 | 30 | mA | Note 3 |
| Power consumption | | 100 | | mW | |
| **Logic** (over specified operating temperature range) | | | | | |
| High level input voltage | 2.0 | | | V | |
| Low level input voltage | | | 0.8 | V | |
| High level input current | | | 60 | μA | $V_{IN} = 5.5V$, $V_{CC} = Max.$ |
| | | | 20 | μA | $V_{IN} = 2.4V$, $V_{CC} = Max.$ |
| Low level input current | | | −5 | μA | $V_{IN} = 0.4V$, $V_{CC} = Max.$ |
| Input clamp diode voltage | | −1.5 | | V | $I_{IN} = -8mA$ |
| Enable pulse width | 100 | | | ns | |
| Data set-up time | 150 | | | ns | Note 4 |
| Data hold time | 10 | | | ns | Note 5 |

Note 3 All inputs HIGH ($V_{IH} = 3.5V$)
Note 4 Set up time before $\overline{\text{enable}}$ goes high
Note 5 Hold time after $\overline{\text{enable}}$ goes high

## D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (< 1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

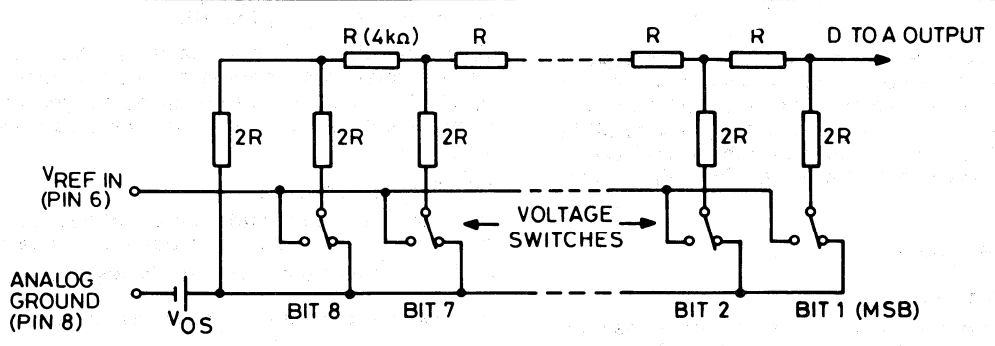



**Fig. 2 The R-2R ladder network**

Analogue output $= \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the data latch.

$V_{OS}$ is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. **The value of Vos is typically 1mV. This offset will normally be removed by the setting up procedure (see Operating Notes) and because the offset temperature coefficient is low (±6μV/°C) the effect on accuracy is negligible.**

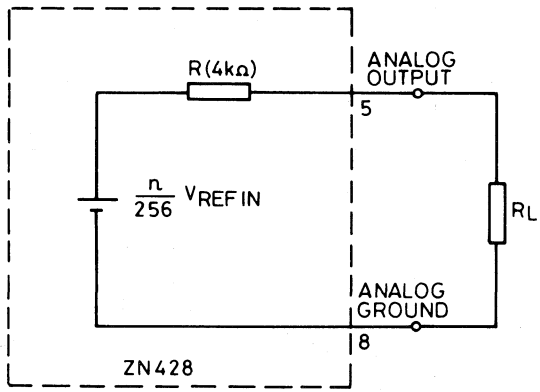



**Fig. 3 Analogue output equivalent circuit**

Fig. 3 shows an equivalent circuit of the output (ignoring $V_{OS}$). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R+R_L}$ % per °C

**$R_L$ should be chosen as large as possible to make the gain drift small. As an example if $R_L$ = 400kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN428 can be buffered by an amplifier (see Operating Notes).**

## REFERENCE

### (a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 4). A resistor ($R_{REF}$), should be connected between $+V_{CC}$ (pin 10) and pin 7. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor $C_{REF} = 1\mu F$ is required between pins 7 and 8 for internal reference option, $V_{REF\ OUT}$ (pin 7) being connected to $V_{REF\ IN}$ (pin 6).

Up to five ZN428's may be driven from one internal reference (there is no need to reduce $R_{REF}$). This useful feature saves power and gives excellent gain tracking between the converters.

### (b) External reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5}{n}$ Ω, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3V for ratiometric operation. The ZN428 is guaranteed monotonic for $V_{REF\ IN}$ above 2V.

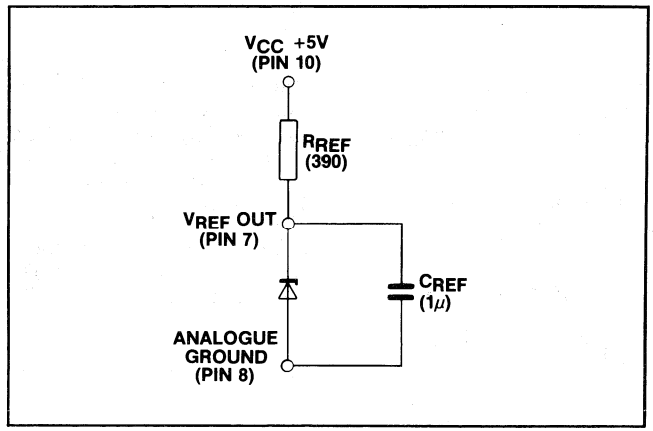



**Fig.4 Internal voltage reference**

## LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the enable input is low the data inputs drive the D to A directly. When enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig. 5.

The ZN428 is provided with separate analogue and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

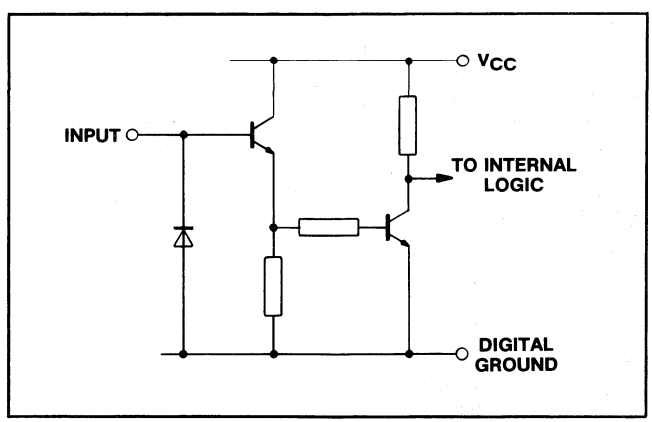



**Fig.5 Equivalent circuit of all inputs**

## OPERATING NOTES

### (1) Unipolar D-A converter

The nominal output range of the ZN428 is 0 to $V_{REF\ IN}$ through a 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig. 6) is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full-scale range is given by

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4kΩ). The required nominal values of R1 and R2 are given by $R1 = 4Gk\Omega$ and $R_2 = 4G/(G\text{-}1)k\Omega$.

Using these relationships a table of nominal resistance values for $R_1$ and $R_2$ can be constructed for $V_{REF\ IN} = 2.5V$.

| Output range | G | $R_1$ | $R_2$ |
|---|---|---|---|
| +5V | 2 | 8kΩ | 8kΩ |
| +10V | 4 | 16kΩ | 5.33kΩ |

For gain setting $R_1$ is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig. 7. Settling time for a major transistion is 1.5μs typical.

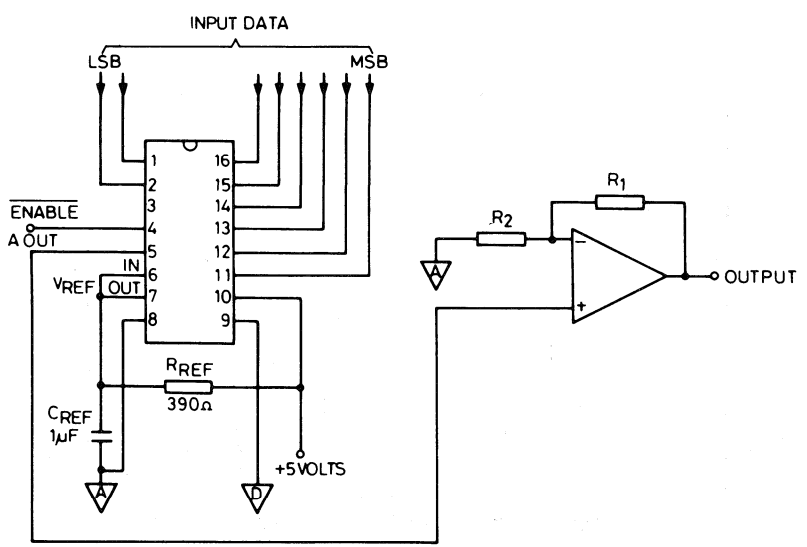



**Fig. 6 Unipolar operation - basic circuit**

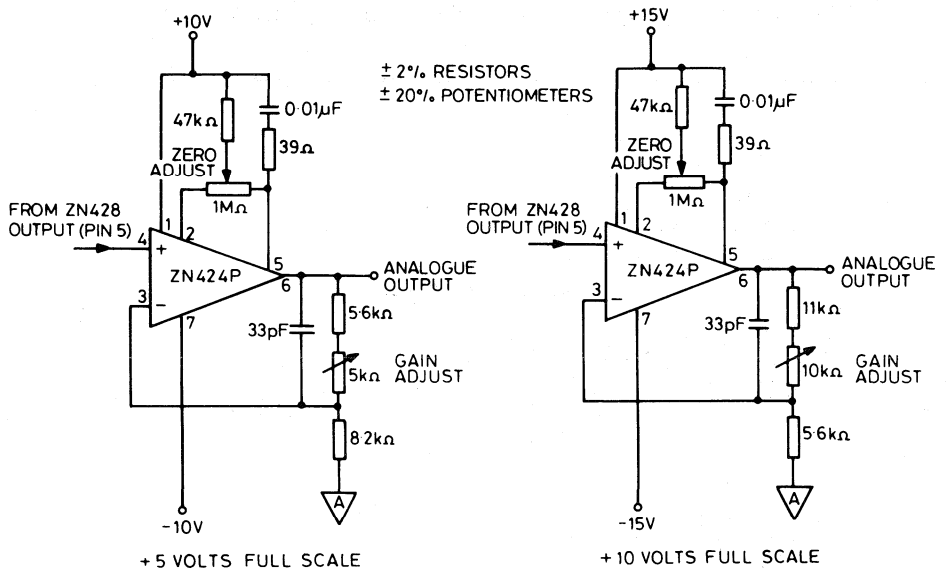



**Fig. 7 Unipolar operation - component values**

## UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$.

(ii) Set all bits ON (high) and adjust gain until $V_{OUT} = FS - 1LSB$.

### UNIPOLAR SETTING UP POINTS

| Output range, +FS | LSB | FS - 1LSB |
|---|---|---|
| +5V | 19.5mV | 4.9805V |
| +10V | 39.1mV | 9.9609V |

$$1LSB = \frac{FS}{256}$$

### UNIPOLAR LOGIC CODING

| Input code (Binary) | Analogue output (Nominal value) |
|---|---|
| 11111111 | FS - 1LSB |
| 11111110 | FS - 2LSB |
| 11000000 | ¾ FS |
| 10000001 | ½FS + 1LSB |
| 10000000 | ½FS |
| 01111111 | ½FS - 1LSB |
| 01000000 | ¼FS |
| 00000001 | 1LSB |
| 00000000 | 0 |

**(2) Bipolar D-A Converter**

For bipolar operation the output from the ZN428 is offset by half full scale by connecting a resistor $R_3$ between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 8).

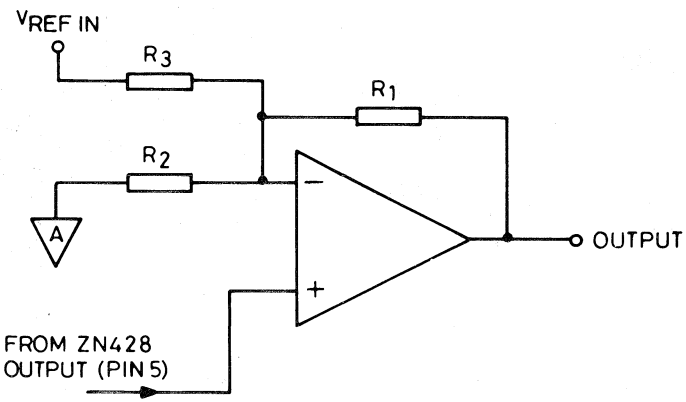



**Fig. 8 Bipolar operation - basic circuit**

When the digital input to the ZN428 is zero the analogue output is zero and the amplifier output should be −Full scale. An input of all ones to the D-A will give a ZN428 output of $V_{REF\ IN}$ and the amplifier output required is +Full-scale. Also, to match the ladder resistance the parallel combination of $R_1$, $R_2$ and $R_3$ should be 4kΩ.

The nominal values of $R_1$, $R_2$ and $R_3$ which meet these conditions are given by

$R_1 = 8Gk\Omega$, $R_2 = 8G/(G-1)k\Omega$ and $R_3 = 8k\Omega$

where the resultant output range is $\pm G\ V_{REF\ IN}$.

A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ±5 and ±10V output ranges are given in the following table:

| Output Range | G | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|---|
| ±5V | 2 | 16kΩ | 16kΩ | 8kΩ |
| ±10V | 4 | 32kΩ | 10.66kΩ | 8kΩ |

Minus full scale (offset) is set by adjusting $R_1$ about its nominal value relative to $R_3$. Plus full-scale (gain) is set by adjusting $R_2$ relative to $R_1$.

Practical circuit realisations are given in Fig. 9.

Note that in the ±5V case $R_3$ has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5μs typical.

## BIPOLAR ADJUSTMENT PROCEDURE

(1) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust offset until the amplifier output reads −full-scale.

(2) Set all bits ON (high) and adjust gain until the amplifier output reads +(full-scale - 1LSB).

### BIPOLAR SETTING UP POINTS

| Input range, ±FS | LSB | −FS | +(FS - 1LSB) |
|---|---|---|---|
| ±5V | 39.1mV | −5.0000V | +4.9609V |
| ±10V | 78.1mV | −10.0000V | +9.9219V |

$$1LSB = \frac{2FS}{256}$$

### BIPOLAR LOGIC CODING

| Input code (Offset binary) | Analogue output (Nominal value) |
|---|---|
| 11111111 | +(FS - 1LSB) |
| 11111110 | +(FS - 2LSB) |
| 11000000 | +½FS |
| 10000001 | +1LSB |
| 10000000 | 0 |
| 01111111 | −1LSB |
| 01000000 | −½FS |
| 00000001 | −(FS - 1LSB) |
| 00000000 | −FS |

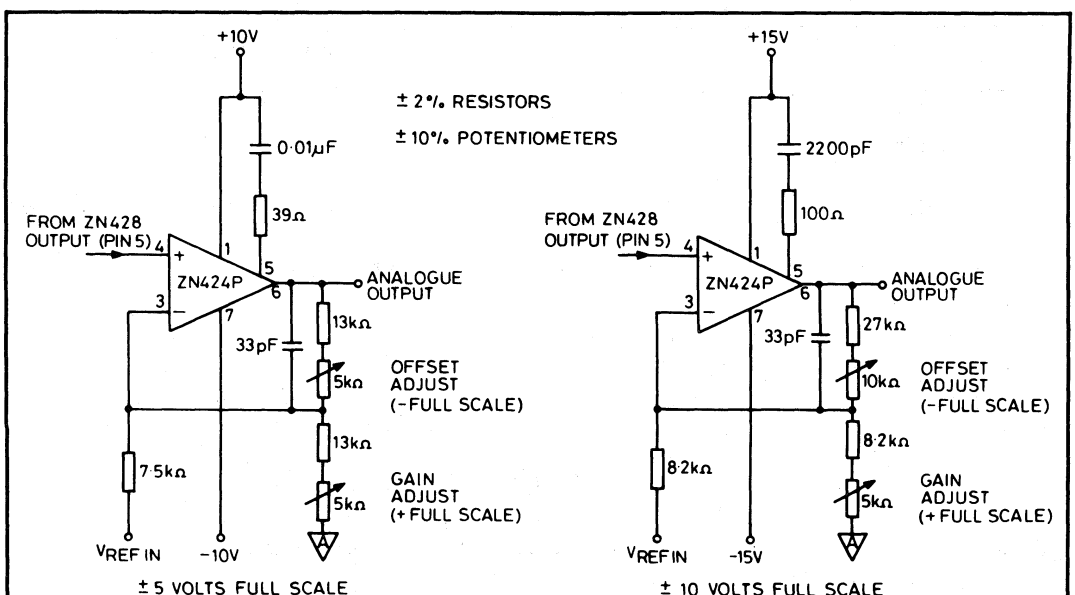



**Fig. 9 Bipolar operation - component values**

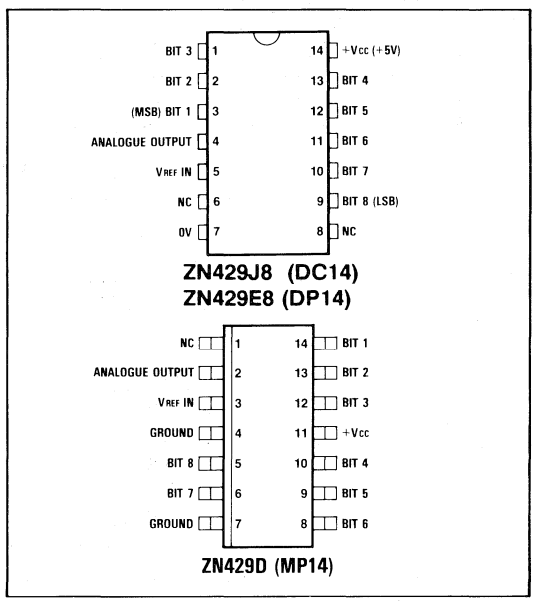
# ZN429E8 / ZN429J8 / ZN429D

## LOW COST 8-BIT D-A CONVERTER

The ZN429 is a monolithic 8-bit D-A converter containing an R-2R ladder network of diffused resistors with precision bipolar switches.

### FEATURES

- Linearity Error ±½ LSB
- Single +5V Supply
- Low Power Consumption 25mW Typical
- Settling Time 1 microsecond Typical
- TTL and 5V CMOS Compatible
- Designed for Low-Cost Applications




**Pin connections - top view**

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| **ZN429D** | 0°C to +70°C | MP14 |
| **ZN429E8** | 0°C to +70°C | DP14 |
| **ZN429J8** | -55°C to +125°C | DC14 |

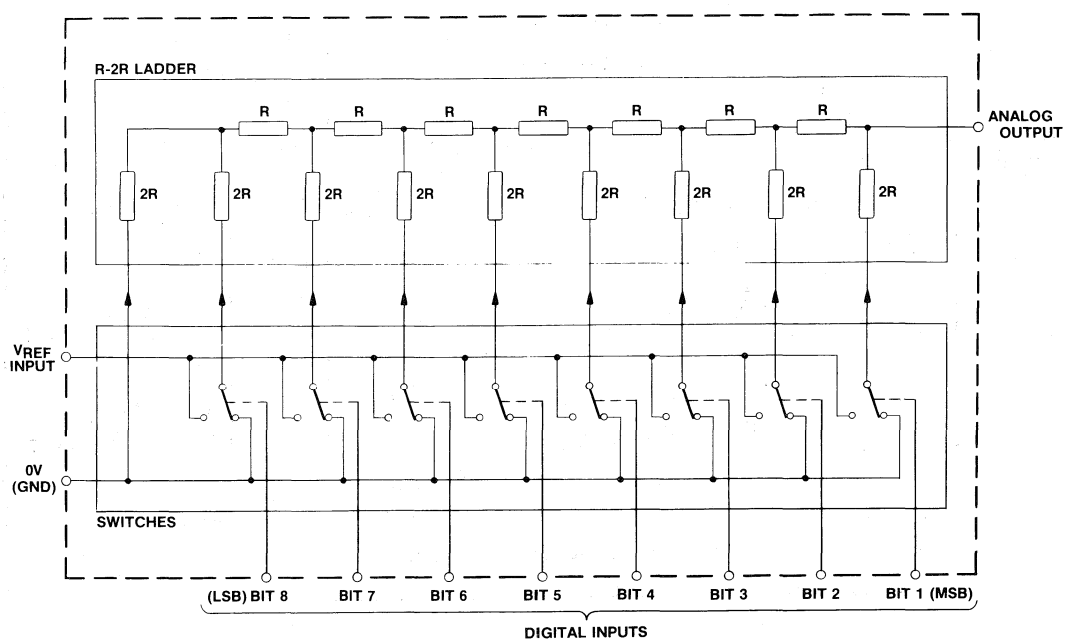



**Fig.1 System diagram (see pin connection diagrams above for pin outs)**

## INTRODUCTION

The ZN429 is an 8-bit D-A converter. It contains an advanced design of R-2R ladder network and an array of precision bipolar switches on a single monolithic chip.

The special design of ladder network results in full 8-bit accuracy using normal diffused resistors.

The converter is of the voltage switching type and uses an R-2R resistor ladder network as shown in Fig. 2.

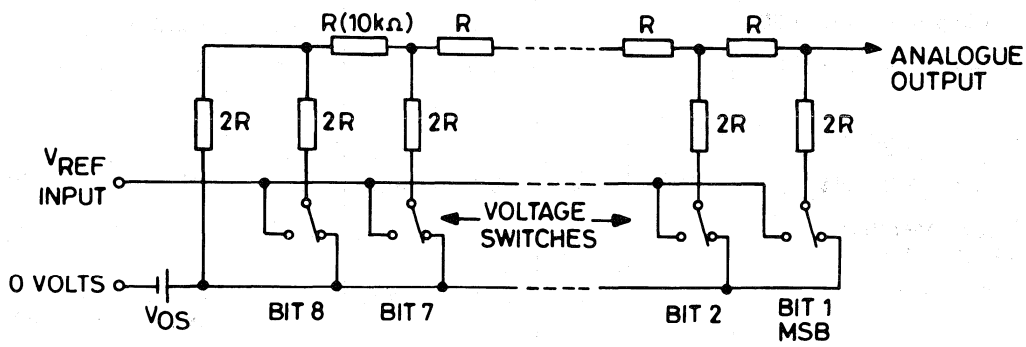



Fig. 2 The R-2R ladder network

Each 2R element is connected either to 0V or $V_{REF}$ by transistor switches specially designed for low offset voltage (typically 1mV).

Binary weighted voltages are produced at the output of the R-2R ladder, the value depending on the digital number applied to the bit inputs.

An external fixed or varying reference is required which should have a slope resistance less than 2Ω.

Suggested external reference sources are the ZN404 or one of the ZN458 range. Each ZN404 is capable of supplying up to five ZN429 circuits and this is increased to ten for the ZN458 range.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | +7V |
| Max. voltage, logic and $V_{REF}$ inputs | +5.5V |
| Storage temperature range | −55 to +125°C |

**ELECTRICAL CHARACTERISTICS** (at $T_{amb} = 25°C$ and $V_{CC} = +5V$ unless otherwise specified).

| Parameter | Symbol | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Converter** | | | | | | |
| Resolution | | 8 | – | – | Bits | |
| Accuracy | | 8 | – | – | Bits | |
| Non-linearity | | – | – | ±0.5 | LSB | Note 1 |
| Differential non-linearity | | – | ±0.5 | – | LSB | Note 2 |
| Settling time to 0.5LSB | | – | 1.0 | – | μs | 1 LSB step |
| Settling time to 0.5LSB | | – | 2.0 | – | μs | All bits ON to OFF or OFF to ON |
| Offset voltage | | | | | | |
| ZN429J-8 | $V_{OS}$ | | 5.0 | 8.0 | mV | All bits OFF note 1 |
| ZN429E-8, ZN429D | $V_{OS}$ | – | 3.0 | 5.0 | mV | All bits OFF note 1 |
| $V_{OS}$ temperature co-efficient | | – | 5 | – | μV/°C | |
| Full-scale output | | 2.545 | 2.550 | 2.555 | V | All bits ON Ext. $V_{REF} = 2.56V$ |
| Full-scale temperature coefficient | | – | 3 | – | ppm/°C | Ext. $V_{REF} = 2.560V$ |
| Non-linearity temp. co-efficient | | – | 7.5 | – | ppm/°C | Relative to F.S.R. |
| Analogue output resistance | $R_O$ | – | 10 | – | kΩ | |
| External reference voltage | | 0 | – | 3.0 | V | |
| Supply voltage | $V_{CC}$ | 4.5 | – | 5.5 | V | |
| Supply current | $I_S$ | – | 5 | 9 | mA | |
| High level input voltage | $V_{IH}$ | 2.0 | – | – | V | |
| Low level input voltage | $V_{IL}$ | – | – | 0.7 | V | |
| High level input current | $I_{IH}$ | – | – | 10 | μA | $V_{CC} = max$, $V_I = 2.4V$ |
| | | – | – | 100 | μA | $V_{CC} = max$, $V_I = 5.5V$ |
| Low level input current | $I_{IL}$ | – | – | −0.18 | mA | $V_{CC} = max$, $V_I = 0.3V$ |

Notes:

1. The ZN429J-8 differs from the ZN429E-8 and the ZN429D in the following respects:
   (a) For the ZN429J-8, the maximum linearity error may increase to ±0.4% FSR i.e. ±1LSB over the temperature ranges −55 to 0°C and +70 to +125°C.
   (b) Offset voltage. The difference is due to package lead resistance. This offset will normally be removed by the setting up procedure, and because the offset temperature coefficient is low, the specified accuracy will be maintained.
2. Monotonic over full temperature range.

## APPLICATIONS

### (1) Unipolar D-A converter

The nominal output range of the ZN429 is 0 to $V_{REF\ IN}$ through a 10kΩ resistance. Other output ranges can readily be obtained using an external amplifier.

The resulting full-scale range is given by

$$V_{OUT\ FS} = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.\ V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (10kΩ). The required nominal values of R1 and R2 are given by

$$R1 = 10Gk\Omega \text{ and } R2 = 10G/(G\text{-}1)\ k\Omega$$

Using these relationships a table of nominal resistance values for R1 and R2 can be constructed for $V_{REF\ IN} = 2.5V$.

| Output range | G | R1 | R2 |
|---|---|---|---|
| +5V | 2 | 20kΩ | 20kΩ |
| +10V | 4 | 40kΩ | 13.33kΩ |

For gain setting R1 is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig. 4. Settling time for a major transition is 2.5μs typical.

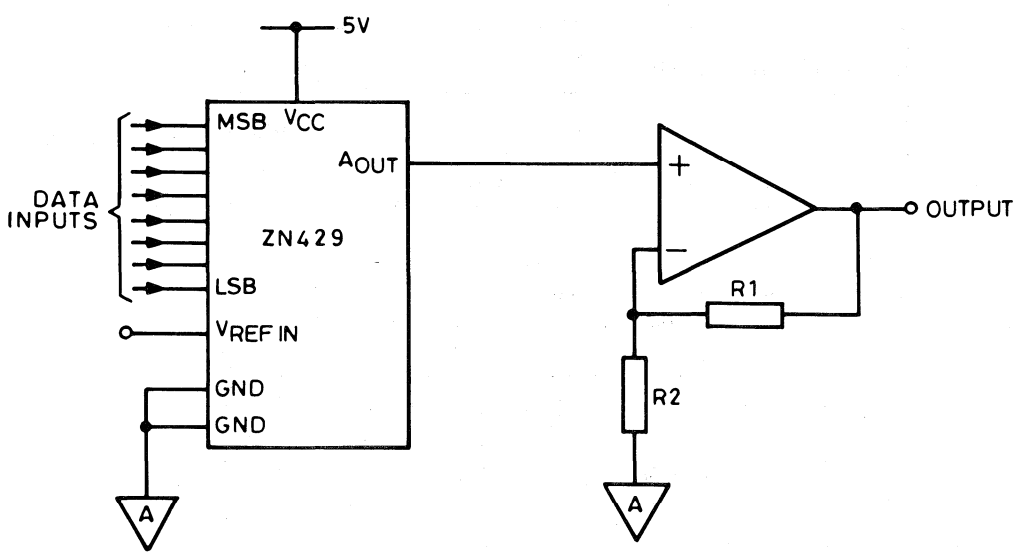



Fig. 3 Unipolar operation - basic circuit

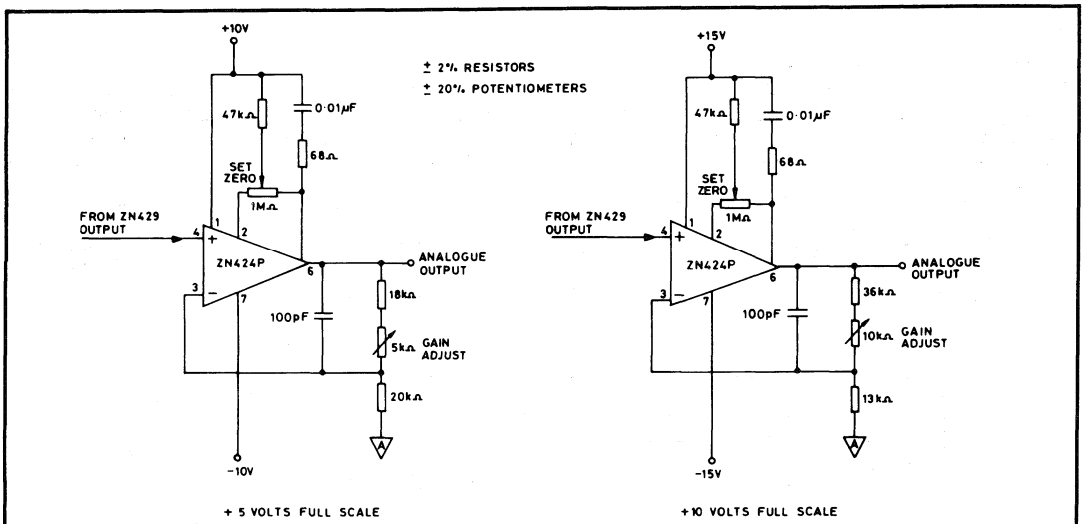



**Fig. 4 Unipolar operation - component values**

## UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (LOW) and adjust zero until $V_{OUT} = 0.0000V$

(ii) Set all bits ON (HIGH) and adjust gain until $V_{OUT} = FS - 1LSB$.

### UNIPOLAR SETTING UP POINTS

| Output range, +FS | LSB | FS − 1LSB |
|---|---|---|
| +5V | 19.5mV | 4.9805V |
| +10V | 39.1mV | 9.9609V |

$$1LSB = \frac{FS}{256}$$

### UNIPOLAR LOGIC CODING

| Input code (Binary) | Analogue output (Nominal value) |
|---|---|
| 11111111 | FS − 1LSB |
| 11111110 | FS − 2LSB |
| 11000000 | ¾FS |
| 10000001 | ½FS + 1LSB |
| 10000000 | ½FS |
| 01111111 | ½FS − 1LSB |
| 01000000 | ¼FS |
| 00000001 | 1LSB |
| 00000000 | 0 |

**(2) Bipolar D-A converter**

For bipolar operation the output from the ZN429 is offset by half full-scale by connecting a resistor R3 between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 5).

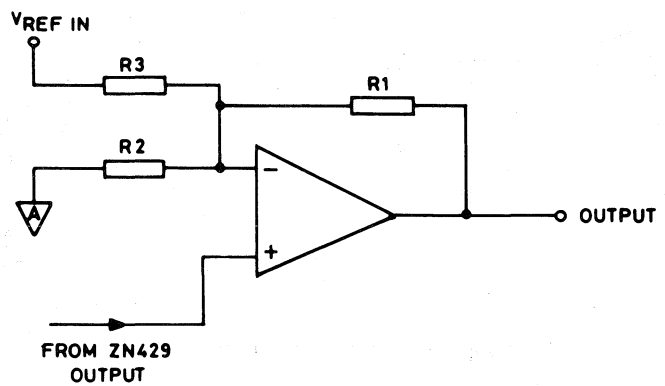



**Fig. 5 Bipolar operation - basic circuit**

When the digital input of the ZN429 is zero the analogue output is zero and the amplifier output should be −full-scale. An input of all ones to the D-A will give a ZN429 output of $\simeq V_{REF\ IN}$ and the amplifier output required is +full-scale. Also, to match the ladder resistance, the parallel combination of R1, R2 and R3 should be 10kΩ.

The nominal values of R1, R2 and R3 which meet these conditions are given by

R1 = 20GkΩ, R2 = 20G/(G-1)kΩ and R3 = 20kΩ

where the resultant output range is $\pm G.V_{REF\ IN}$.

Assuming that $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ±5 and ±10V output ranges are given in the following table.

| Output range | G | R1 | R2 | R3 |
|---|---|---|---|---|
| ±5V | 2 | 40kΩ | 40kΩ | 20kΩ |
| ±10V | 4 | 80kΩ | 26.67kΩ | 20kΩ |

Minus full-scale (OFFSET) is set by adjusting R1 about its nominal value relative to R3. Plus full-scale (GAIN) is set by adjusting R2 relative to R1

Settling time for a major transition is 2.5μs typical.

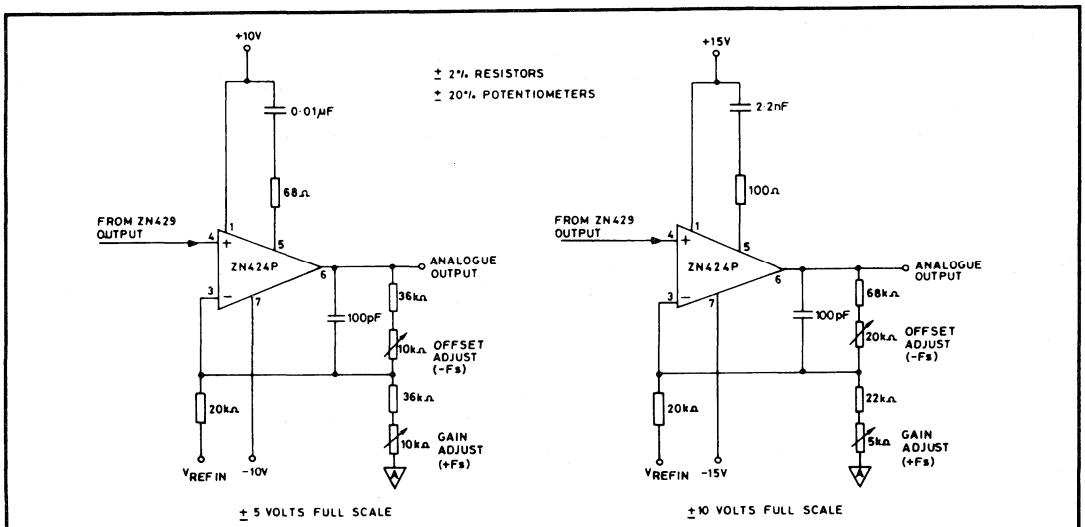



**Fig. 6 Bipolar operation component values**

## BIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (LOW) and adjust OFFSET until the amplifier output reads −FULL-SCALE.

(ii) Set all bits ON (HIGH) and adjust gain until the amplifier reads +(FULL-SCALE - 1LSB).

### BIPOLAR SETTING UP POINTS

| Input range, ±FS | LSB | −FS | +(FS - 1LSB) |
|---|---|---|---|
| ±5V | 39.1mV | −5.0000V | +4.9609V |
| ±10V | 78.1mV | −10.0000V | +9.9219V |

$$1LSB = \frac{2FS}{256}$$

### BIPOLAR LOGIC CODING

| Input code (Offset binary) | Analogue output (Nominal value) |
|---|---|
| 11111111 | +(FS − 1LSB) |
| 11111110 | +(FS − 2LSB) |
| 11000000 | +½FS |
| 10000001 | + 1LSB |
| 10000000 | 0 |
| 01111111 | − 1LSB |
| 01000000 | −½FS |
| 00000001 | −(FS - 1LSB) |
| 00000000 | −FS |

For both unipolar and bipolar operation, an alternative output buffer, employing the 741 operational amplifier, or any other suitable op-amp, may be used.

The feedback resistors chosen are as indicated in the relevant sections.

The following circuit shows the use of the 741 in the unipolar operation mode for a voltage output range of 0→5V with a 2.5V reference.

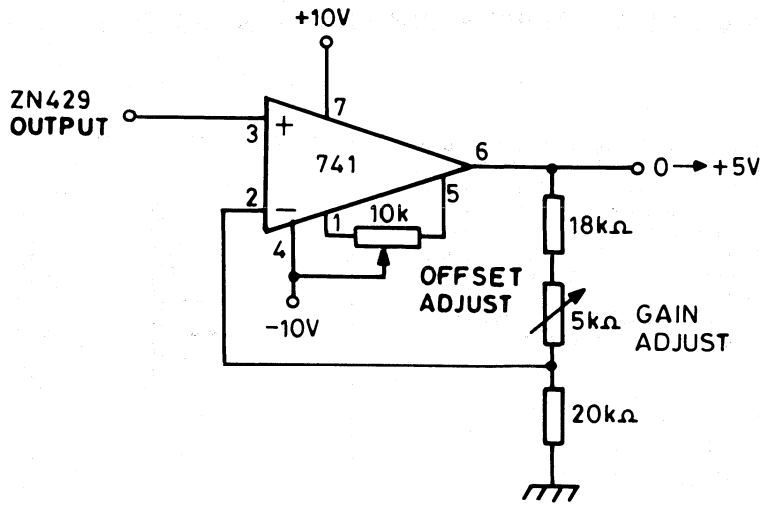



**Fig. 7 Unipolar operation (+5V full-scale) using 741 op-amp**

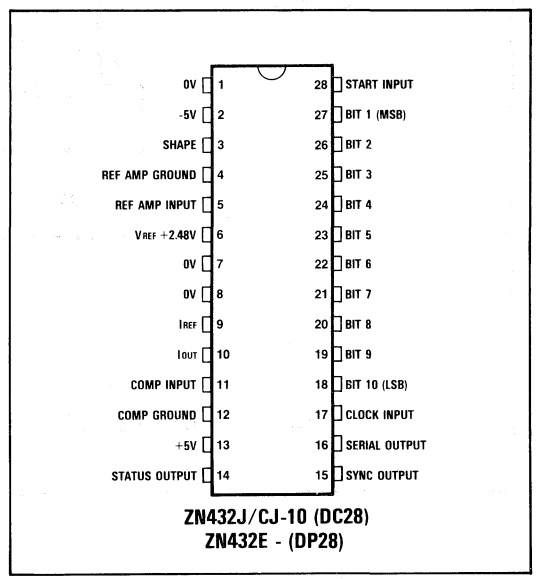
# ZN432E / ZN432CJ10

## 10-BIT SUCCESSIVE APPROXIMATION A-D CONVERTER

The ZN432 range of successive approximation analogue to digital converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), successive approximation logic with TTL interfacing. 2.5V precision voltage reference with reference amplifier, and fast comparator with good overload recovery. The overall accuracy of the A-D system is sufficient to guarantee no missing codes over the operating temperature range.

### FEATURES

- Choice of Linearity Error
- 3 Operating Temperature Ranges
- 20 microseconds Conversion Time Guaranteed
- Input Range as Desired
- ±5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction




**ZN432J/CJ-10 (DC28)**
**ZN432E - (DP28)**

**Pin connections - top view**

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| **ZN432E** | 0°C to +70°C | DP28 |
| **ZN432J-10** | -55°C to +125°C | DC28 |
| **ZN432CJ-10** | 0°C to +70°C | DC28 |

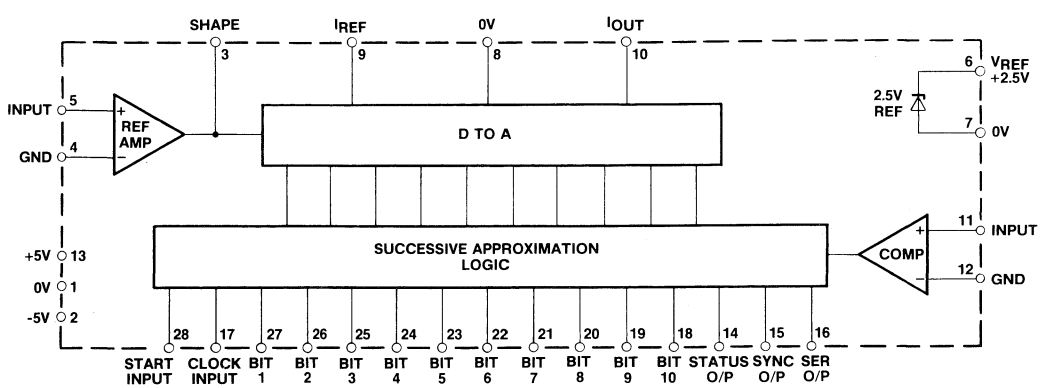



**Fig.1 System diagram**

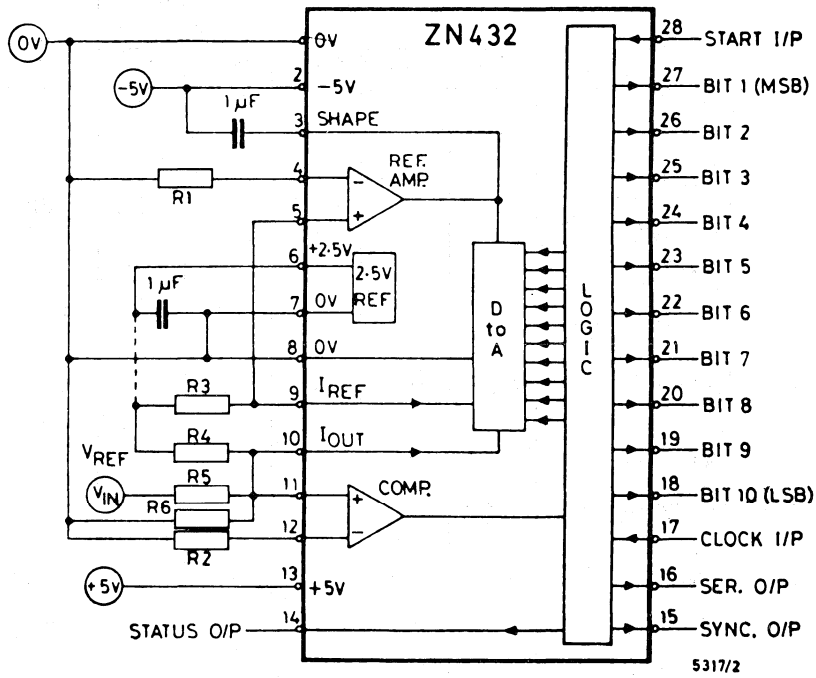



Fig. 2 Typical external components

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | ±7V |
| Logic input voltage | $+V_{CC}$ and 0V |
| Storage temperature range | −55 to +125°C |

**CHARACTERISTICS** (at ±5V supplies and internal reference unless otherwise specified).

| Parameter | Version | $t_{amb}$ = +25°C | | | Over Spec. Temp. range | | Units | Conds. |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Max. | | |
| **Converter** Resolution | | 10 | | | 10 | | Bits | Note 1 |
| Linearity error | ZN432J-10 | | | ±0.5 | | ±0.5 | LSB | |
| | ZN432CJ-10 | | | | | | | |
| | ZN432E | | | ±1 | | ±1 | LBS | |
| Differential linearity error | All types | | ±0.5 | | | | LSB | Note 1 |
| DAC reference current, $I_{REF}$ | All types | 0.25 | 0.5 | 1 | 0.25 | 1 | mA | Note 2 |
| Conversion time | All types | | 15 | 20 | | 20 | μs | Note 3 |
| Nominal analogue input range | All types | −2.5 | | +2.5 | | | V | Note 4 |
| Supply rejection | All types | | 0.1 | | | | %/V | |
| Gain error | All types | | ±0.05 | | | | % | Note 5 |
| Gain T.C. | ZN432J-10 | | 10 | | | | ppm/°C | |
| | ZN432CJ-10 | | | | | | | |
| | ZN432E | | 20 | | | | ppm/°C | |
| Zero T.C. | ZN432J-10 | | 7 | | | | ppm/°C | |
| | ZN432CJ-10 | | | | | | | |
| | ZN432E | | 15 | | | | ppm/°C | |
| Supply voltage | All types | ±4.5 | ±5 | ±5.5 | ±4.5 | ±5.5 | V | |
| Supply current | All types | | 35 | | | | mA | |
| Power consumption | All types | | 350 | | | | mW | |

**CHARACTERISTICS** (Cont.)

| Parameter | Version | $t_{amb}$ = +25°C | | | Over Spec. Temp. range | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Min. | Max. | | |
| **Internal voltage reference** | | | | | | | | |
| Output voltage | ZN432J-10<br>ZN432CJ-10 | 2.44 | 2.48 | 2.52 | | | V | Note 6 |
| | ZN432E | 2.38 | 2.46 | 2.54 | | | V | |
| Slope impedance | All types | | 0.75 | | | | Ω | |
| Max. load current | All types | | ±2 | | | | mA | |
| **Logic** | **All types** | | | | | | | |
| High level input voltage | | 2.0 | | | 2.0 | | V | |
| Low level input voltage | | | | 0.8 | | 0.8 | V | |
| High level input current | | | 7 | | | | μA | $V_S = \pm 5.5V$<br>$V_I = 2.4V$ |
| | | | 50 | | | | μA | $V_S = \pm 5.5V$<br>$V_I = 5.5V$ |
| Low level input current | | | 1 | | | | μA | $V_S = \pm 5.5V$<br>$V_I = 0.4V$ |
| High level output voltage | | 2.4 | | | 2.4 | | V | $I_{load} = -40\mu A$ |
| Low level output voltage | | | | 0.4 | | 0.4 | V | $I_{load} = 1.6mA$ |

NOTES

1. No missing codes over full temperature range at resolution appropriate to accuracy.
2. The full scale D-A output current $I_{OUT} = 4 \times I_{REF}$. For optimum performance, $I_{REF} = 0.5mA$.
3. This corresponds to a maximum clock rate of 550kHz based on 11 clock periods per conversion cycle (see Fig. 5). This provides an update rate of 45kHz.
4. Single polarity and other input ranges may be provided by different input resistor values (see 'Calculation of External Resistors'.
5. Excluding reference.
6. For typical temperature performance, see Fig. 6.

## TEST CIRCUIT

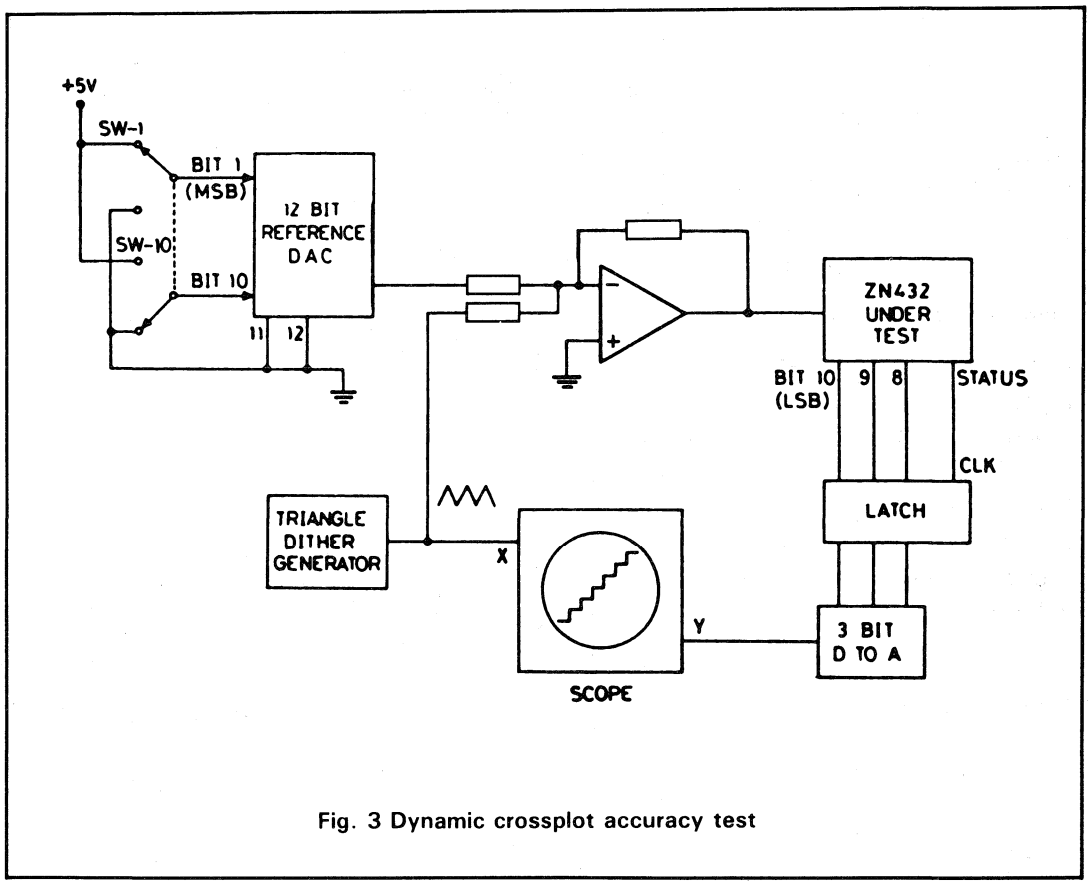



Fig. 3 Dynamic crossplot accuracy test

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the characteristic to be displayed. For example, code 10000 00000 would select half full-scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ LSB) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference DAC in the summing amplifier. The resulting analogue signal including dither is used as $V_{IN}$ for the ZN432 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3-bit DAC of at least 6-bit accuracy and the analogue output used as the Y deflection of the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

## CALCULATION OF EXTERNAL RESISTORS (See Fig. 2)

1. $R_3$, $R_4$, $R_5$ can affect gain and offset stability and thus require to be of high quality.
2. $R_1$ and $R_2$ are to allow for the bias current of the reference amplifier and comparator, thus:

$$R_1 = R_3$$

And $R_2$ = parallel combination of $R_4$, $R_5$, and $R_6$.

3. $I_{REF}$ should be 0.5mA

Therefore $$R_3 = \frac{V_{REF}}{0.5mA}$$

$I_{outFS}$ is four times $I_{REF}$, i.e., 2mA

4. Analysing the network yields the following:

$$R_4 = \frac{-V_{REF}\, R_5}{V_{in}\ min}$$

$$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{out\ FS}}$$

Where $V_{in}$ max is the voltage for the logic output to be all 1's.
$V_{in}$ min is the voltage for the logic output to be all 0's.

5. $R_6$ should be chosen such that the parallel combination of $R_4$, $R_5$ and $R_6$ is about 1.25kΩ as this determines the D-A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

| $V_{in}$ max | $V_{in}$ min | $V_{REF}$ | $R_1$[1] | $R_2$[1] | $R_3$ | $R_4$ | $R_5$ | $R_6$[1] |
|---|---|---|---|---|---|---|---|---|
| + 2.5 | − 2.5 | 2.5 | 5kΩ | 1.25kΩ | 5kΩ | 2.5kΩ | 2.5kΩ | ∞ |
| + 2.5 | − 2.5 | 5* | 10kΩ | 1.25kΩ | 10kΩ | 5kΩ | 2.5kΩ | 5kΩ |
| + 2.5 | 0 | 2.5 | 5kΩ | 1.25kΩ | 5kΩ | ∞ | 1.25kΩ | ∞ |
| + 5 | 0 | 2.5 | 5kΩ | 1.25kΩ | 5kΩ | ∞ | 2.5kΩ | 2.5kΩ |
| + 4 | 2 | 2.5 | 5kΩ | 1.25kΩ | 5kΩ | 3.75kΩ | 3kΩ | 5kΩ |
| + 4 | − 2 | 12* | 24kΩ | 1.25kΩ | 24kΩ | 3.75kΩ | 3kΩ | 5kΩ |
| + 10 | − 10 | 2.5 | 5kΩ | 1.25kΩ | 5kΩ | 2.5kΩ | 10kΩ | 3.33kΩ |

Note 1 Nearest prefered value may be used for $R_1$, $R_2$ and $R_6$.

*Note 2 External reference.

7. For setting up $R_4$ will adjust the offset.
$R_3$ will adjust the gain.

For unipolar operation where $R_4$ approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of $R_4$ (Typical values only).

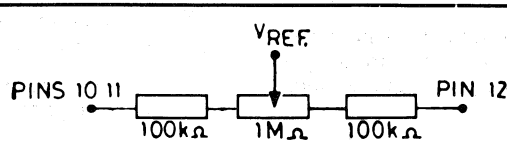



**Fig. 4 Offset circuit with unipolar operation**

## TIMING DETAILS

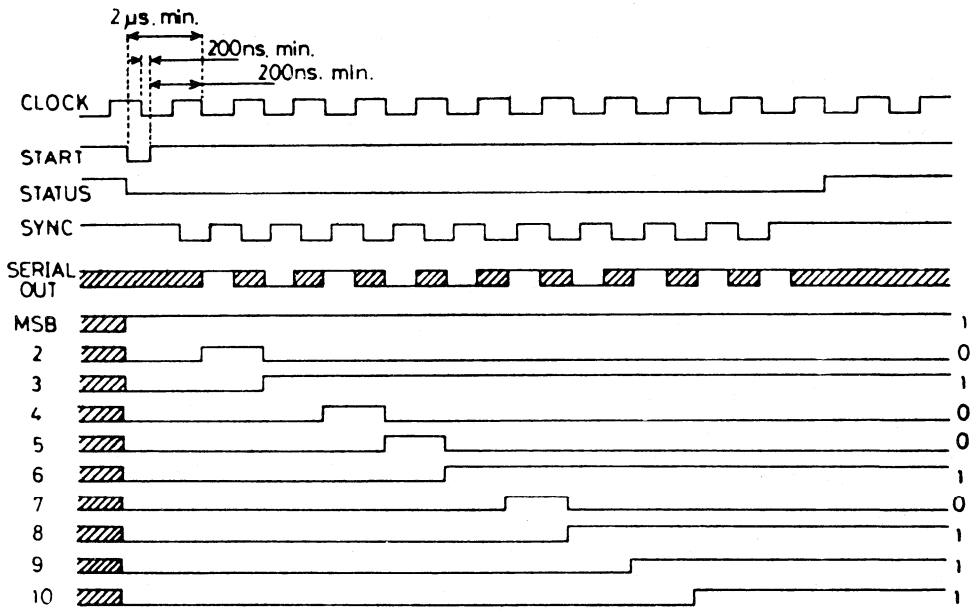



Fig. 5 Timing diagram

## NOTES ON TIMING DIAGRAM

1. Conversion is initiated by a 'START' pulse which sets the MSB to 1 and all other bits to 0.

2. The first active (negative going) edge of clock after the trailing edge of the 'START' pulse should not occur until at least 2$\mu$s after the leading edge of the 'START' pulse to allow for MSB settling.

3. A negative going edge of clock must not occur within 200ns either side of the trailing edge of the 'START' pulse.

4. As a special case of conditions (2) and (3) the 'START' pulse may be coincident with, and of the same duration as, a negative going clock pulse.

5. Serial data is available during conversion at the Serial Output.

Ten SYNC pulses are provided to facilitate data transmission.

The serial output data is valid on the positive going edge of the SYNC pulse.

6. Cross hatching indicates a 'don't care' condition or, in the case of serial output, invalid data.

7. The conversion sequence shown is for the digital word 1010010111.

8. The parallel output data is valid when the status output goes HIGH.

## LOGIC CODING

**Table 1 Unipolar operation**

| Analog input Notes 1, 2 | Digital output code MSB LSB |
|---|---|
| FS – 1LSB | 1111111111 |
| FS – 2LSB | 1111111110 |
| ¾FS | 1100000000 |
| ½FS + 1LSB | 1000000001 |
| ½FS | 1000000000 |
| ½FS – 1LSB | 0111111111 |
| ¼FS | 0100000000 |
| 1LSB | 0000000001 |
| 0 | 0000000000 |

**Table 2 Bipolar operation**

| Analog input Notes 1, 2 | Digital output code MSB LSB |
|---|---|
| +(FS – 1LSB) | 1111111111 |
| +(FS – 2LSB) | 1111111110 |
| +(½FS) | 1100000000 |
| +(1LSB) | 1000000001 |
| 0 | 1000000000 |
| –(1LSB) | 0111111111 |
| –(½FS) | 0100000000 |
| –(FS – 1LSB) | 0000000001 |
| –FS | 0000000000 |

**NOTES:**

1. Analog inputs shown are nominal centre values of code.
2. "FS" is full-scale.

## OFFSET AND GAIN SETTING

For unipolar, supply an input of ½LSB for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

For bipolar, supply an input of –(full-scale – ½LSB) for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

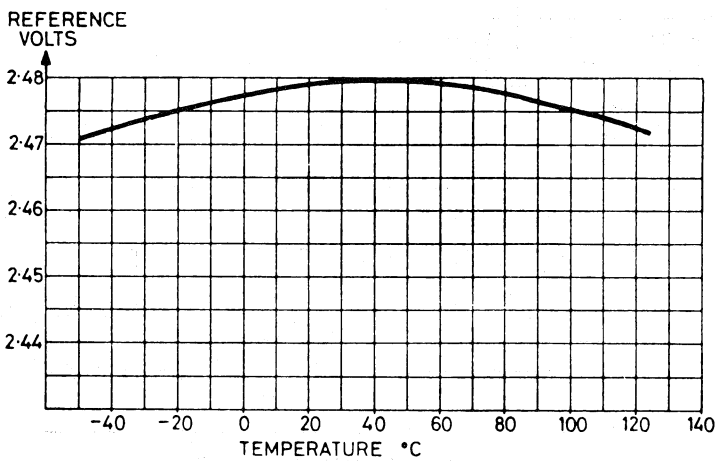



**Fig. 6 Typical reference voltage v temperature (all types)**

# ZN433J10 / ZN433CJ10

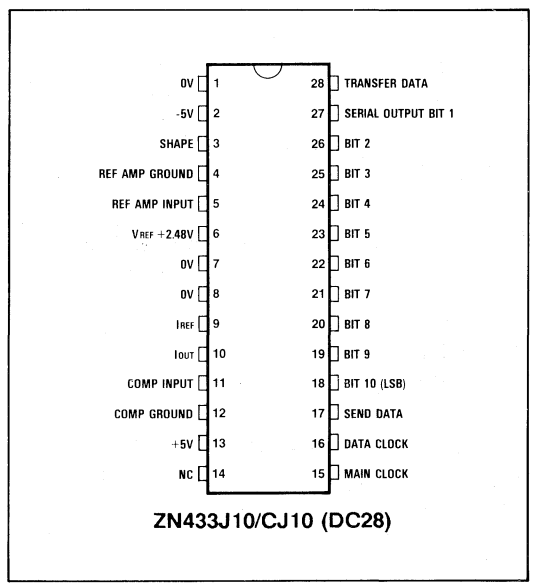
## 10-BIT TRACKING A-D CONVERTER

The ZN433 range of tracking A-D converters combine several innovations to provide this function on a fully monolithic silicon integrated circuit. The chip contains a current switching array using a matrix of diffused resistors (no trim required), tracking logic with TTL interfacing, 2.5V precision voltage reference with reference amplifier, and fast window comparator with good overload recovery.

The tracking principle ensures continuous up to date conversion data. This is suitable for single channel conversion, e.g. digital transducers, and often obviates the need for sample and hold.

### FEATURES

- ±½ LSB Linearity Error
- 1 microsecond Conversion Time (Assuming Continuous Tracking)
- Input Range as Desired
- ±5V Supplies, TTL/CMOS Compatible
- Parallel and Serial Outputs
- Bipolar Monolithic Construction
- No Missing Codes over Full Operating Temperature Range




Pin connections - top view

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| ZN433J10 | -55°C to +125°C | DC28 |
| ZN433CJ10 | 0°C to +70°C | DC28 |

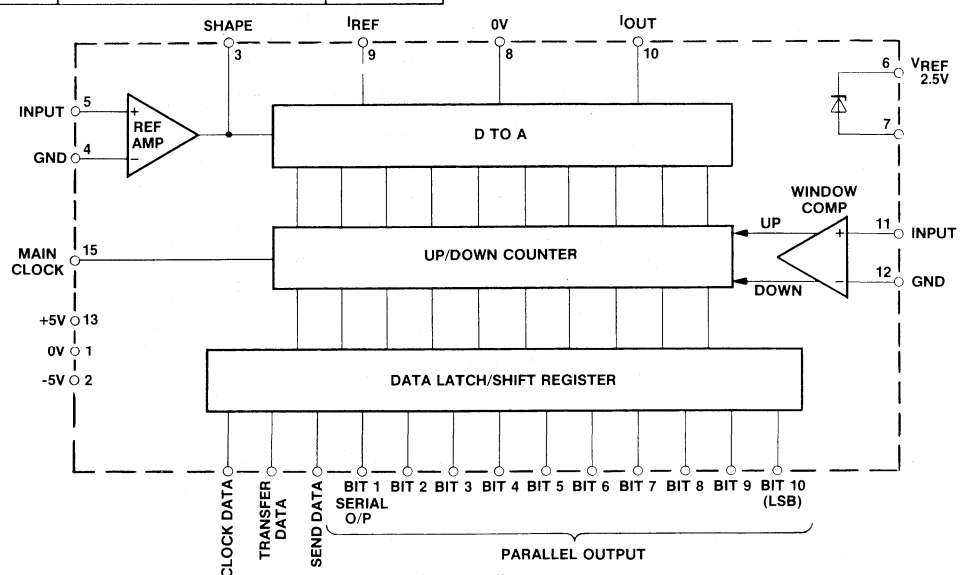



Fig.1 System diagram

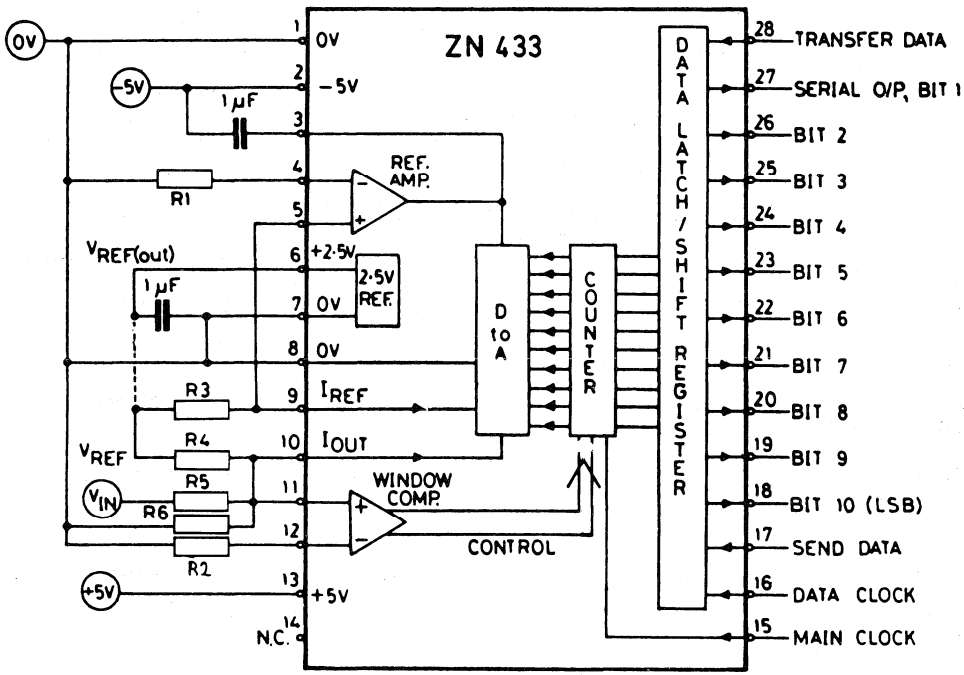



**Fig. 2 Typical external components**

For resistor values, see 'Calculation of External Resistors'. When the internal reference is used, $V_{REF}$ OUT (pin 6) is connected to R3 and R4 as shown. An external reference may also be used, which for ratiometric operation can vary by ±20% of nominal.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | ±7V |
| Logic input voltage | $+V_{CC}$ and 0V |
| Storage temperature range | −55 to +125°C |

**CHARACTERISTICS** (at ±5V supplies and internal reference unless otherwise specified).

| Parameter | $t_{amb}$ = +25°C | | | Over Spec. Temp. range | | Units | Conds. |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| **Converter** | | | | | | | |
| Resolution | 10 | | | 10 | | Bits | Note 1 |
| Non-linearity | | | ±0.5 | | | LSB | |
| Differential non-linearity | | ±0.5 | | | | LSB | Note 1 |
| D-A reference current, $I_{REF}$ (pin 9) | 0.8 | | 1.2 | 0.8 | 1.2 | mA | Note 2 |
| Max. clock rate | 1 | 1.2 | | 1 | | MHz | Note 3 |
| Nominal analogue input range | −2.5 | | +2.5 | | | V | Note 4 |
| Supply rejection | | 0.1 | | | | %/V | |
| Gain T.C. (note 5) | | 10 | | | | ppm/°C | |
| Zero T.C. | | 7 | | | | ppm/°C | |
| Supply voltage | ±4.5 | ±5 | ±5.5 | ±4.5 | ±5.5 | V | |
| Supply current | | 50 | | | | mA | |
| Power consumption | | 500 | | | | mW | |
| **Internal voltage reference** | | | | | | | |
| Output voltage | | 2.480 | | | | V | |
| Output voltage tolerance (note 6) | | | ±1.5 | | | % | |
| Slope impedance | | 0.75 | | | | Ω | |
| Maximum reference load current | | ±4 | | | | mA | |

**CHARACTERISTICS** (Cont.)

| Parameter | $t_{amb} = +25°C$ | | | Over Spec. Temp. range | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| **Logic** | | | | | | | |
| High level input voltage | 2.0 | | | 2.0 | | V | |
| Low level input voltage | | | 0.8 | | 0.8 | V | |
| High level input current | | 7 | | | | $\mu$A | $V_S = \pm 5.5V$, $V_I = 2.4V$ |
| | | 50 | | | | $\mu$A | $V_S = \pm 5.5V$, $V_I = 5.5V$ |
| Low level input current | | 1 | | | | $\mu$A | $V_S = \pm 5.5V$, $V_I = 0.4V$ |
| High level output voltage | 2.4 | | | 2.4 | | V | $I_{load} = -40\mu A$ |
| Low level output voltage | | | 0.4 | | 0.4 | V | $I_{load} = 1.6mA$ |

**NOTES**

1. **No missing codes over full temperature range.**
2. **The full-scale D-A output current $I_{OUT}$ = 4 times $I_{REF}$. For optimum performance $I_{REF}$ = 1.0mA.**
3. **For main clock waveform see Fig.5. Input signals which do not change by more than 1 LSB/$\mu$s may be tracked continuously without the need for a sample and hold. This corresponds to a full-scale bandwidth of 300Hz. Higher frequencies may be tracked if the amplitude is reduced, e.g. the half full-scale bandwidth is 600Hz.**
4. **Single polarity and other input ranges may be provided by different input resistor values.**
5. **Excluding reference.**
6. **For typical temperature performance see Fig.6.**

## TEST CIRCUIT

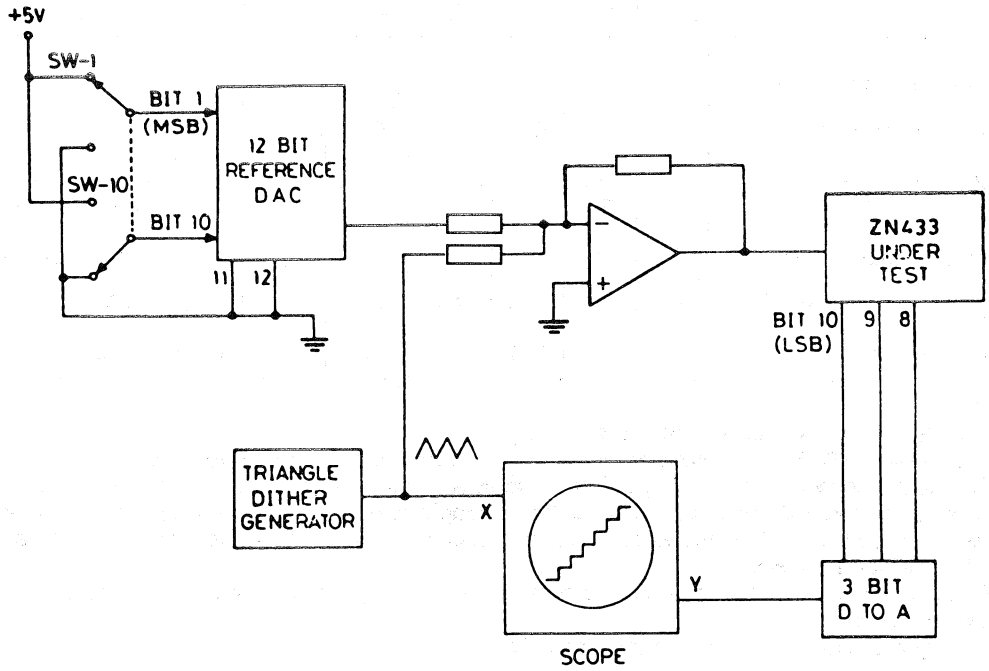



**Fig. 3 Dynamic crossplot accuracy test**

Switches SW-1 to SW-10 are set to the appropriate digital code to select the point on the charactristic to be displayed. For example, code 10000 00000 would select half full-scale, i.e. the major transition.

The output from the dither generator (suggested peak to peak amplitude = $\pm 4 \times$ LSB) is used as the X deflection for the scope and is also superimposed on the analogue output from the reference DAC in the summing amplifier. The resulting analogue signal including dither is used as $V_{IN}$ for the ZN433 under test.

Bit 10, 9 and 8 outputs are fed to the inputs of a 3-bit DAC of at least 6-bit accuracy and the analogue output used as the Y deflection of the scope. Differential non-linearity is shown by horizontal lines which are longer or shorter than the rest.

## CALCULATION OF EXTERNAL RESISTORS

1. $R_3$, $R_4$, $R_5$ can affect gain and offset stability and thus require to be of high quality.
2. $R_1$ and $R_2$ are to allow for the bias current of the reference amplifier and comparator which both operate in a virtual earth mode. Thus: $R_1 = R_3$

   And $R_2$ = parallel combination of $R_4$, $R_5$, and $R_6$.
3. $I_{REF}$ should be 1.0mA, though it may be varied from 0.8 to 1.2mA.

   Therefore $$R_3 = \frac{V_{REF}}{1.0mA}$$

   $I_{out\ FS}$ is four times $I_{REF}$, i.e., 4mA ($I_{out}$ for zero reading is 0mA).
4. Analysing the network yields the following:

$$R_4 = \frac{-V_{REF}\ R_5}{V_{in}\ min}$$

$$R_5 = \frac{V_{in}\ max - V_{in}\ min}{I_{outFS}}$$

   Where $V_{in}$ max is the voltage for the logic output to be all 1's.
   $V_{in}$ min is the voltage for the logic output to be all 0's.
5. $R_6$ should be chosen such that the parallel combination of $R_4$, $R_5$ and $R_6$ is about 625Ω as this determines the D-A time constant and hence conversion time.
6. The following is a table of values to give examples of the above equations.

| $V_{in}$ max | $V_{in}$ min | $V_{REF}$ | $R_1$[1] | $R_2$[1] | $R_3$ | $R_4$ | $R_5$ | $R_6$[1] |
|---|---|---|---|---|---|---|---|---|
| +2.5 | −2.5 | 2.5 | 2.5kΩ | 625Ω | 2.5kΩ | 1.25kΩ | 1.25kΩ | ∞ |
| +2.5 | −2.5 | 5* | 5kΩ | 625Ω | 5kΩ | 2.5kΩ | 1.25kΩ | 2.5kΩ |
| +2.5 | 0 | 2.5 | 2.5kΩ | 625Ω | 2.5kΩ | ∞ | 625Ω | ∞ |
| +5 | 0 | 2.5 | 2.5kΩ | 625Ω | 2.5kΩ | ∞ | 1.25kΩ | 1.25kΩ |
| +4 | −2 | 2.5 | 2.5kΩ | 625Ω | 2.5kΩ | 1.875kΩ | 1.5kΩ | 2.5kΩ |
| +4 | −2 | 12* | 12kΩ | 625Ω | 12kΩ | 1.875kΩ | 1.5kΩ | 2.5kΩ |
| +10 | −10 | 2.5 | 2.5kΩ | 625Ω | 2.5kΩ | 1.25kΩ | 5kΩ | 1.67kΩ |

Note 1 Nearest prefered value may be used for $R_1$, $R_2$ and $R_6$.

*Note 2 External reference.

7. For setting up $R_4$ will adjust the offset.
   $R_3$ will adjust the gain.

For unipolar operation where $R_4$ approaches ∞ and a zero adjustment is required, the following offset circuit is suggested in place of $R_4$ (Typical values only).

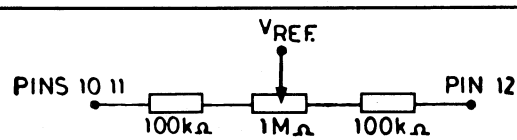



Fig. 4 Offset circuit with unipolar operation

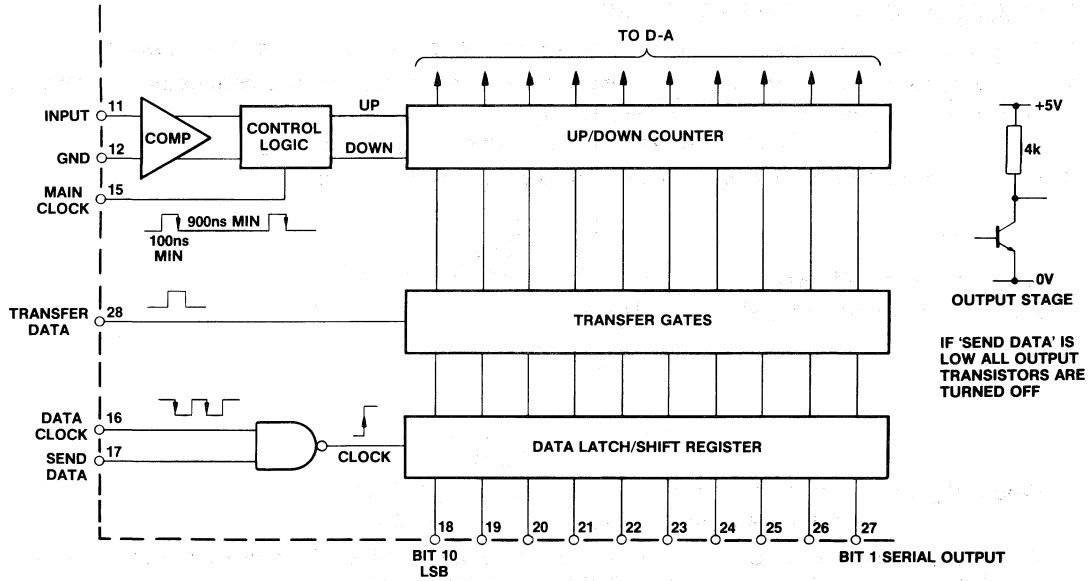



Fig.5 Logic system

## NOTES ON LOGIC DIAGRAM

1. The Window comparator and control logic determine whether the counter will clock up or down or keep the same value on an active (negative going) edge of the main clock.

2. Parallel data from the up/down counter will be loaded into the output data latch/shift register when the TRANSFER DATA input is HIGH. TRANSFER DATA should not be taken HIGH until 150ns after the MAIN CLOCK edge and should go LOW before the next MAIN CLOCK edge. The minimum TRANSFER DATA pulse width is 50ns.

If TRANSFER DATA is held permanently HIGH then the counter outputs will appear directly at the bit outputs.

3. Serial output data (MSB first) can be obtained from the MSB output (pin 27) by applying a DATA CLOCK (pin 16, 1MHz maximum, 100ns minimum pulse width).

4. A LOW on SEND DATA (pin 17) disables the DATA CLOCK and turns off all the output transistors so that all the bit outputs are HIGH (see diagram of output).

## LOGIC CODING

**Table 1 Unipolar operation**

| Analogue input Notes 1, 2 | Digital output code MSB LSB |
|---|---|
| FS – 1LSB | 1111111111 |
| FS – 2LSB | 1111111110 |
| ¾FS | 1100000000 |
| ½FS + 1LSB | 1000000001 |
| ½FS | 1000000000 |
| ½FS – 1LSB | 0111111111 |
| ¼FS | 0100000000 |
| 1LSB | 0000000001 |
| 0 | 0000000000 |

**Table 2 Bipolar operation**

| Analogue input Notes 1, 2 | Digital output code MSB LSB |
|---|---|
| + (FS – 1LSB) | 1111111111 |
| + (FS – 2LSB) | 1111111110 |
| + (½FS) | 1100000000 |
| + (1LSB) | 1000000001 |
| 0 | 1000000000 |
| – (1LSB) | 0111111111 |
| – (½FS) | 0100000000 |
| – (FS – 1LSB) | 0000000001 |
| – FS | 0000000000 |

Notes:

1. Analogue inputs shown are nominal centre values of code.
2. "FS" is full-scale.

## OFFSET AND GAIN SETTING

For unipolar operation, supply an input of ½LSB for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

For bipolar operation, supply an input of – (full-scale – ½LSB) for transition 0000000000 to 0000000001, and of (full-scale – 1½LSB) for transition 1111111111 to 1111111110.

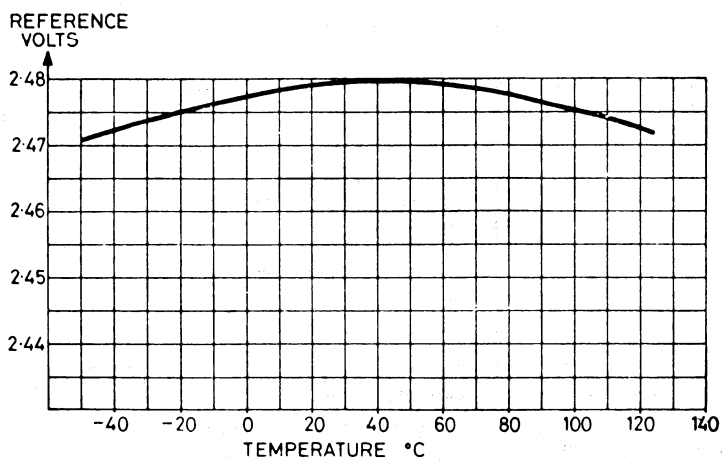



**Fig. 6 Typical reference voltage v temperature (all types)**

3011-1.0

# ZN435E

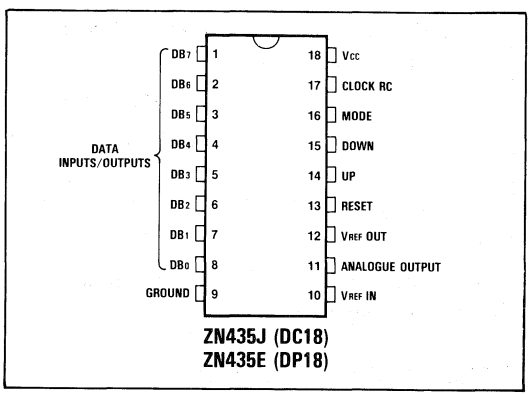
## 8-BIT MULTIFUNCTION DATA CONVERTER

*Not recommended for new designs - alternative is ZN525*

The ZN435 is a versatile, multifuction 8-bit data conversion system. A voltage output DAC, 8-bit up/down counter, stable 2.5V bandgap reference and clock generator are contained on a single chip.

### FEATURES

- Multimode Device Operates as:
  - DAC
  - ADC
  - Tracking ADC
  - Voltage to Frequency Converter
  - Ramp and Sawtooth Generator
  - Nonlinear Waveform Generator
  - Voltage-Controlled Oscillator
  - Track-and-Hold Circuit
- 8-Bit Accuracy
- 800ns D-A Converter Settling Time
- On-Chip Up/Down Counter
- On-Chip Clock
- On-Chip Voltage Reference
- Single +5V Supply
- Commercial or Military Temperature Range




**Pin connections - top view**

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| ZN435E | 0°C to +70°C | DP18 |

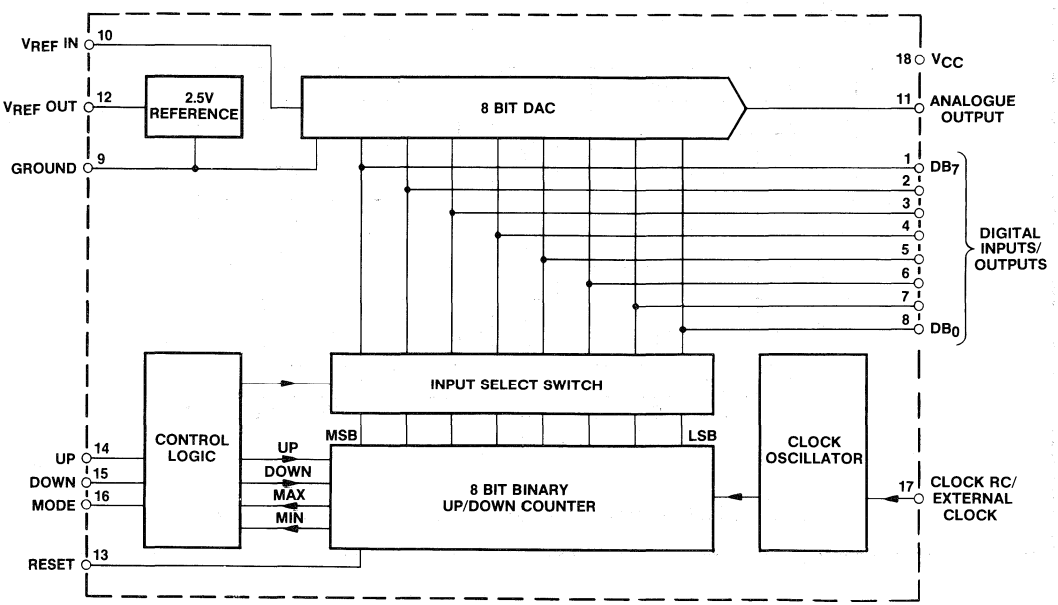



**Fig.1 System diagram**

## ABSOLUTE MAXIMUM RATINGS

| | | |
|---|---|---|
| Supply voltage | +7.0V | |
| Max. voltage, logic and $V_{REF}$ inputs | $V_{CC}$ | |
| | Min. | Max. |
| Operating temperature range ZN435E | 0°C | +70°C |
| Storage temperature range | −55°C | +125°C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5V, $V_{REF}$ = 1.5-3.0V, $T_{amb}$ = +25°C unless otherwise specified).

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **D-A converter** | | | | | |
| Resolution | 8 | – | – | Bits | |
| Linearity error | – | ±0.25 | ±0.5 | LSB | $T_{min}$ $T_{amb}$ $T_{max}$ |
| Differential linearity error | ±0.25 | | ±1 | LSB | |
| Zero error | – | 5.0 | 10.0 | mV | ZN435E<br>All bits OFF |
| Settling time to 0.5LSB | – | 500 | – | ns | All bits OFF to ON |
| | – | 800 | – | ns | or vice versa |
| Full-scale output | 2.545 | 2.550 | 2.555 | V | All bits ON<br>$V_{REF}$ = 2.56V |
| Output resistance | – | 4 | – | kΩ | |
| Full-scale temperature coefficient | – | 4 | – | ppm/°C | Ext. $V_{REF}$ = 2.56V |
| Reference voltage | 0 | – | 3 | V | |

**ELECTRICAL CHARACTERISTICS** (Cont.)

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **On-chip voltage reference** | | | | | |
| Output voltage | 2.4 | 2.59 | 2.7 | V | $R_{REF} = 390\Omega$ |
| Slope resistance | – | 2 | 4 | Ω | $C_{REF} = 220nF$ |
| Temperature coefficient of $V_{REF}$ | – | 50 | – | ppm/°C | |
| Reference current | 4 | – | 15 | mA | |
| **Counter** (with external clock) | | | | | |
| High level threshold voltage $V_{T+}$ | – | – | 2.3 | V | |
| Low level threshold voltage $V_{T-}$ | 1.7 | – | – | V | |
| Maximum clock frequency | 1 | – | – | MHz | Note 1 |
| **On-chip clock** | | | | | |
| Maximum frequency | 500 | – | – | kHz | |
| Clock frequency T.C. | – | 100 | – | ppm/°C | |
| Clock resistor | 3.3 | – | 100 | kΩ | |
| Clock capacitor | 100 | – | – | pF | |
| High level threshold voltage $V_{T+}$ | – | 4.6 | – | V | |
| Low level threshold voltage $V_{T-}$ | – | 1.5 | – | V | |
| Supply rejection | – | 0.8 | – | %/V | |
| **Logic circuits** | | | | | |
| **BIT INPUTS** | | | | | |
| High level input voltage $V_{IH}$ | 2.0 | – | – | V | |
| Low level input voltage $V_{IL}$ | – | – | 0.8 | V | |
| High level input current $I_{IH}$ | – | – | −100 | μA | $V_{IN} = 2.4V$ |
| Low level input current $I_{IL}$ | – | – | −220 | μA | $V_{IN} = 0.4V$ |
| **BIT OUTPUTS** | | | | | |
| High level output voltage $V_{OH}$ | – | 5.0 | – | | No load |
| Low level output voltage $V_{OL}$ | – | 0.1 | – | | |
| High level output voltage $V_{OH}$ | 2.4 | – | – | V | $I_{IH} = -40\mu A$ |
| Low level output voltage $V_{OL}$ | – | – | 0.4 | V | $I_{IL} = 2.5mA$ |

Note 1: Speeds of up to 1.7MHz may be obtained by reducing the mark space ratio of the clock.

**ELECTRICAL CHARACTERISTICS** (Cont.)

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **CONTROL INPUTS** | | | | | |
| High level input voltage $V_{IH}$ | 2 | – | – | V | |
| Low level input voltage $V_{IL}$ | – | – | 0.8 | V | |
| High level input current $I_{IH}$ | – | – | –25 | μA | $V_{IN} = 2.4V$ |
| Low level input current $I_{IL}$ | – | – | –95 | μA | $V_{IN} = 0.4V$ |
| Reset pulse width | 200 | – | – | ns | |
| **Power supply** | | | | | |
| Supply voltage | 4.5 | 5 | 5.5 | V | |
| Supply current | – | 35 | 45 | mA | $V_{CC} = 5.5V$ |

## GENERAL CIRCUIT OPERATION

The ZN435 incorporates an 8-bit DAC based on a voltage switching R-2R ladder network. The reference voltage for this ladder may be derived from the on-chip precision bandgap reference, or an external reference voltage may be supplied.

The ZN435 also contains an 8-bit up/down counter and control logic. The DAC may receive its digital input data from the counter, the counter outputs being simultaneously available at an 8-bit I/O port. Alternatively the counter outputs may be inhibited and the I/O port used to feed data direct to the DAC inputs.

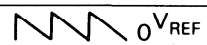
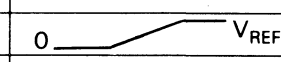
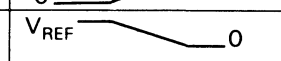
An on-chip oscillator is provided to drive the clock input of the up/down counter. The on-chip clock may be overridden by an external clock signal.

## UP/DOWN COUNTER AND CONTROL LOGIC

The counter is a high-speed, synchronous up/down type, whose operation is determined by four control pins. The functions of the UP, DOWN and RESET inputs are fairly self explanatory, the MODE input determines the behaviour of the counter at zero and full-scale. When the MODE input is high the counter will reset to zero if it is clocked past full-scale in the UP direction and will reset to 255 if it is clocked past zero in the DOWN direction. When the MODE input is low the counter will stop on reaching full-scale or zero.

The normally invalid state of UP and DOWN inputs low simultaneously is also utilised in the ZN435. With the MODE input high and UP and DOWN inputs low the counter will cycle up and down continuously, reversing at full-scale and zero. With all three control inputs low the counter outputs are disabled and the DAC inputs accessible from the I/O port.

A truth table for the control inputs is given in Table 1.

| Reset | Mode | Down | Up | Digital function | Analogue waveform |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | Counter stopped. |  |
| 1 | 1 | 1 | 0 | Count up continuously. |  |
| 1 | 1 | 0 | 1 | Count down continuously. |   |
| 1 | 1 | 0 | 0 | Count up, reverse at F.S., count down, reverse at zero. |   |
| 1 | 0 | 1 | 1 | Counter stopped. |  |
| 1 | 0 | 1 | 0 | Count up, stop at F.S. |   |
| 1 | 0 | 0 | 1 | Count down, stop at zero. |   |
| X | 0 | 0 | 0 | DAC mode, counter output disabled. Counter can still be reset by taking reset input low. |  |
| 0 | X | X | X | Counter reset. Does not affect analogue output in DAC mode. |  |

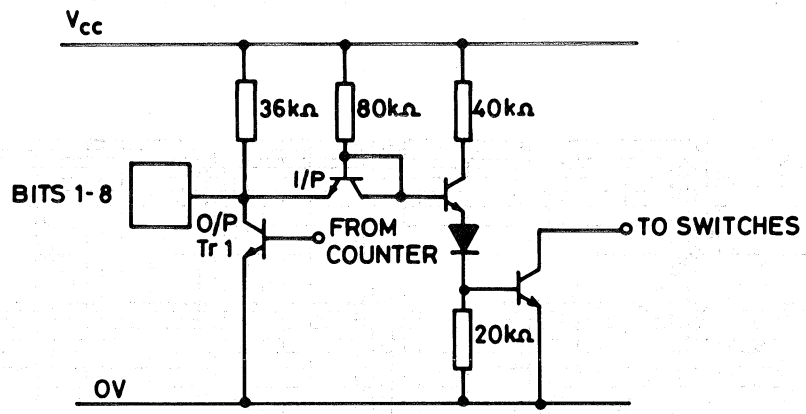



Fig. 2 Bit inputs/outputs

## DATA PORT

One bit of the data port is shown in Fig. 2. The input/output pin is the junction of the counter output buffer and the DAC input buffer.

Normally the DAC is driven from the counter and the counter data is also available at the port. However, when the counter outputs are disabled the output transistors are turned off and the DAC inputs may be accessed from the data port.

The data port can drive or be driven from B-series CMOS and all TTL families.

## CLOCK CIRCUIT

The on-chip clock circuit of the ZN435 is shown in Fig. 3.

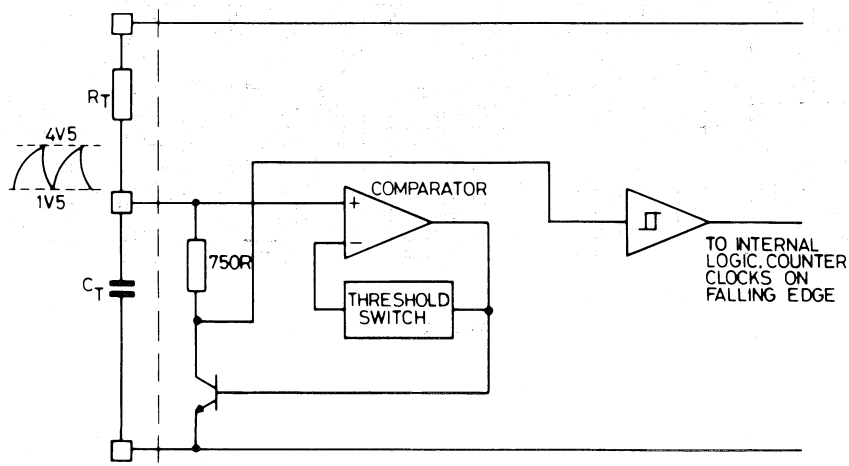



Fig. 3

The frequency of the clock is given by $f_{CLK} \simeq \frac{1}{2R_TC_T}$ (Hz, Ω, F)

Typical graphs of oscillator frequency versus resistor and capacitor values are given in Fig. 4.

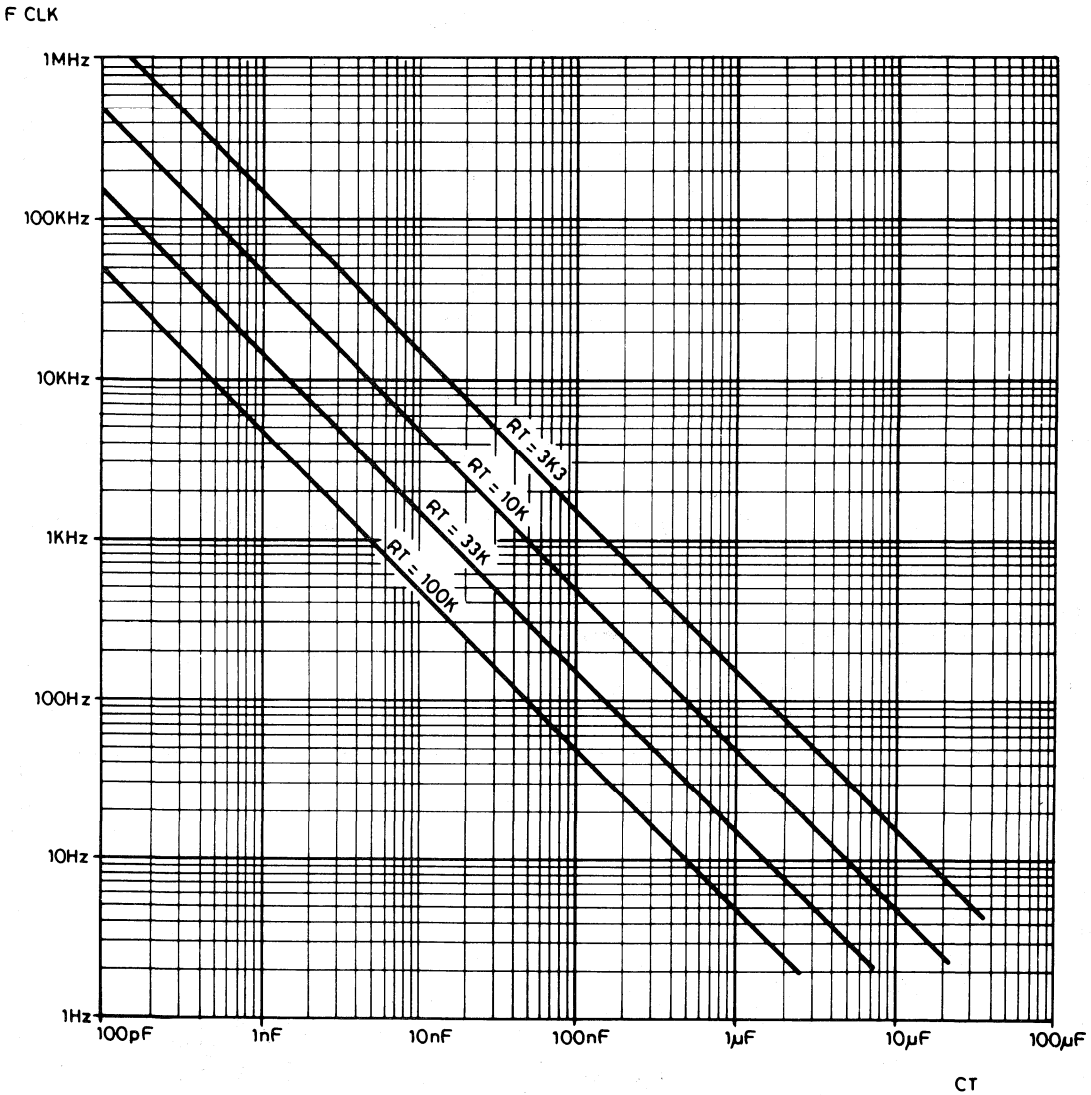



Fig. 4

The external capacitor $C_T$ is charged via the external resistor $R_T$ to the upper threshold of the comparator (about +4.5V with $V_{CC}$ = +5V). The comparator turns on the discharge transistor to discharge $C_T$ and switches its threshold to the lower value of about 1.5V. When the voltage on $C_T$ has fallen to this level the comparator turns off the discharge transistor and the cycle repeats.

The clock can be overdriven from either a TTL totem-pole output (Fig. 5a), an open collector output (Fig. 5b), or a CMOS gate (Fig. 5c). In all three cases the $V_{OH}$ of the driving gate must be attenuated to below 4.5V so that the internal discharge transistor is not turned on.

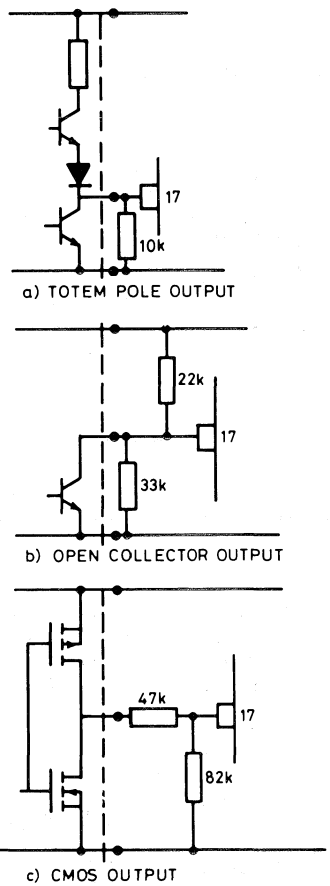



**Fig. 5 Overdriving the clock input**

## ANALOGUE CIRCUITS

### D-A converters

The DAC is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 6.

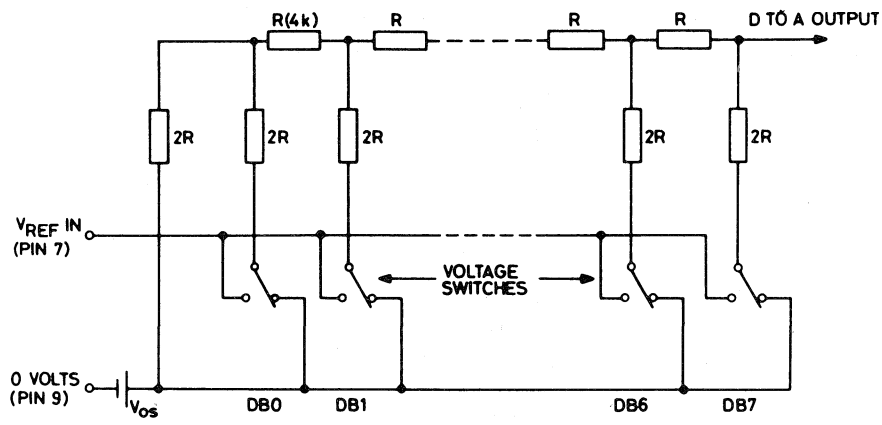



Fig. 6 R-2R ladder network

Each 2R element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (< 1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

$$V_{OUT} = \frac{n}{256} (V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input from the counter or data port.

$V_{OS}$ is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of $V_{OS}$ is typically 5mV.

This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is small the zero drift will be small. The DAC output range can be considered to be 0V to $V_{REF\ IN}$ with an output resistance R (4kΩ).

## REFERENCE

### On-chip reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V zener diode with a very low slope impedance (Fig. 7).

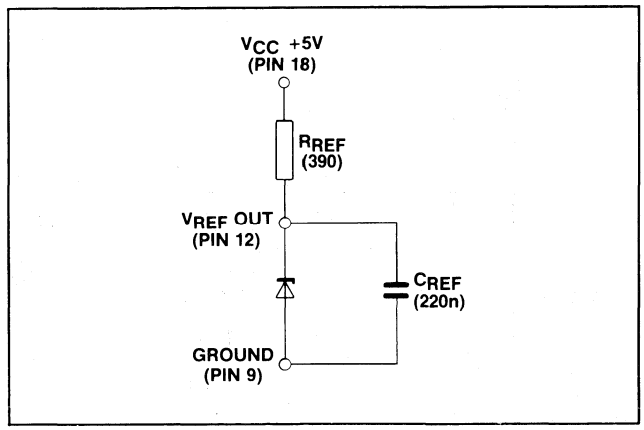



**Fig. 7 Internal voltage reference**

An external resistor ($R_{REF}$) should be connected between pins 12 and 18 to bias up the on-chip reference, whilst a stabilising/decoupling capacitor ($C_{REF}$) is required between pins 12 and 9.

To use the internal reference $V_{REF\ OUT}$ (pin 12) is connected to $V_{REF\ IN}$ (pin 10).

The recommended reference resistor of 390Ω will supply a nominal reference current of 6.4mA which is sufficient to drive the reference inputs of up to five ZN435's. Where several ZN435's are used in a system this useful feature can save up to four resistors and capacitors as well as reducing power consumption and giving excellent gain tracking.

## APPLICATIONS

The applications of the ZN435 are too many and varied to detail in this data sheet. However a few basic configurations are illustrated. It should be noted that there is a danger of obtaining incorrect codes if the up/down control lines change at the same time as the active negative edge of the clock. Therefore if these control lines are changing asynchronously then extra circuitry should be used to prevent them changing at the negative edge of the clock. This is best achieved by latching these signals using positive edge triggered D-type flip-flops as is demonstrated in the circuit diagrams of Figs. 9 and 10.

## WAVEFORM GENERATOR

The circuit of a low frequency waveform generator is illustrated in Fig. 8.

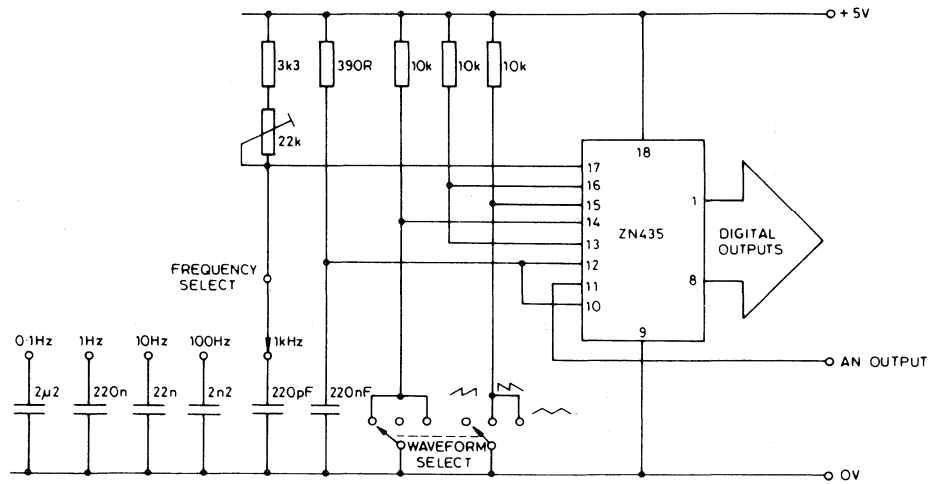



Fig. 8 Waveform generator

**Note:** The frequencies given above apply to the sawtooth waveforms. For the triangular waveforms divide the frequencies above by two.

This will produce stable, linear, sawtooth and triangle waveforms.

## RAMP AND COMPARE A-D CONVERTER

A simple ramp and compare A-D converter can be constructed using the ZN435 as shown below.

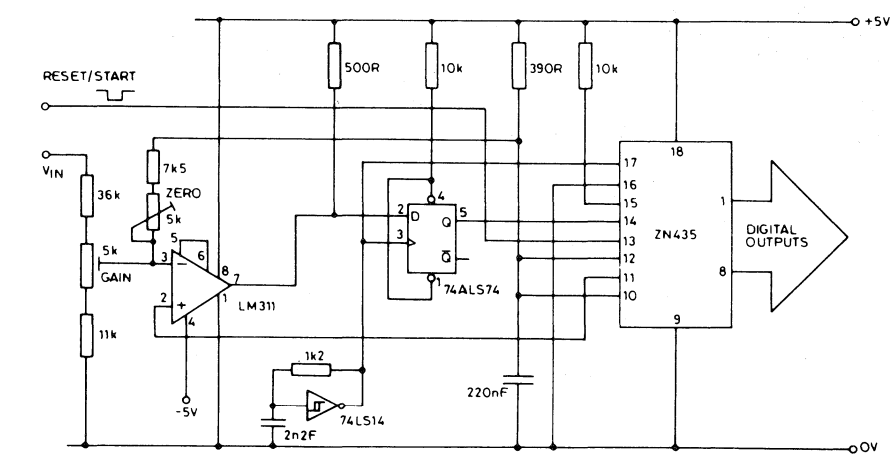



Fig. 9 Ramp and compare ADC

The counter is set to count up from zero, producing a positive going ramp at the analogue output. When the ramp voltage exceeds the analogue input the comparator output will go high, inhibiting the clock and stopping the counter. The converter can be reset and re-started by applying a low going pulse to the reset input. As the counter is constrained to count up only this circuit could also be used as an analogue peak detector. The analogue output of the ZN435 will hold indefinitely a voltage directly proportional to the highest applied input voltage.

The analogue input range is $\pm$ 10V. Other ranges may be accommodated by suitable choice of input resistors. Note that in this circuit the mode input is tied low to make the counter stop at full-scale. This prevents the counter cycling in the event of an overrange input.

Both this circuit and the following tracking converter circuit use high gain comparators. Therefore the usual precautions should be taken when constructing either circuit to prevent oscillation about the threshold, e.g. supply decoupling, careful track layout.

## TRACKING A-D CONVERTER

The on-chip up/down counter allows the ZN435 to be configured as a tracking A-D converter, as shown in Fig. 10.

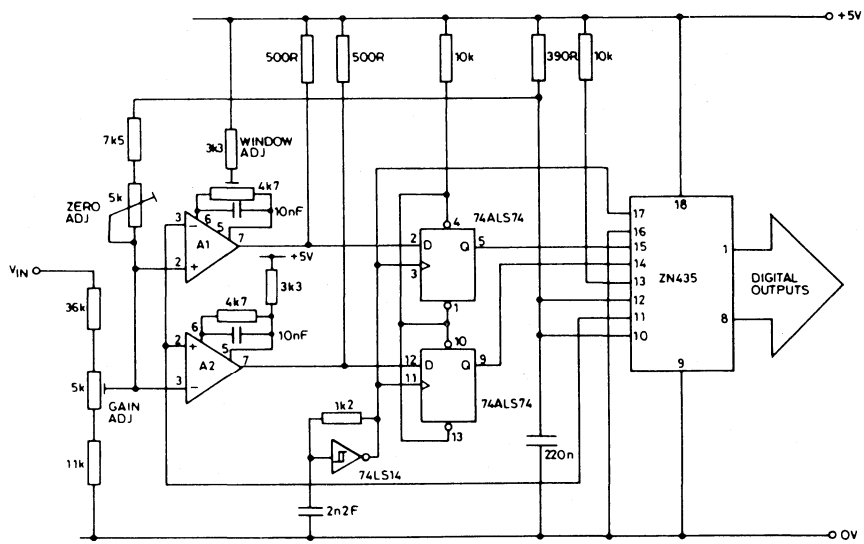



Fig. 10 Tracking ADC

In this circuit two LM311 op-amps are used to make a window comparator. This has a dead-band equal to one LSB of the DAC output (10mV), which is set by adjusting the offset of A1 until its threshold is 10mV above that of A2. This is easily achieved by applying a stable voltage at the input. Then with the ZN435 removed, applying a variable voltage to pin 11 on the ZN435 socket. By varying this voltage and monitoring the op-amp outputs the window can be adjusted so that the threshold of A1 is 10mV above that of A2.

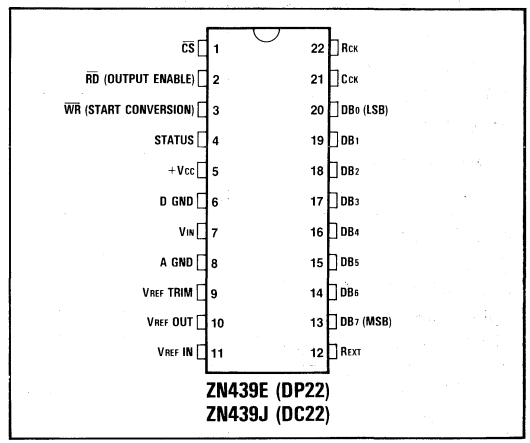
Whenever the analogue voltage is above the threshold of A2 the counter will count up so that the DAC output increases to follow the analogue voltage. Whenever the analogue voltage is below the threshold of A1 the counter will count down so that the DAC output decreases to follow the analogue voltage. When the analogue voltage is between the two thresholds the outputs of A1 and A2 will be high and the counter will be stopped. Again the input voltage range is $\pm$ 10V, other ranges being possible by suitable choice of input resistors.

# ZN439

## 8-BIT MICROPROCESSOR COMPATIBLE A-D CONVERTER

The ZN439 is an 8-bit successive approximation A-D converter, designed to be easily interfaced to microprocessors. All active circuitry is contained on-chip including clock generator trimmable 2.5V bandgap reference, control logic and double buffered latches with three-state outputs.

These features give extra flexibility in use, with just three inputs to control all ADC operations and double buffered output latches which will allow data to be read at any time irrespective of the status of the converter.




**Pin connections - top view**

### FEATURES

- Choice of Linearity: ¼ LSB - ZN439-9, ½ LSB - ZN439-8, 1 LSB - ZN439-7
- 5 microseconds Conversion Time
- Microprocessor, TTL and CMOS Compatible
- On-Chip Clock
- Trimmable Bandgap Reference
- Versatile Microprocessor Interfacing with Double Buffered Output Latch
- Equally Suitable for Stand-Alone Applications
- ROM Type Operation
- Commercial or Military Temperature Ranges

### ORDERING INFORMATION

| Device type | Linearity error(LSB) | Operating temperature | Package |
|---|---|---|---|
| ZN439J9 | ¼ | –55°C to +125°C | DC22 |
| ZN439E8 | ½ | 0°C to +70°C | DP22 |
| ZN439J8 | ½ | –55°C to +125°C | DC22 |
| ZN439J7 | 1 | –55°C to +125°C | DC22 |

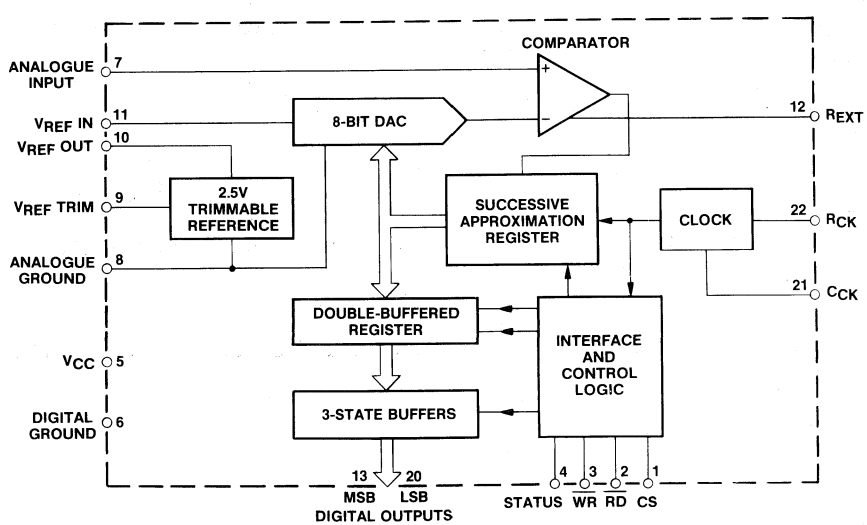



**Fig.1 System diagram**

**ELECTRICAL CHARACTERISTICS** (at $V_{CC} = 5V$, $T_{amb} = 25°C$ and $f_{CLK} = 1.6MHz$ unless otherwise specified).

| Parameter | $T_{amb} = +25°C$ | | | Over specified Temp. range | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| **ZN439-9** | | | | | | | |
| Linearity error | – | – | ±0.25 | – | ±0.25 | LSB | |
| Differential linearity error | – | – | ±0.5 | – | ±0.5 | LSB | |
| **ZN439-8** | | | | | | | |
| Linearity error | – | – | ±0.5 | – | ±0.5 | LSB | |
| Differential linearity error | – | – | ±0.75 | – | ±0.75 | LSB | |
| **ZN439-7** | | | | | | | |
| Linearity error | – | – | ±1 | – | ±1 | LSB | |
| Differential linearity error | – | – | ±1 | – | ±1 | LSB | |
| **ALL TYPES** | | | | | | | |
| Zero transition | – | 7 | – | – | – | mV | ZN439E |
| (00000000→00000001) | – | 7 | – | – | – | mV | ZN439J |
| Full-scale transition | – | 2.550 | – | – | – | V | ZN439E |
| (11111110→11111111) | – | 2.550 | – | – | – | V | ZN439J |
| Linearity temperature coefficient | | ±3 typ. | | | | ppm/°C | Ext. Ref. |
| Differential linearity temperature coefficient | | ±6 typ. | | | | ppm/°C | |
| Gain temperature coefficient | | ±10 typ. | | | | ppm/°C | |
| Offset temperature coefficient | | ±7 typ. | | | | ppm/°C | |
| Resolution | 8 | – | – | – | – | Bits | |
| Conversion time | 5 | – | – | – | – | µs | |
| Supply rejection | – | 0.2 | – | – | – | %/V | |
| Supply voltage | 4.5 | 5.0 | 5.5 | 4.5 | 5.5 | V | |
| Supply current | – | 30 | 45 | – | – | mA | Outputs in high impedance state |
| Power consumption | – | 150 | 225 | – | – | mW | |
| Reference input range | 1.5 | – | 3.0 | – | – | V | |
| Ladder output impedance | – | 2.7 | – | – | – | kΩ | |
| **COMPARATOR** | | | | | | | |
| Input current | – | 1.0 | – | – | – | µA | $V_{in} = +3V$, $R_{ext} = 82K$ |
| Input resistance | – | 100 | – | – | – | kΩ | |
| Tail current | 25 | – | 150 | 25 | 150 | µA | $R_{ext} = 82K$, $V- = -5V$ |
| Negative supply | −3 | −5 | −30 | −3 | −30 | V | |
| Input voltage | −0.5 | – | +3.5 | −0.5 | +3.5 | V | |

**ELECTRICAL CHARACTERISTICS** (Cont.)

| Parameter | $T_{amb} = +25°C$ | | | Over specified Temp. range | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| **INTERNAL VOLTAGE REFERENCE** | | | | | | | |
| Output voltage | – | 2.588 | – | – | – | V | PIN 9 NC<br>$R_{REF} = 1.6K$<br>$C_{REF} = 0.47\mu F$ |
| Output voltage tolerance | – | – | ±3 | – | – | % | |
| Slope impedance | – | 0.75 | – | – | – | Ω | |
| Reference current | 0.25 | – | 5.2 | 0.25 | 5.2 | mA | |
| Trim range | ±5 | – | – | ±5 | – | % | $R_{TRIM} = 10K$ |
| Output voltage temperature coefficient | – | 70 | – | – | – | ppm/°C | At 5mA operating current (worst case) 25ppm at 2.0mA |
| **CLOCK** | | | | | | | |
| Maximum on-chip clock frequency | – | 1.6 | – | – | – | MHz | $R_{ck} = 1.5K\Omega$<br>$C_{ck} = 100pF$<br>(See Fig. 13) |
| Clock frequency tempco | – | −0.1 | – | – | – | %/°C | |
| Clock capacitor | 100 | – | – | – | – | pF | |
| Clock resistor | 1.0 | – | – | – | – | kΩ | |
| Maximum external clock frequency | 2 | – | – | 2 | – | MHz | |
| Clock pulse width | 250 | – | – | – | – | ns | |
| High level I/P voltage $V_{IH}$ | 3.5 | – | – | 3.5 | – | V | |
| Low level I/P voltage $V_{IL}$ | – | – | 0.8 | – | 0.8 | V | |
| High level I/P current $I_{IH}$ | – | 1 | – | – | – | μA | $V_{CC} - 5.5V$<br>$V_{IN} = 4V$ |
| Low level I/P current $I_{IL}$ | – | 10 | – | – | – | nA | $V_{CC} = 5.5V$<br>$V_{IN} = 0.8V$ |
| Supply rejection | – | 3.5 | – | – | – | %/V | Int. clock Freq. |
| **LOGIC $\overline{WR}$ + $\overline{CS}$ INPUTS** | | | | | | | |
| High level I/P voltage $V_{IH}$ | 2 | – | – | 2 | – | V | |
| Low level I/P voltage $V_{IL}$ | – | – | 0.8 | – | 0.8 | V | |
| High level I/P current $I_{IH}$ | – | 40 | – | – | – | μA | $V_{CC} = +5.5V$<br>$V_{IN} = +5.5V$ |
| High level I/P current $I_{IH}$ | – | 20 | – | – | – | μA | $V_{CC} = +5.5V$<br>$V_{IN} = +2.4V$ |
| Low level I/P current $I_{IL}$ | – | −50 | – | – | – | μA | $V_{CC} = +5.5V$<br>$V_{IN} = +0.4V$ |
| **LOGIC $\overline{RD}$ INPUT** | | | | | | | |
| High level I/P voltage $V_{IH}$ | 2 | – | – | 2 | – | V | |
| Low level I/P voltage $V_{IL}$ | – | – | 0.8 | – | 0.8 | V | |
| High level I/P current $I_{IH}$ | – | 220 | – | – | – | μA | $V_{CC} = +5.5V$<br>$V_{IN} = +5.5V$ |

**ELECTRICAL CHARACTERISTICS** (Cont.)

| Parameter | $T_{amb} = +25°C$ | | | Over specified Temp. range | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| High level I/P current $I_{IH}$ | – | 120 | – | – | – | μA | $V_{CC} = +5.5V$ $V_{IN} = +2.4V$ |
| Low level I/P current $I_{IL}$ | – | −370 | – | – | – | μA | $V_{CC} = +5.5V$ $V_{IN} = +0.4V$ |
| **DATA AND STATUS OUTPUTS** | | | | | | | |
| High level output voltage $V_{OH}$ | 2.4 | – | – | 2.4 | – | V | $I_{OH\ MAX}$ |
| Low level output voltage $V_{OL}$ | – | – | 0.4 | – | 0.4 | V | $I_{OL\ MAX}$ |
| High level output current $I_{OH}$ | – | – | −800 | – | – | μA | |
| Low level output current $I_{OL}$ | – | – | 2 | – | – | mA | |
| Three-state disable output leakage current | – | – | 2.0 | – | – | μA | $V_{OUT} = 0.4V$ |
| (Data output only) | – | – | 2.0 | – | – | μA | $V_{OUT} = 2.4V$ |
| Enable/disable Delay times $T_{E1}$ | 90 | 120 | 160 | – | – | ns | |
| $T_{E0}$ | 60 | 100 | 120 | – | – | ns | |
| $T_{D1}$ | 80 | 120 | 160 | – | – | ns | |
| $T_{D0}$ | 60 | 80 | 110 | – | – | ns | |
| Write pulse width | 150 | – | – | – | – | ns | |
| WR input to status O/P high | – | 280 | 350 | – | – | ns | |
| Read pulse width | 160 | – | – | – | – | ns | |
| Read input high to status output high | – | 240 | 400 | – | – | ns | |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | +7V |
| Maximum voltage, logice and $V_{REF}$ inputs, $A_{IN}$ | $V_{CC}$, −0.5V |
| Operating temperature range | 0°C to +70°C (ZN439E)<br>−55°C to +125°C (ZN439J) |
| Storage temperature range | −55°C to +125°C |

## GENERAL CIRCUIT OPERATION

The ZN439 utilises the successive approximation technique to produce an 8-bit parallel digital output. Upon receipt of a negative going pulse on the $\overline{WR}$ input the status output goes high, and the DAC input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. If the analogue input is larger, the MSB is left in circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all the 8 bits have been compared. On the 8th negative clock edge status goes low indicating that the conversion is complete.

The double-buffered register means the outputs can be enabled at any time, irrespective of the conversion status, and valid data will always be presented to the data bus. **Therefore the $\overline{RD}$ signal can be completely asynchronous with respect to the status.** Data can be read by taking $\overline{RD}$ low, thus enabling the three-state outputs. $\overline{RD}$ cannot be tied low as this will prevent the converter from updating it's outputs at the end of a conversion.

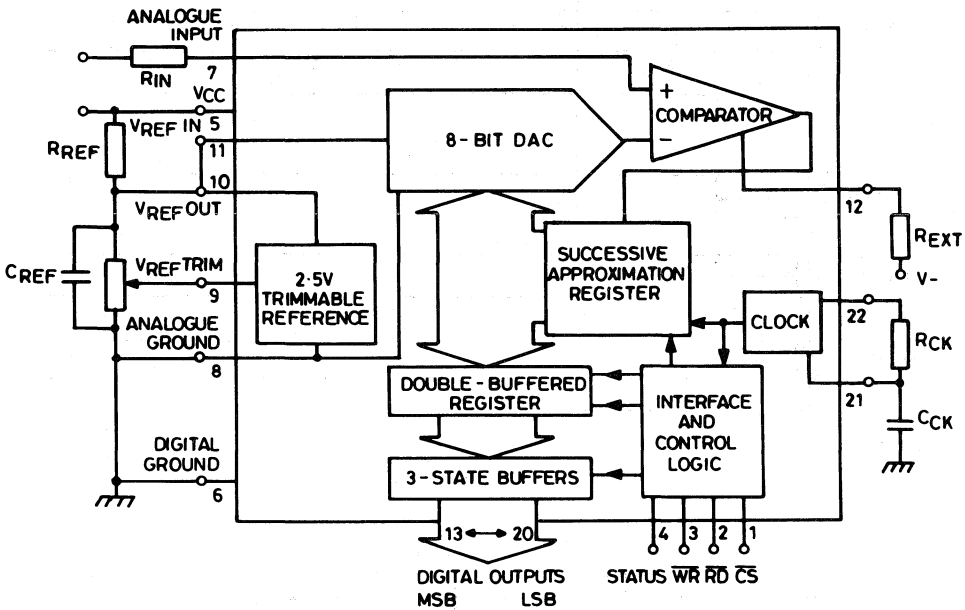



Fig. 2 Typical external components

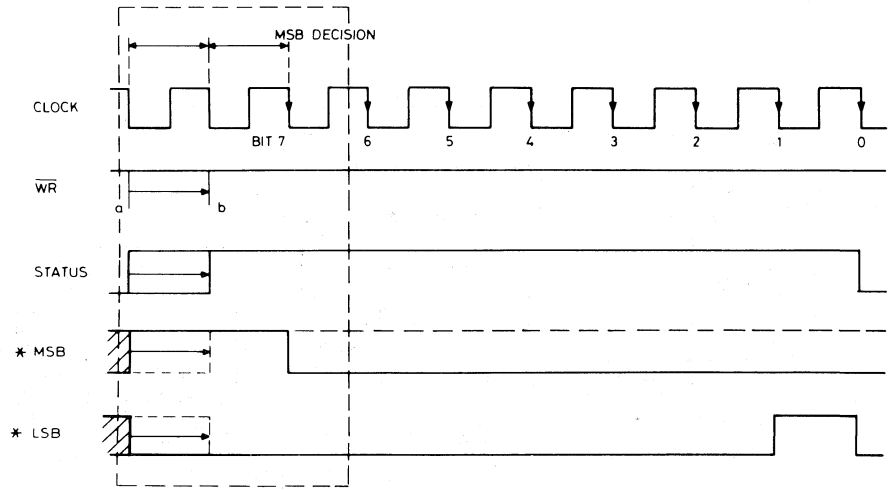
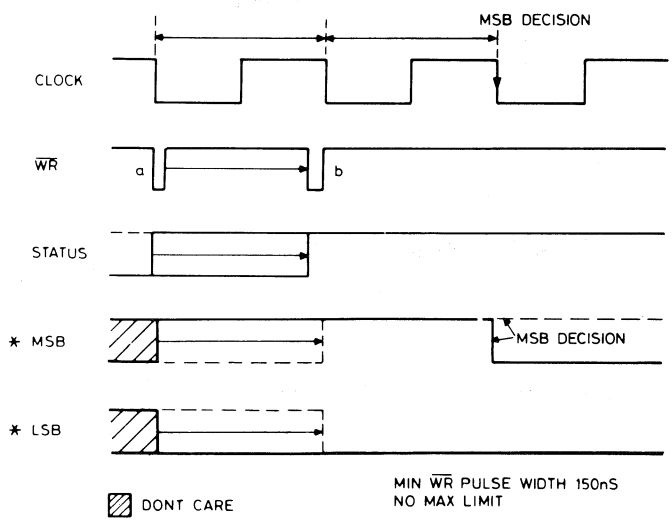



Fig. 3a




*Note: These signals are the internal MSB and LSB of the successive approximation register.

Fig. 3b (expanded inset)

Fig. 3 Timing diagram

## CONVERSION TIMING

The ZN439 will accept a low going convert ($\overline{WR}$) pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 8 and up to 9 clock pulses later depending on the relative timing of the clock and convert signals. Timing diagrams for a conversion are shown in Fig. 3.

The ZN439 is first selected by taking $\overline{CS}$ (chip select) low. The converter is cleared by a low going convert ($\overline{WR}$) pulse, which sets the most significant bit and the status while resetting all other bits. Holding the $\overline{WR}$ input low will not inhibit the operation of the device.

The convert ($\overline{WR}$) pulse can be as short as 150ns; however the MSB must be allowed to settle for at least 625ns before the MSB decision is made. To ensure that this criterion is met even with short write pulses the converter waits for a falling clock edge before commencing with the conversion. This ensures that the MSB is allowed to settle for at least a full clock period or 625ns at maximum clock frequency. If the $\overline{WR}$ input is pulsed low at any time the conversion will restart. The input signals can be locked out during a conversion by removing the $\overline{CS}$ signal. This will isolate the converter from the external signals around it.

The status output goes low at the end of a conversion indicating that new data is now available. Internal logic monitors the $\overline{WR}$ input and if at the end of a conversion the $\overline{WR}$ input is high the clock signal will be locked out of the converter leaving it set up (i.e. the code 10000000 will appear on the input to the DAC) and waiting for its next convert ($\overline{WR}$) pulse. If the $\overline{WR}$ input is low the clock signal will not be inhibited allowing the converter to procede with another conversion. The double buffering on the three-state data outputs gives extra flexibility allowing the $\overline{RD}$ input to operate completely asynchronously with respect to the status and always produce valid data. Note that the $\overline{RD}$ input cannot be tied low as this will prevent the converter from updating at the end of a conversion.

## CONTINUOUS CONVERSION

The ZN439 can be made to cycle by simply tying the $\overline{CS}$ and $\overline{WR}$ inputs low. It should be noted that after power up, valid data will only be available after the internal reference has stabilised. This time will depend upon the values of the reference decoupling capacitor and load resistor, but will be approximately 2mS for a 1K6 resistor and a 0.47$\mu$F capacitor.

A timing diagram for the continuous conversion mode is shown in Fig. 5 (overleaf).

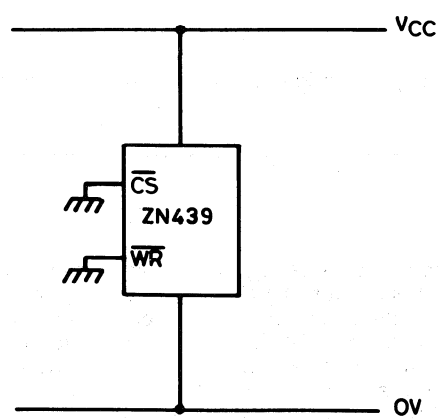



**Fig. 4 Circuit for continuous conversion**

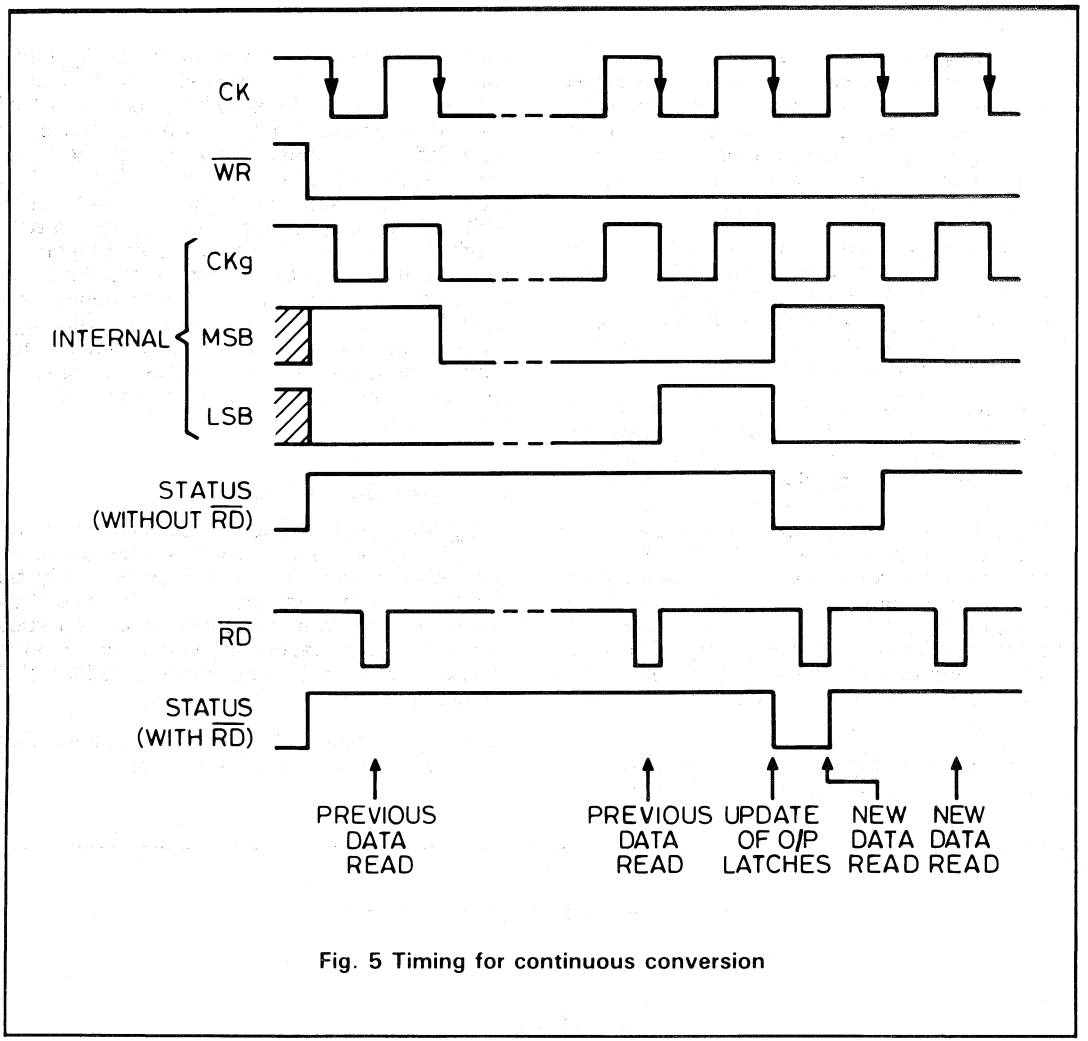



Fig. 5 Timing for continuous conversion

## INTERRUPT DRIVEN

The ZN439 can also be used in an interrupt driven mode by using the status output. A WR pulse initiates a conversion sending the status high. The high to low transition of the STATUS output, indicating the end of a conversion, can be used as an interrupt signal by the microprocessor i.e. informing the microprocessor that a conversion has been completed. On receiving the interrupt the microprocessor sends out an RD pulse to take in the new data. On the rising edge of the RD pulse data is latched into the microprocessor and internal control logic forces the status output high hence removing the interrupt signal.

A timing diagram for the interrupt driven mode is shown in Fig. 6.

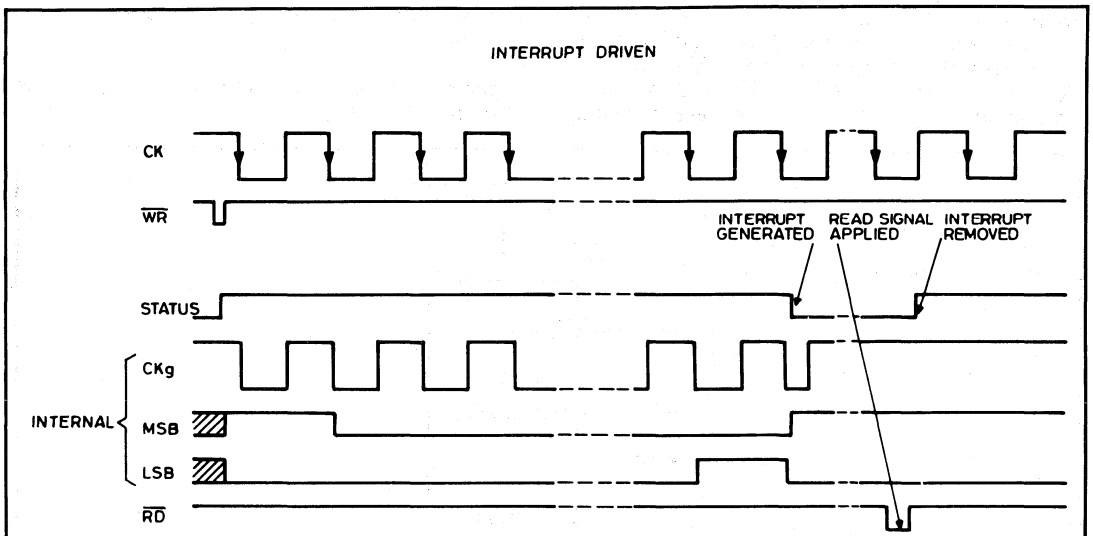



Fig. 6 Timing for interrupt driven mode

## 'STAND ALONE' OPERATION

The ZN439 is equally suitable for stand alone applications containing an on-chip clock and a 2.5V trimmable bandgap reference.

A typical circuit for unipolar operation is shown in Fig. 7a.

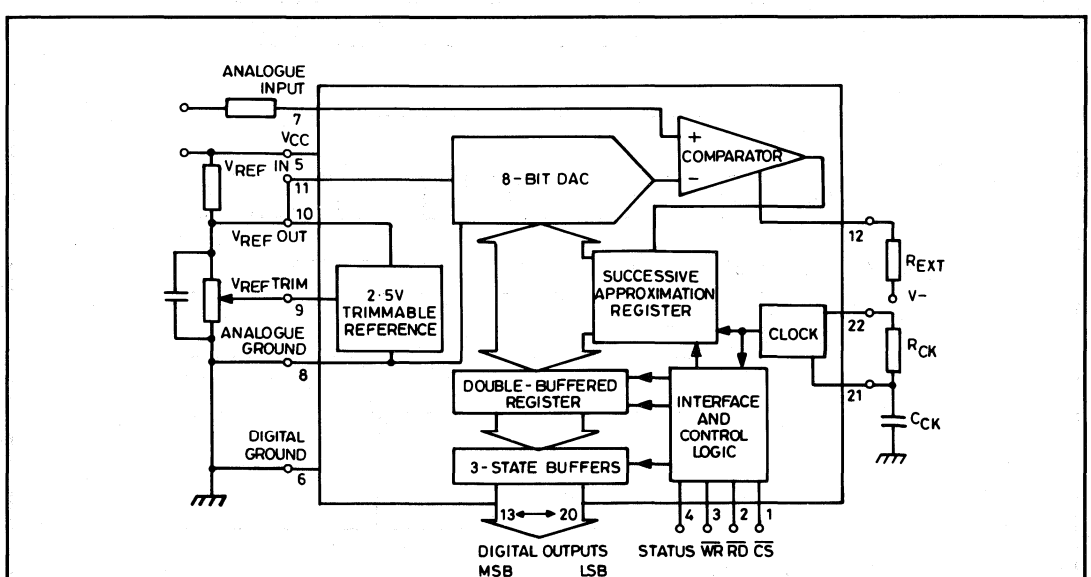



Fig. 7a Unipolar operation

By tying the $\overline{WR}$ and $\overline{CS}$ inputs low the device can be made to cycle. Also if the status output is connected via an inverter to the $\overline{RD}$ input the device can be updated at the end of each conversion and the output buffers enabled without the need for extra external control signals.

A timing diagram for stand alone operation is shown in Fig. 8.

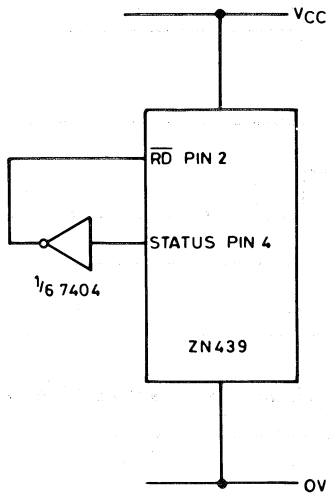
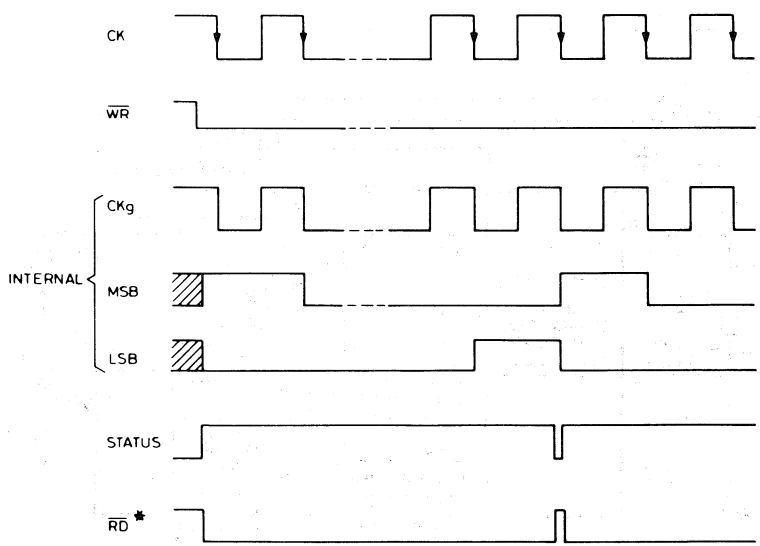



**Fig. 7b Circuit for updating 'stand alone' converter**




*Data valid while read is low subject to three-state delays

**Fig. 8 Timing for 'stand alone' operation**

## DATA OUTPUTS

The data outputs are provided with three-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig. 9. Whilst the $\overline{RD}$ input is high both output transistors are off and the device presents only a high impedance load to the bus. When $\overline{RD}$ is low the data outputs will assume the logic states present on the outputs of the double buffered register.

A test circuit and timing diagram for the output enable/disable delays are given in Fig. 10 (overleaf).

The status output utilises the same active pull-up as the data outputs for CMOS/TTL compatibility.

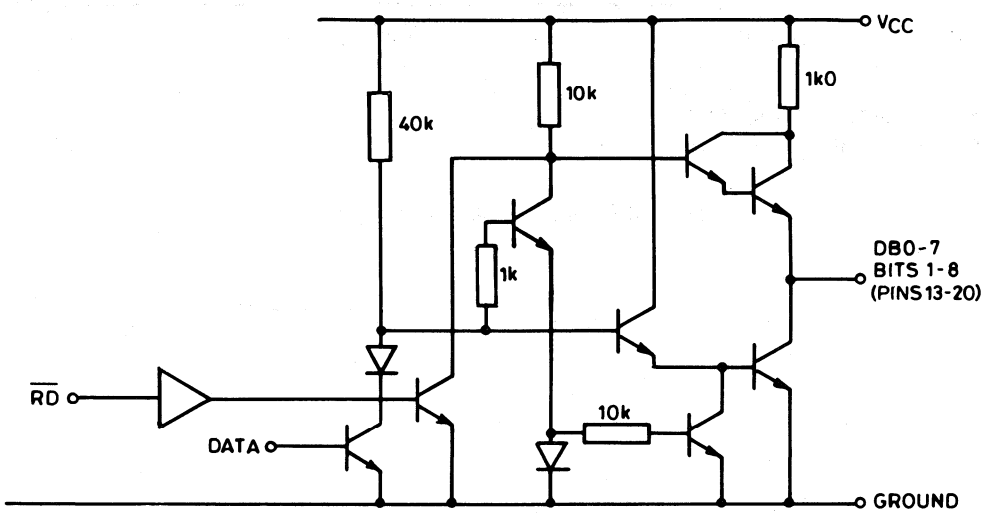
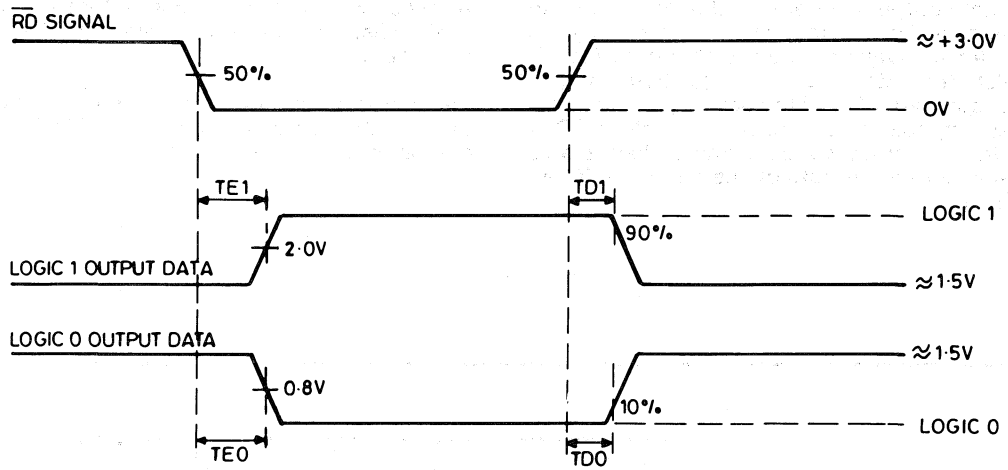



**Fig. 9 Data outputs**




TE = RD ENABLE DELAY TIME
TD = RD DISABLE DELAY TIME

Fig. 10a Output enable/disable delays

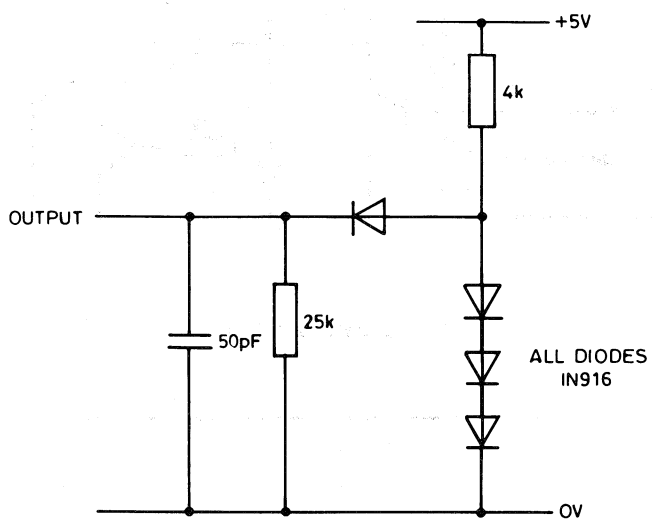



Fig. 10b Output load circuit

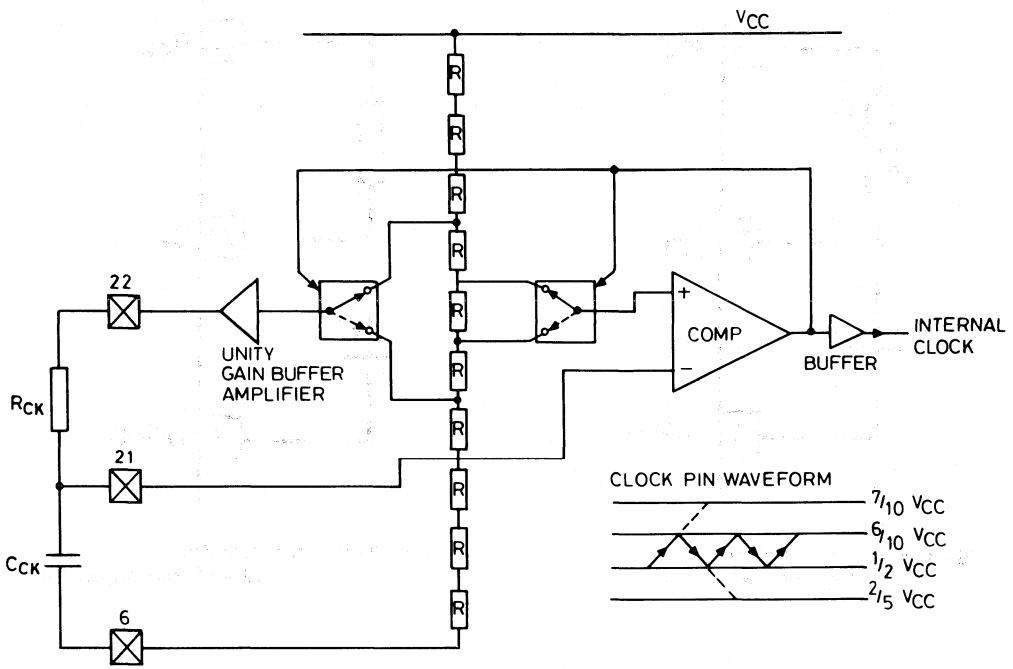



**Fig. 11 Clock oscillator circuit**

## ON-CHIP CLOCK

The ZN439 on-chip clock oscillator operates with only two external components; a resistor connected between pin 21 and pin 22 and a capacitor between pin 21 and pin 6. The clock oscillator circuit and the external component connections are shown in Fig. 11.

The oscillator frequency may be varied with the aid of a potentiometer or variable capacitor as shown in Fig. 12a and Fig. 12b. Alternatively it is possible to overdrive the oscillator input with an external clock signal from a TTL or CMOS gate as shown in Fig. 12c.

A graph of oscillator frequency against capacitor and resistor values is given in Fig. 13.

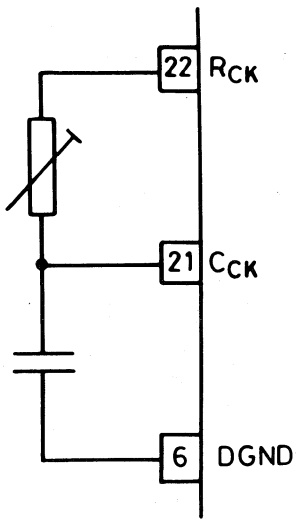



Fig. 12a Fixed capacitor + fixed/variable resistor

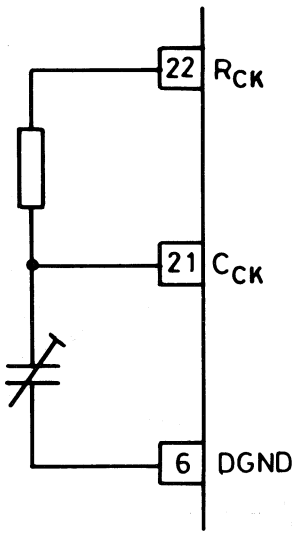



Fig. 12b Fixed resistor + fixed/variable capacitor

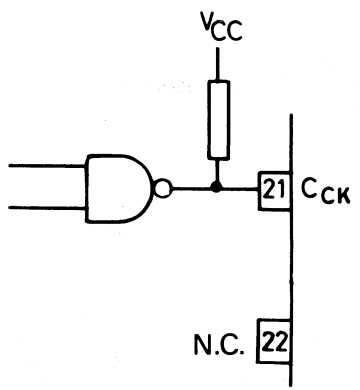



Fig. 12c External TTL or CMOS drive

Fig. 12 Clock circuit external components

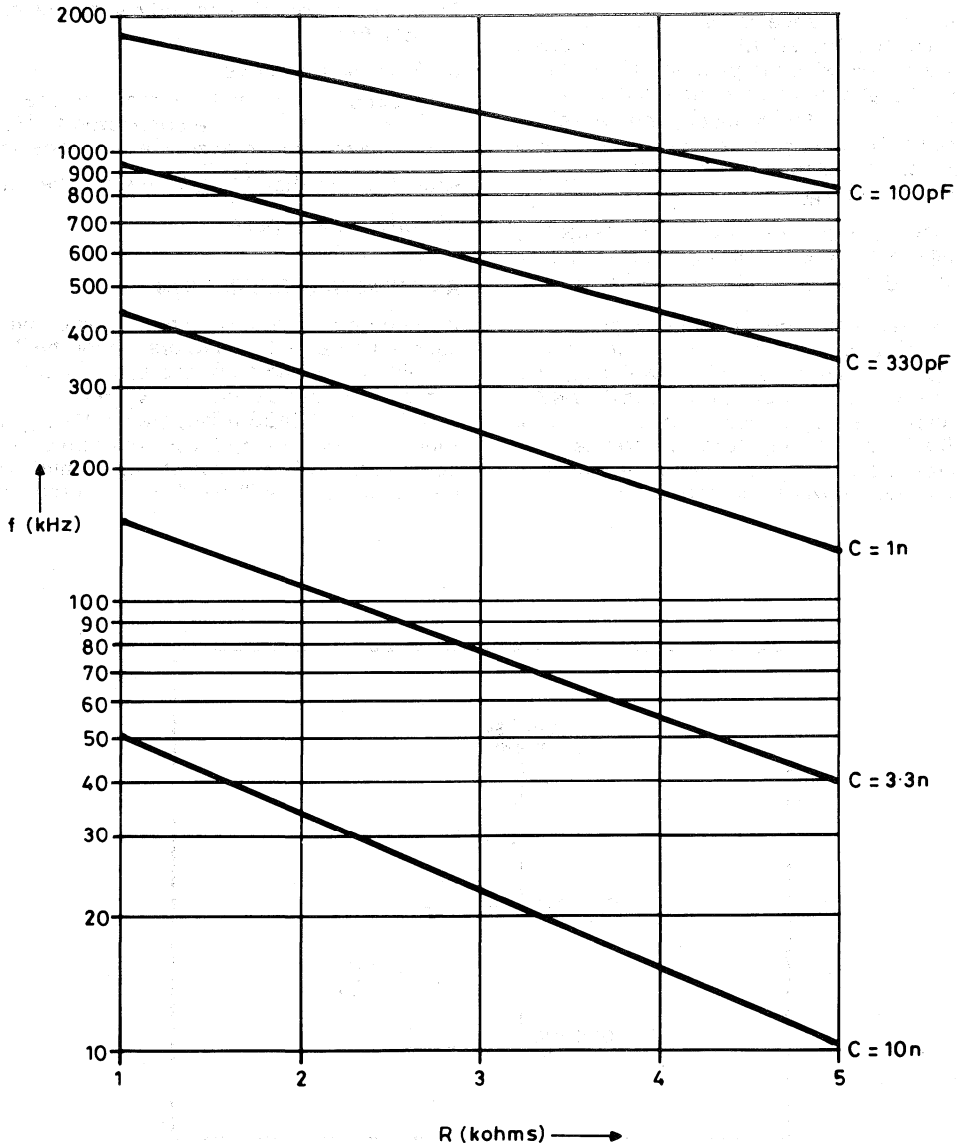



Fig. 13 Typical clock frequency v R. and C. values

## ANALOGUE CIRCUITS

### REFERENCE

**(a) Internal reference**

The internal reference is an active bandgap circuit which is equivalent to a 2.5 Zener diode with a very low slope impedance (Fig. 14). A resistor ($R_{REF}$) should be connected between $V_{CC}$ and $V_{REF\ OUT}$, and a decoupling capacitor, $C_{REF}$ (0.47$\mu$F), is required between $V_{REF\ OUT}$ and AGND. For internal reference operation $V_{REF\ OUT}$ is connected to $V_{REF\ IN}$.

A suitable current to drive one ZN439 is nominally 1.5mA and will be supplied by an $R_{REF}$ of 1K6 [(5 – 2.56)/1K6 = 1.5mA].

If the reference is required to drive more than one ZN439 then the reference current can be increased e.g. an $R_{REF} = 470\Omega$ will supply a nominal reference current of (5 – 2.56)/0.47 = 5.2mA and this may be used to drive up to four ZN439's from just one internal reference. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively with $R_{REF} = 680\Omega$, the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 1.5mA.

**(b) External reference**

If required an external reference in the range +1.5 to +3.0V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

### RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN439 should be derived from the same supply. The external reference can vary from +1.5 to +3.0V. The ZN439 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

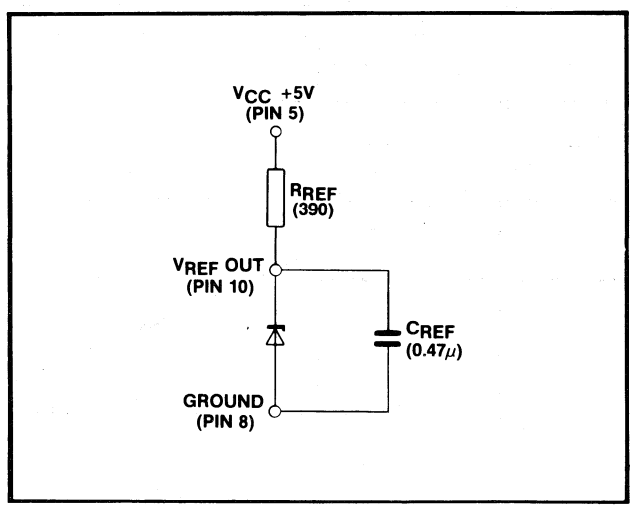



Fig. 14 Internal voltage reference

## COMPARATOR

The ZN439 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 15. A negative supply voltage is required to supply the tail current of the comparator. However as this is only 25 to 150$\mu$A and need not be well stablised it can be supplied by a simple diode pump circuit driven from the $R_{CK}$ pin (pin 22).

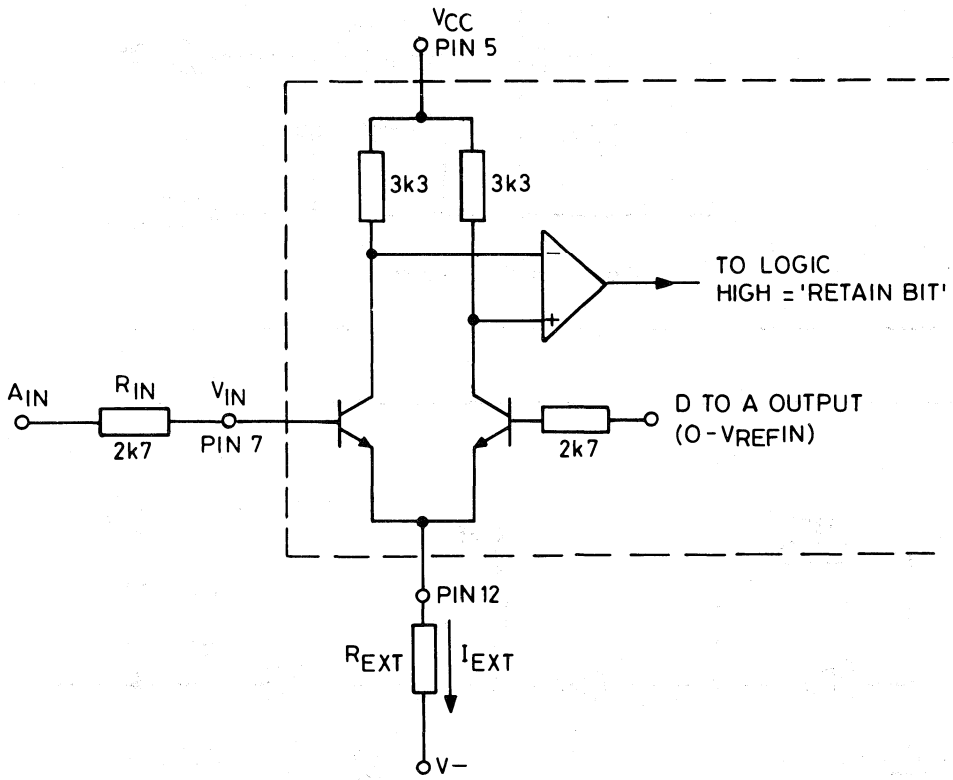



**Fig. 15 Comparator equivalent circuit**

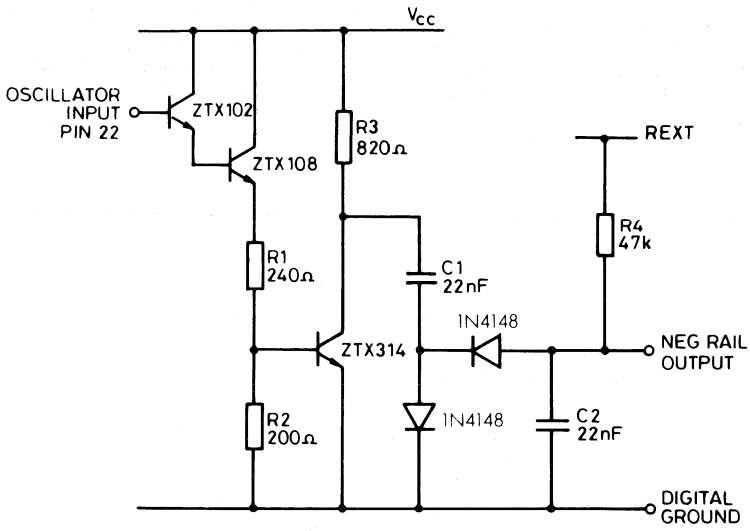



Fig. 16 Diode pump circuit

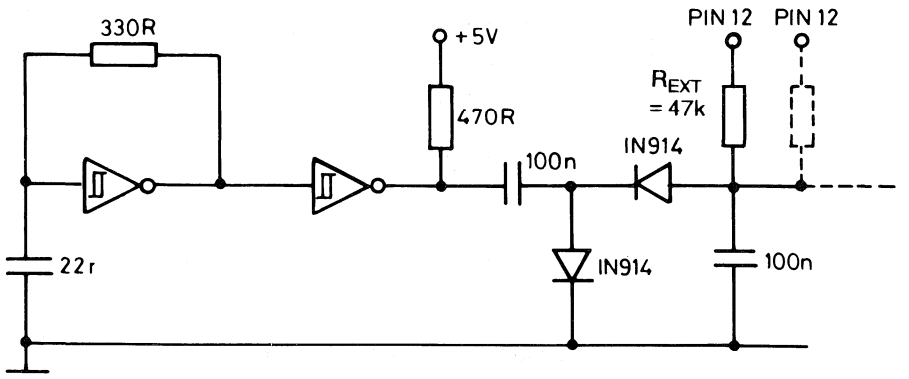



Fig. 17 Diode pump circuit to supply comparator tail current for up to five ZN439's

A suitable circuit is shown in Fig. 16. This circuit can be used in any converter operation mode. The diode pump circuit shown in Fig. 16 is driven by the on-chip clock (pin 22) and applies a voltage of about −3V to R4, thus providing the tail current for the comparator.

Where several ZN439's are used in a system the self-oscillating diode pump circuit of Fig. 17 is recommended. Alternatively, if a negative supply is available in the system then this may be utilised. A list of suitable resistors for different supply voltages is given in Table 1.

Table 1

| $V_-$ (volts) | $R_{EXT}$ (kΩ) |
|---|---|
| 3 | 47 |
| 5 | 82 |
| 10 | 150 |
| 12 | 180 |
| 15 | 220 |
| 20 | 330 |
| 25 | 390 |
| 30 | 470 |

## D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 18. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{D-A output} = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the D-A from the successive approximation register.

$V_{OS}$ is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally by removed by the setting up procedure and since the offset temperature coefficient is low (7ppm/°C) the effect on accuracy will be negligible.

The D-A output range can be considered to be $0 - V_{REF\ IN}$ through an output resistance R(2k7).

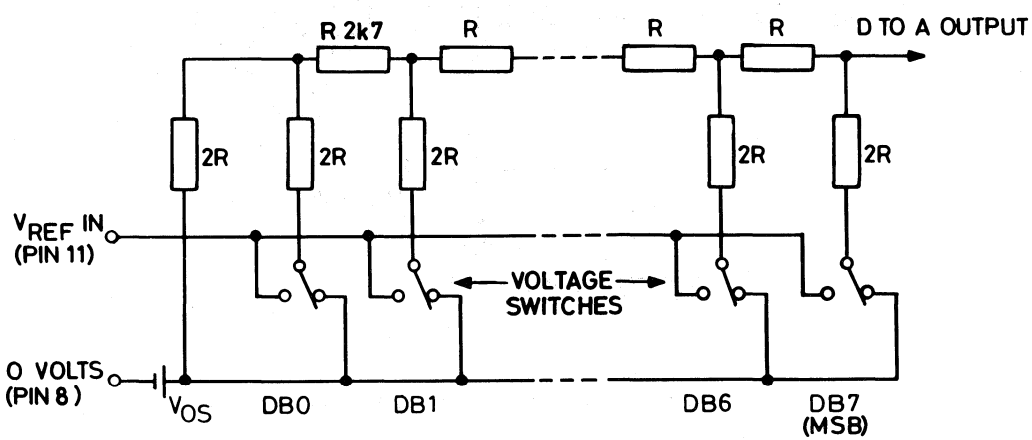
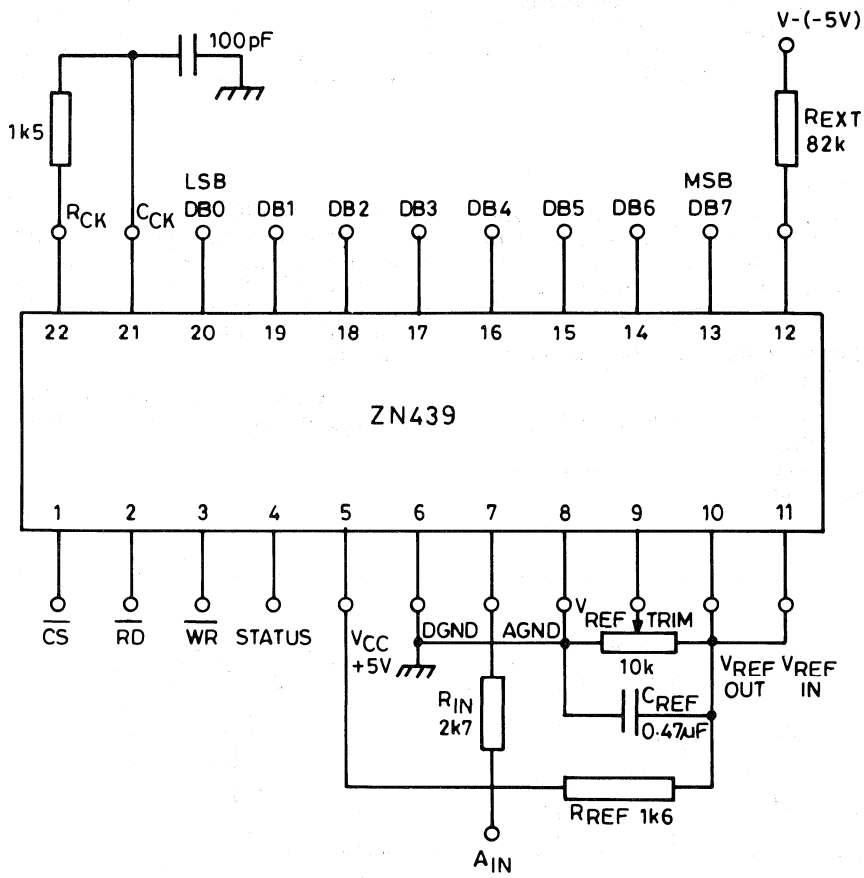



Fig. 18 R-2R ladder network

## ANALOGUE INPUT RANGES

The basic connection of the ZN439 shown in Fig. 19 has an analogue input range 0 to $V_{REF\,IN}$ which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analogue input ranges so that the comparator always sees a positive input voltage.




Nominal $A_{IN}$ range = 0 to $V_{REF\,IN}$

Fig. 19 External components for basic operation

## UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig. 20.

The values of $R_1$ and $R_2$ are chosen so that $V_{IN} = V_{REF\ IN}$ when the analogue input ($A_{IN}$) is at full-scale.

The resulting full-scale range is given by: $A_{IN}FS = \left(1 + \frac{R_1}{R_2}\right)$, $V_{REF\ IN} = G.V_{REF\ IN}$.

To match the ladder resistance $R_1/R_2$ ($R_{IN}$) = 2.7k.

The required nominal values of $R_1$ and $R_2$ are given by $R_1 = 2.7Gk$, $R_2 = \frac{2.7G}{G-1}$ k

Using these relationships a table of nominal values of $R_1$ and $R_2$ can be constructed for $V_{REF\ IN} = 2.5V$.

| Input range | G | $R_1$ | $R_2$ |
|---|---|---|---|
| +5V | 2 | 5.4k | 5.4k |
| +10V | 4 | 10.8k | 3.6k |

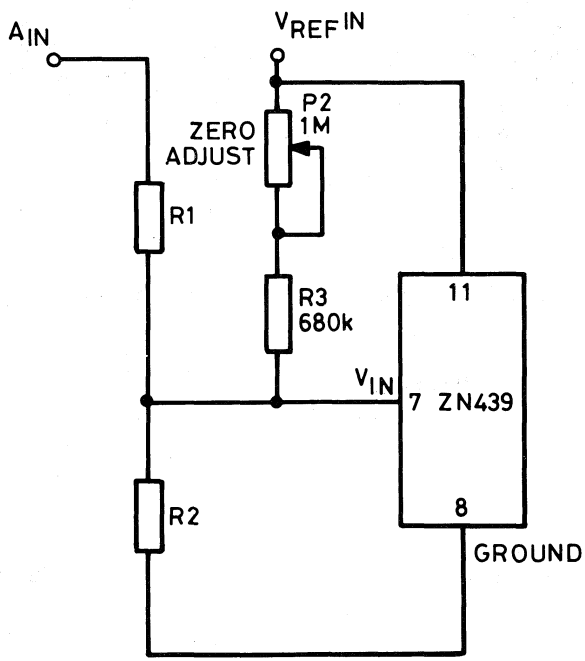



Fig. 20 General unipolar input connections

## GAIN ADJUSTMENT

Due to tolerances in $R_1$ and $R_2$, tolerances in $V_{REF}$ and the gain (full-scale) error of the DAC, some adjustment should be incorporated into $R_1$ to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting $R_1$ by at least $\pm 5\%$ of its nominal value is suggested.

## ZERO ADJUSTMENT

Zero adjustment must be provided to set the zero transition to the value of $+\frac{1}{2}$LSB. This is achieved by applying an adjustable positive offset to tie the comparator input via P2 and $R_3$. The values shown are suitable for all input ranges greater than $1\frac{1}{2}$ times $V_{REF\ IN}$.

Practical circuits values for +5 and +10V input ranges are given in Fig. 21 which incorporates both zero and gain adjustments.

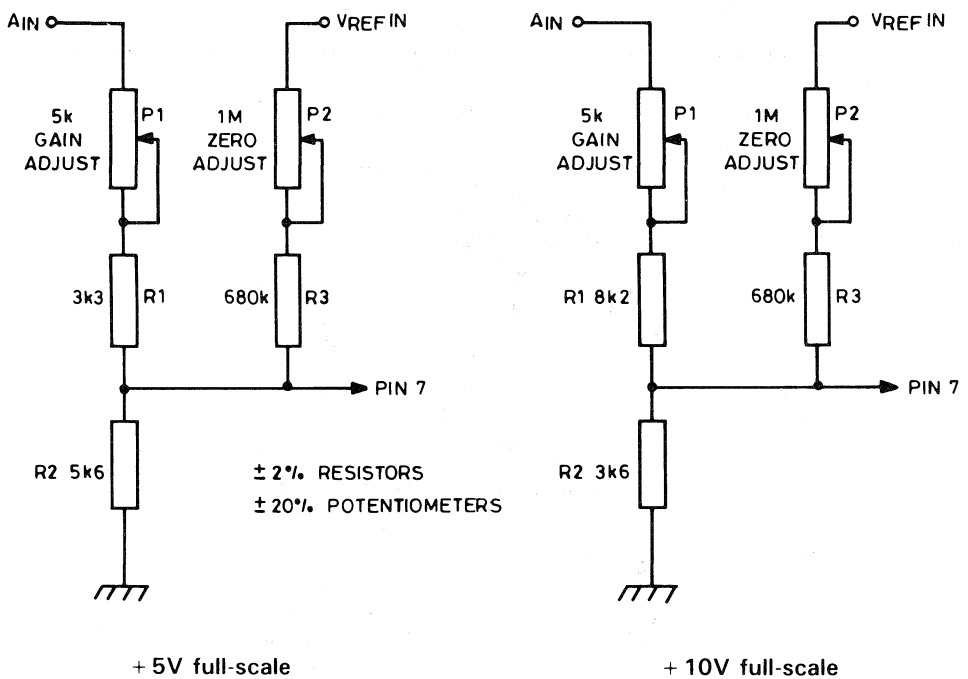



Fig. 21 Unipolar operation component values

## UNIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{WR}$ pulses at intervals long enough to allow a complete conversion or hold $\overline{WR}$ low and monitor the digital outputs.

## OFFSET SETTING

(ii) Apply ½LSB to $A_{IN}$ and adjust zero until DB0 (LSB) just flickers between 0 and 1 with all other bits at 0.

i.e. for transition 00000000 to 00000001.

## GAIN SETTING

(iii) Apply full-scale minus 1.½LSB to $A_{IN}$ and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.

i.e. for transition 11111111 to 11111110.

### UNIPOLAR SETTING-UP POINTS

| Input range, +FS | ½LSB | FS - 1½LSB |
|---|---|---|
| +5V | 9.8mV | 4.9707V |
| +10V | 19.5mV | 9.9414V |

$$1LSB = \frac{FS}{256}$$

### UNIPOLAR LOGIC CODING

| Analogue input ($A_{IN}$) (Nominal code centre value) | Output code (Binary) |
|---|---|
| FS - 1LSB | 11111111 |
| FS - 2LSB | 11111110 |
| ¾FS | 11000000 |
| ½ FS + 1LSB | 10000001 |
| ½FS | 10000000 |
| ½FS - 1LSB | 01111111 |
| ¼FS | 01000000 |
| 1LSB | 00000001 |
| 0 | 00000000 |

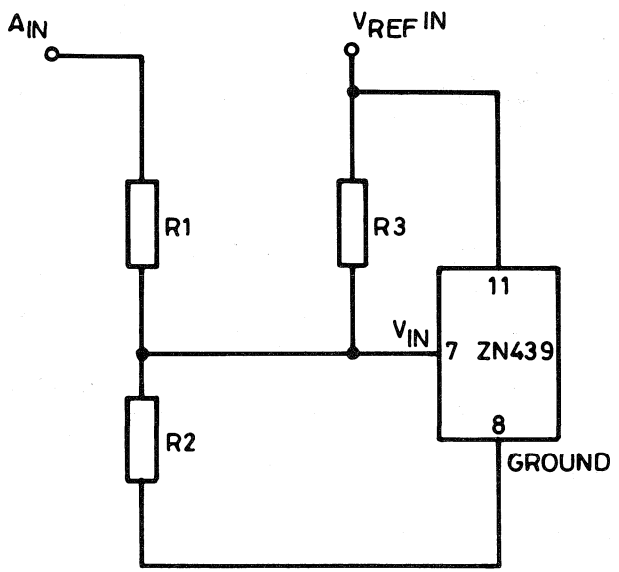



**Fig. 22 Basic bipolar input connection**

## BIPOLAR OPERATION

For bipolar operation the input to the ZN439 is offset by half full-scale by connecting a resistor $R_3$ between $V_{REF\ IN}$ and $V_{IN}$ (Fig. 22).

When $A_{IN} = -FS$, $V_{IN}$ needs to be equal to zero.

When $A_{IN} = +FS$, $V_{IN}$ needs to be equal to $V_{REF\ IN}$.

If the full-scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G - 1)$. $R_2$ and $R_1 = G$. $R_3$ fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ $(= R_{IN}) = 2.7k$.

Thus the nominal values of $R_1$, $R_2$, $R_3$ are given by $R_1 = 5.4Gk$, $R_2 = 5.4G/(G - 1)k$, $R_3 = 5.4k$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) results if $R_1 = R_3 = 5.4k$ and $R_2 = \infty$.

Assuming the $V_{REF\ IN} = 2.5V$ the nominal values of resistors for $\pm 5$ and $\pm 10V$ input ranges are given in the following table.

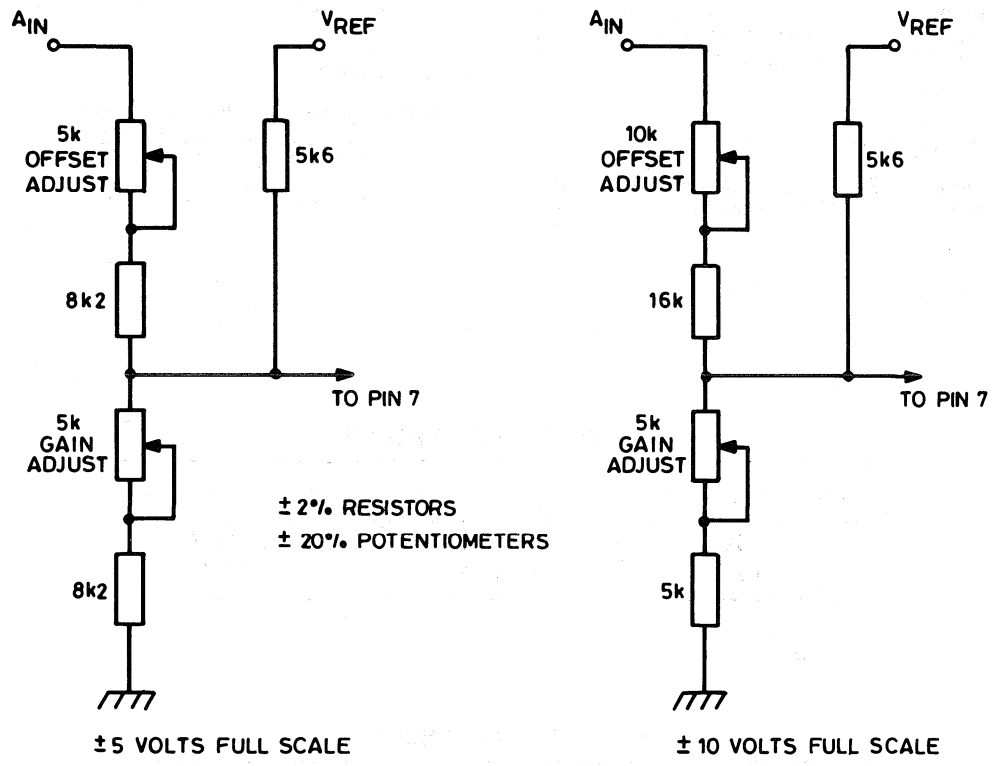



**Fig. 23 Bipolar operation - component values**

| Input range | G | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|---|
| ± 5V | 2 | 10.8k | 10.8k | 5.4k |
| ± 10V | 4 | 21.6k | 7.2k | 5.4k |

Minus full-scale (offset) is set by adjusting $R_1$ about its nominal value relative to $R_3$. Plus full-scale (gain) is set by adjusting $R_2$ relative to $R_1$. Practical circuit realisations are given in Fig. 23.

## BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{WR}$ pulses at intervals long enough to allow a complete conversion or hold $\overline{WR}$ low and monitor the digital outputs.

## OFFSET SETTING

(ii) Apply $-$(FS - ½LSB) to $A_{IN}$ and adjust offset until the DB0 (LSB) output just flickers between 0 and 1 with all other bits at 0.

i.e. for transition 00000000 to 00000001.

## GAIN SETTING

(iii) Apply +(FS - 1½LSB) to $A_{IN}$ and adjust gain until DB0 (LSB) just flickers between 0 and 1 with all other bits at 1.

i.e. for transition 11111111 to 11111110.

### BIPOLAR SETTING-UP POINTS

| Input range, ±FS | −(FS − ½LSB) | +(FS − 1½LSB) |
|---|---|---|
| ±5V | −4.9805V | +4.9414V |
| ±10V | −9.9609V | +9.8828V |

$$1LSB = \frac{2FS}{256}$$

### BIPOLAR LOGIC CODING

| Analogue input ($A_{IN}$) (Nominal code centre value) | Digital output code MSB LSB |
|---|---|
| +(FS - 1LSB) | 11111111 |
| +(FS - 2LSB) | 11111110 |
| +½FS | 11000000 |
| +1LSB | 10000001 |
| 0 | 10000000 |
| −1LSB | 01111111 |
| −½FS | 01000000 |
| −(FS - 1LSB) | 00000001 |
| −FS | 00000000 |

3013-1.0

# ZN447/ZN448/ZN449

## 8-BIT MICROPROCESSOR COMPATIBLE A-D CONVERTERS

The ZN447, ZN448 and ZN449 are 8-bit, successive approximation A-D converters designed for easy interfacing to microprocessors. All active circuitry is contained on-chip including a clock generator and stable 2.5V bandgap reference.

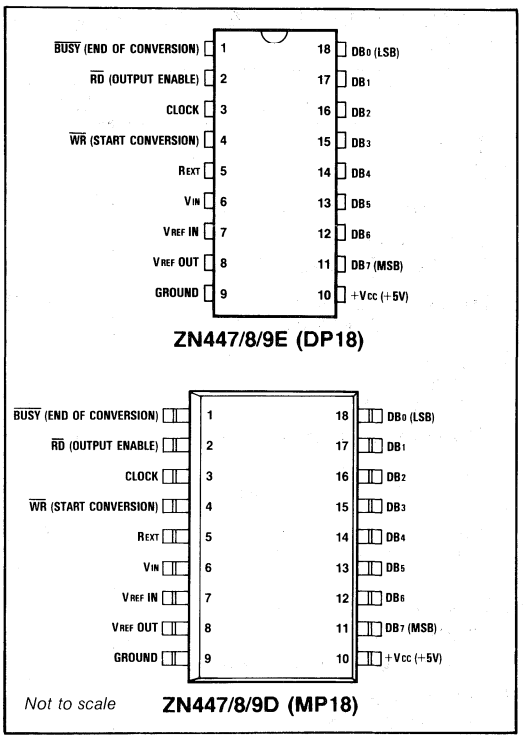
Only a reference resistor and capacitor, clock resistor and capacitor and input resistors are required for operation with either unipolar or bipolar input voltage.

### FEATURES

- Easy Interfacing to Microprocessor, or operates as a 'Stand-Alone' Converter
- Fast: 9 microseconds Conversion time Guaranteed
- Choice of Linearity: 0.3 LSB — ZN447, 0.5 LSB — ZN448, 1 LSB — ZN449
- On-Chip Clock
- Choice of On-Chip or External Reference Voltage
- Unipolar or Bipolar Input Ranges
- Commercial Temperature Range

### ORDERING INFORMATION

| Device type | Linearity error(LSB) | Operating temperature | Package |
|---|---|---|---|
| **ZN447D** | 0.3 | 0°C to +70°C | MP18 |
| **ZN447E** | 0.3 | 0°C to +70°C | DP18 |
| **ZN448D** | 0.5 | 0°C to +70°C | MP18 |
| **ZN448E** | 0.5 | 0°C to +70°C | DP18 |
| **ZN449D** | 1 | 0°C to +70°C | MP18 |
| **ZN449E** | 1 | 0°C to +70°C | DP18 |




Pin connections - top view

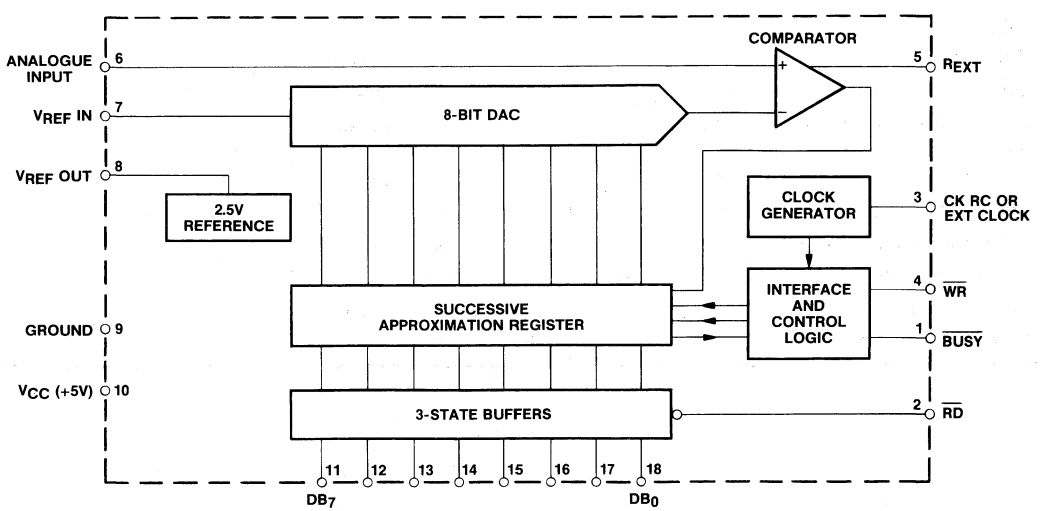



Fig.1 System diagram

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC+}$ | +7V |
| Max. voltage, logic and $V_{REF}$ inputs | $+V_{CC}$ |
| Operating temperature range | 0°C to +70°C (MP and DP packages) |
| Storage temperature range | -55°C to +125°C |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5V, $T_{amb}$ = 25°C, $f_{CLK}$ = 900kHz, unless otherwise specified).

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **ZN447** | | | | | |
| Linearity error | – | – | ±0.3 | LSB | |
| Differential linearity error | – | – | ±0.5 | LSB | |
| Zero transition (00000000→00000001) | 10.5 | 12 | 13.5 | mV | MP package |
| | 13.5 | 15 | 16.5 | mV | DP package |
| Full-scale transition (11111110→11111111) | 2.548 | 2.550 | 2.552 | V | $V_{REF}$ = 2.560V |
| **ZN448** | | | | | |
| Linearity error | – | – | ±0.5 | LSB | |
| Differential linearity error | – | – | ±0.75 | LSB | |
| Zero transition (00000000→00000001) | 9 | 12 | 15 | mV | MP package |
| | 12 | 15 | 18 | mV | DP package |
| Full-scale transition (11111110→11111111) | 2.545 | 2.550 | 2.555 | V | $V_{REF}$ = 2.560V |
| **ZN449** | | | | | |
| Linearity error | – | – | ±1 | LSB | |
| Differential linearity error | – | – | ±1 | LSB | |
| Zero transition (00000000→00000001) | 7 | 12 | 17 | mV | MP package |
| | 10 | 15 | 20 | mV | DP package |
| Full-scale transition (00000000→11111111) | 2.542 | 2.550 | 2.558 | V | $V_{REF}$ = 2.560V |
| **All types** | | | | | |
| Resolution | 8 | – | – | bits | |
| Linearity temperature coefficient | – | ±3 | – | ppm/°C | |
| Differential linearity temperature coefficient | – | ±6 | – | ppm/°C | |
| Full-scale temperature coefficient | – | ±2.5 | – | ppm/°C | |
| Zero temperature coefficient | – | ±8 | – | μV/°C | |
| Reference input range | 1 | – | 3 | V | |
| Supply voltage | 4.5 | 5 | 5.5 | V | |
| Supply current | – | 25 | 40 | mA | |
| Power consumption | – | 125 | 200 | mW | |

**ELECTRICAL CHARACTERISTICS** (Cont.)

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **Comparator** | | | | | |
| Input current | – | 1 | – | μA | $V_{IN} = +3V$, $R_{EXT} = 82k\Omega$ |
| Input resistance | – | 100 | – | kΩ | |
| Tail current | 25 | 65 | 150 | μA | $V- = -5V$ |
| Negative supply | −3 | −5 | −30 | V | |
| Input voltage | −0.5 | – | +3.5 | V | |
| **On-chip reference** | | | | | |
| Output voltage ZN447 | 2.520 | 2.550 | 2.580 | | $R_{REF} = 390\Omega$ |
| ZN448 | 2.520 | 2.550 | 2.580 | V | |
| ZN449 | 2.500 | 2.550 | 2.600 | | $C_{REF} = 4\mu7$ |
| Slope resistance | – | 0.5 | 2 | Ω | |
| $V_{REF}$ temperature coefficient | – | 50 | – | ppm/°C | |
| Reference current | 4 | – | 15 | mA | |
| **Clock** | | | | | |
| On-chip clock frequency | – | – | 1 | MHz | |
| Clock frequency temperature coefficient | – | +0.5 | – | %/°C | |
| Clock resistor | – | – | 2 | kΩ | |
| Maximum external clock frequency | 0.9 | – | 1 | MHz | |
| Clock pulse width | 500 | – | – | ns | |
| High level input voltage $V_{IH}$ | 4 | – | – | V | |
| Low level input voltage $V_{IL}$ | – | – | 0.8 | V | |
| High level input current $I_{IH}$ | – | – | 800 | μA | $V_{IN} = +4V$, $V_{CC} = MAX$ |
| Low level input current $I_{IL}$ | – | – | −500 | μA | $V_{IN} = +0.8V$, $V_{CC} = MAX$ |
| **Logic** (over operating temperature range) | | | | | |
| **Convert input** | | | | | |
| High level input voltage $V_{IH}$ | 2 | – | – | V | |
| Low level input voltage $V_{IL}$ | – | – | 0.8 | V | |
| High level input current $I_{IH}$ | – | 300 | – | μA | $V_{IN} = +2.4V$, $V_{CC} = MAX$ |
| Low level input current $I_{IL}$ | – | ±10 | – | μA | $V_{IN} = +0.4V$, $V_{CC} = MAX$ |
| **$\overline{RD}$ input** | | | | | |
| High level input voltage $V_{IH}$ | 2 | – | – | V | |
| Low level input voltage $V_{IL}$ | – | – | 0.8 | V | |
| High level input current $I_{IH}$ | – | +150 | – | μA | $V_{IN} = +2.4V$, $V_{CC} = MAX$ |
| Low level input current $I_{IL}$ | – | −300 | – | μA | $V_{IN} = +0.4V$, $V_{CC} = MAX$ |

**ELECTRICAL CHARACTERISTICS** (Cont.)

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| High level output voltage $V_{OH}$ | 2.4 | – | – | V | $I_{OH}$ = MAX, $V_{CC}$ = MIN |
| Low level output voltage $V_{OL}$ | – | – | 0.4 | V | $I_{OL}$ = MAX, $V_{CC}$ = MIN |
| High level output current $I_{OH}$ | – | – | −100 | μA | |
| Low level output current $I_{OL}$ | – | – | 1.6 | mA | |
| Three-state disable output leakage | – | – | 2 | μA | $V_{OUT}$ = +2V |
| Input clamp diode voltage | – | – | −1.5 | V | |
| $\overline{RD}$ input to data output | – | 180 | 250 | ns | |
| Enable/disable delay times $T_{E1}$ | 180 | 210 | 260 | ns | |
| $T_{E0}$ | 60 | 80 | 100 | ns | |
| $T_{D1}$ | 80 | 110 | 140 | ns | |
| $T_{D0}$ | 60 | 80 | 100 | ns | |
| Convert pulse width $t_{\overline{WR}}$ | 200 | – | – | ns | |
| $\overline{WR}$ input to $\overline{BUSY}$ output | – | – | 250 | ns | |

## GENERAL CIRCUIT OPERATION

The ZN447 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{WR}$ input the $\overline{BUSY}$ output goes low, the MSB is set to 1 and all other bits are set to 0, which produces an output voltage of $V_{REF/2}$ from the DAC. This is compared to the input voltage $V_{IN}$; a decision is made on the next negative clock edge to reset the MSB to 0 if $\frac{V_{REF}}{2} > V_{IN}$ or leave it set to 1 if $\frac{V_{REF}}{2} < V_{IN}$. Bit 2 is set to 1 on the same clock edge, producing an output from the DAC of $\frac{V_{REF}}{4}$ or $\frac{V_{REF}}{2} + \frac{V_{REF}}{4}$ depending on the state of the MSB. This voltage is compared to $V_{IN}$ and on the next clock edge a decision is made regarding bit 2, whilst bit 3 is set to 1. This procedure is repeated for all eight bits. On the eighth negative clock edge $\overline{BUSY}$ goes high indicating that the conversion is complete.

During a conversion the $\overline{RD}$ input will normally be held high to keep the three-state buffers in their high impedance state. Data can be read out by taking $\overline{RD}$ low, thus enabling the three-state outputs. Readout is non-destructive.

## CONVERSION TIMING

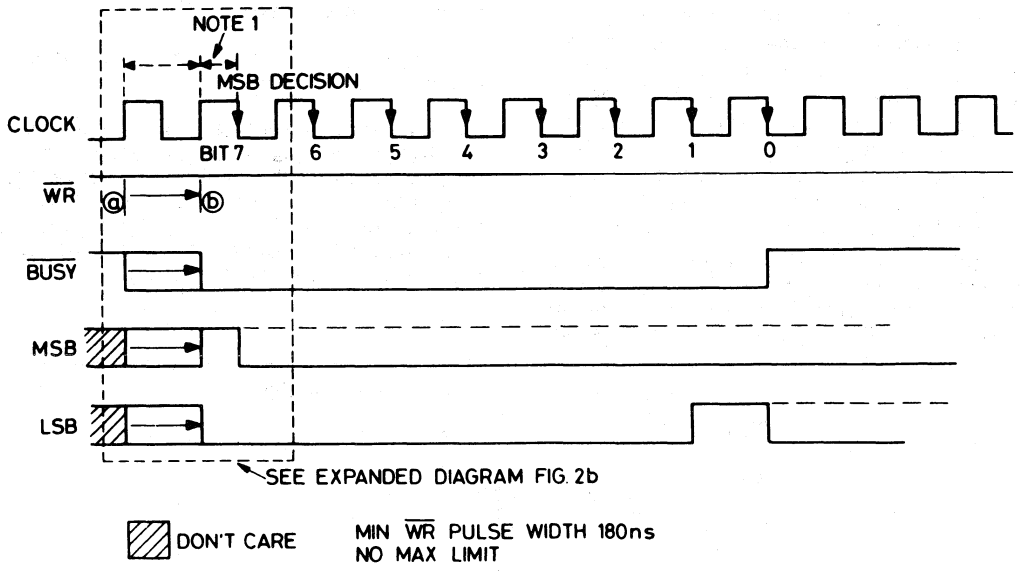
The ZN447 will accept a low-going CONVERT pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 7.5 and 8.5 clock pulses later depending on the relative timing of the clock and CONVERT signals. Timing diagrams for a conversion are shown in Fig. 2.

The converter is cleared by a low-going CONVERT pulse, which sets the most significant bit and resets all the other bits and the $\overline{BUSY}$ flag. Whilst the CONVERT input is low the MSB output of the DAC is continuously compared with the analogue input, but otherwise the converter is inhibited.

After the CONVERT input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The CONVERT pulse can be as short as 200ns; however the MSB must be allowed to settle for at least 550ns before the MSB decision is made. To ensure that this criterion is met even with short CONVERT pulses the converter waits, after the CONVERT input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or 550ns at maximum clock frequency. The CONVERT input is not locked out during a conversion and if it is pulsed low at any time the converter will restart.

The $\overline{BUSY}$ output goes high simultaneously with the LSB decision, at the end of a conversion indicating data valid. Note that if the three-state data outputs are enabled during a conversion the valid data will be available at the outputs after the rising edge of the $\overline{BUSY}$ signal. If, however, the outputs are not enabled until after $\overline{BUSY}$ goes high then the data will be subject to the propagation delay of the three-state buffers. (See under DATA OUTPUTS).




NOTE 1. GUARANTEED PERIOD OF 0.5 CLOCK CYCLE MIN. 1.5 CLOCK CYCLES MAX. ALLOWS MSB TO SETTLE BEFORE MSB DECISION

Fig. 2a

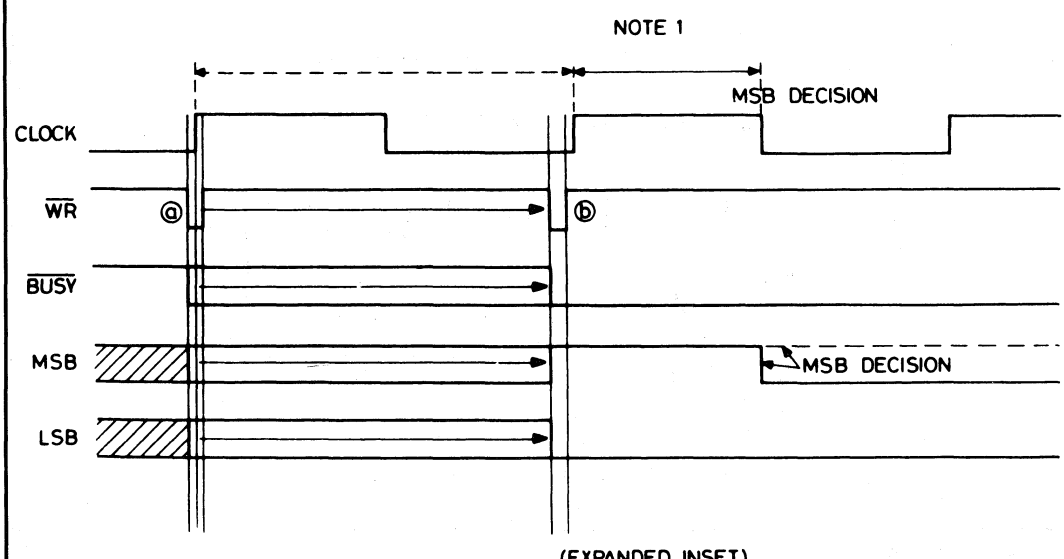



Fig. 2b

Fig. 2 ZN447 timing diagram

If a free-running conversion is required, then the converter can be made to cycle by inverting the $\overline{BUSY}$ output and feeding it to $\overline{WR}$. To ensure that the converter starts reliably after power-up an initial start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive-going pulse which can be derived from a simple RC network that gives a single pulse when power is applied, as shown in Fig. 3a.

The ADC will complete a conversion on every eighth clock pulse, with the $\overline{BUSY}$ output going high for a period determined by the propagation delay of the NOR gate, during which time the data can be stored in a latch. The time available for storing data can be increased by inserting delays into the inverter path.

A timing diagram for the continuous conversion mode is shown in Fig. 3b.

As the $\overline{BUSY}$ output uses a passive pull-up the rise time of this output depends on the RC time constant of the pull-up resistor and load capacitance. In the continuous conversion mode the use of a 4k7 external pull-up resistor is recommended to reduce the risetime and ensure that a logic 1 level is reached.

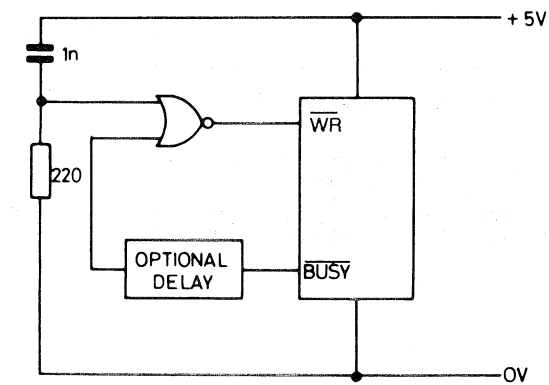



**Fig. 3a Circuit for continuous conversion**

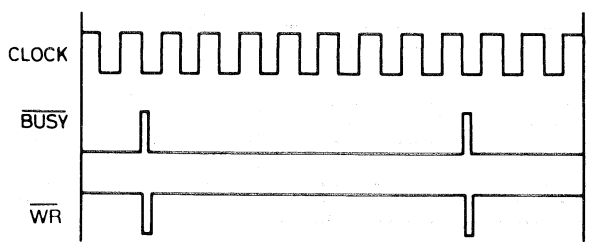



**Fig. 3b Timing for continuous conversion**

## DATA OUTPUTS

The data outputs are provided with three-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig. 4. Whilst the $\overline{RD}$ input is high both output transistors are turned off and the ZN447 presents only a high impedance load to the bus.

When $\overline{RD}$ is low the data outputs will assume the logic states present at the outputs of the successive register.

A test circuit and timing diagram for the output enable/disable delays are given in Fig. 5.

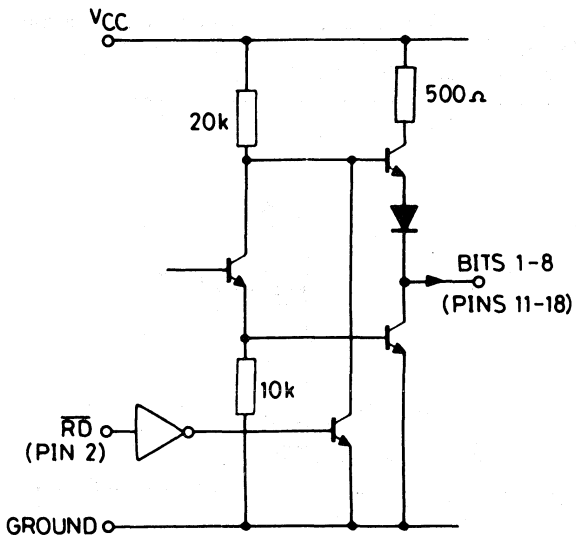



**Fig. 4 Data output**

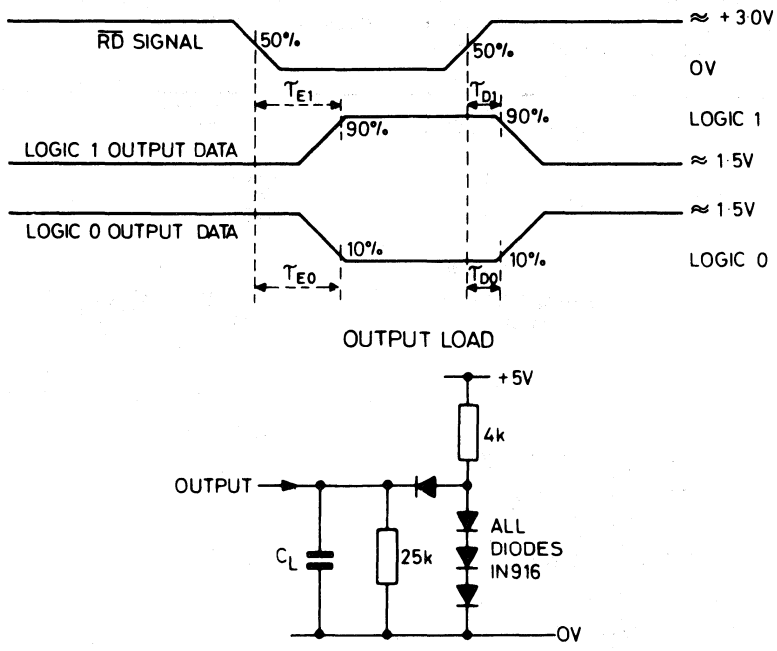



**Fig. 5 Output enable/disable delays**

## $\overline{\text{BUSY}}$ OUTPUT

The $\overline{\text{BUSY}}$ output, shown in Fig. 6, utilises a passive pull-up for CMOS/TTL compatibility. This also allows up to four $\overline{\text{BUSY}}$ outputs to be wire-ANDed together to form a common interrupt line.

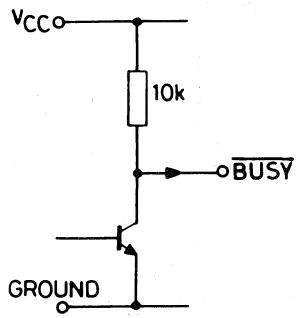



**Fig. 6 $\overline{\text{BUSY}}$ output**

## ON-CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between pin 3 and ground, as shown in Fig. 7a. A graph of typical oscillator frequency versus capacitance is given in Fig. 8. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor, as shown in Fig. 7b. However, due to processing tolerances, the absolute clock frequency may vary considerably between devices. For optimum accuracy and stability of the oscillator frequency, it may be possible to use a crystal or ceramic resonator with suitable load components, as shown in Fig. 7c. The final option is to overdrive the oscillator input with an external clock signal from a TTL or CMOS gate, as shown in Fig. 7d.

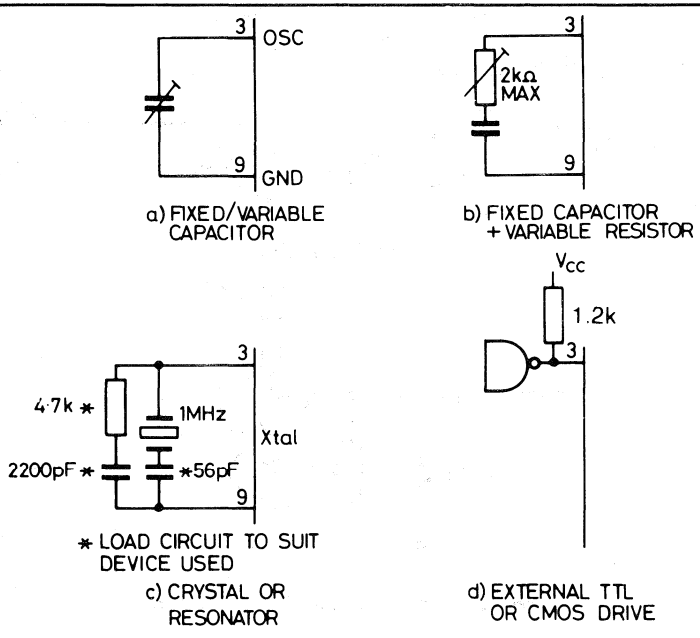



**Fig. 7 Clock circuit external components**

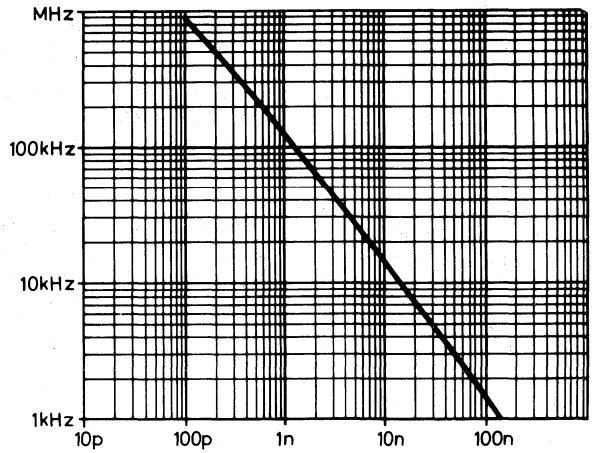



**Fig. 8 Typical clock frequency v $C_{CK}$ ($R_{CK} = 0$)**

## ANALOGUE CIRCUITS

### D-A converter

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 9. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder.

D to A output $= \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the successive approximation register.

$V_{OS}$ is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low ($8\mu V/°C$) the effect on accuracy will be negligible.

The D-A output range can be considered to be $0 - V_{REF\ IN}$ through an output resistance R (4k).

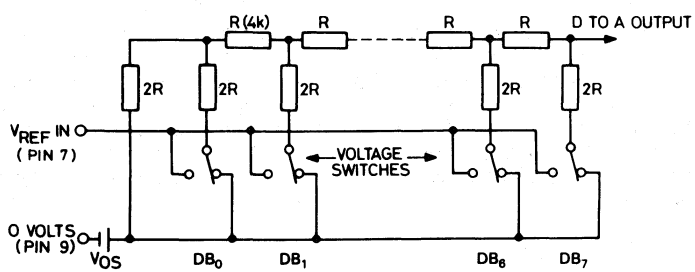



**Fig. 9 R-2R ladder network**

## REFERENCE

### (a) Internal reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 10). A resistor ($R_{REF}$) should be connected between pins 8 and 10.

The recommended value of 390Ω will supply a nominal reference current of $(5-2.5)/0.39 = 6.4$mA. A stabilising/decoupling capacitor, $C_{REF}$ (4μ7), is required between pins 8 and 9. For internal reference operation $V_{REF\ OUT}$ (pin 8) is connected to $V_{REF\ IN}$ (pin 7).

Up to five ZN447's may be driven from one internal reference, there being no need to reduce $R_{REF}$. This useful feature saves power and gives excellent gain tracking between the converters.

Alternatively the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 3mA.

### (b) External reference

If required an external reference voltage in the range +1.5 to +3V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

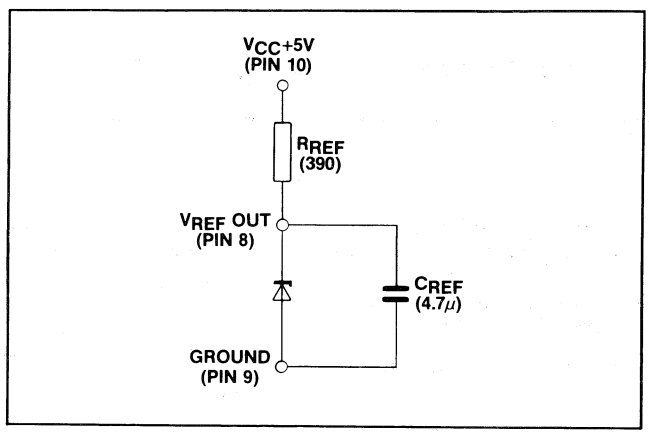



**Fig. 10 Internal voltage reference**

## RATIOMETRIC OPERATION

If the output from a transducer varies with its supply then an external reference for the ZN447 should be derived from the same supply. The external reference can vary from +1.5 to +3V. The ZN447 will operate if $V_{REF\ IN}$ is less than +1.5V but reduced overdrive to the comparator will increase its delay and so the conversion time will need to be increased.

## COMPARATOR

The ZN447 contains a fast comparator, the equivalent input circuit of which is shown in Fig. 11. A negative supply voltage is required to supply the tail current of the comparator. However as this is only 25 to 150μA and need not be well stabilised it can be supplied by a simple diode pump circuit driven from the $\overline{BUSY}$ output.

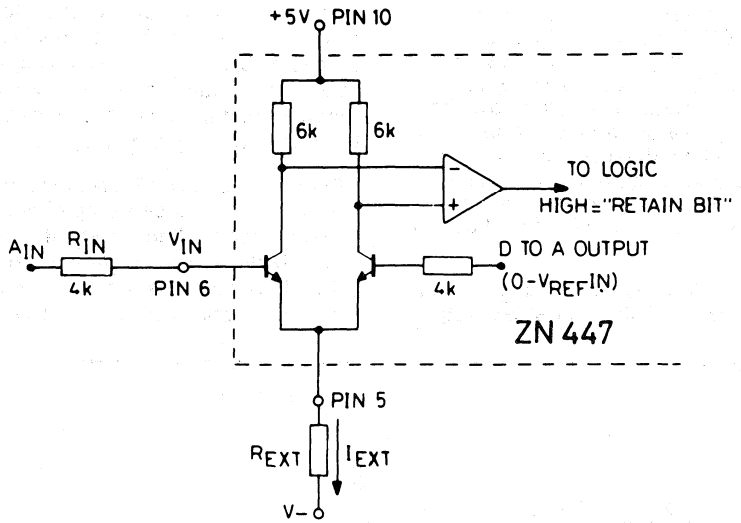



**Fig. 11 Comparator equivalent circuit**

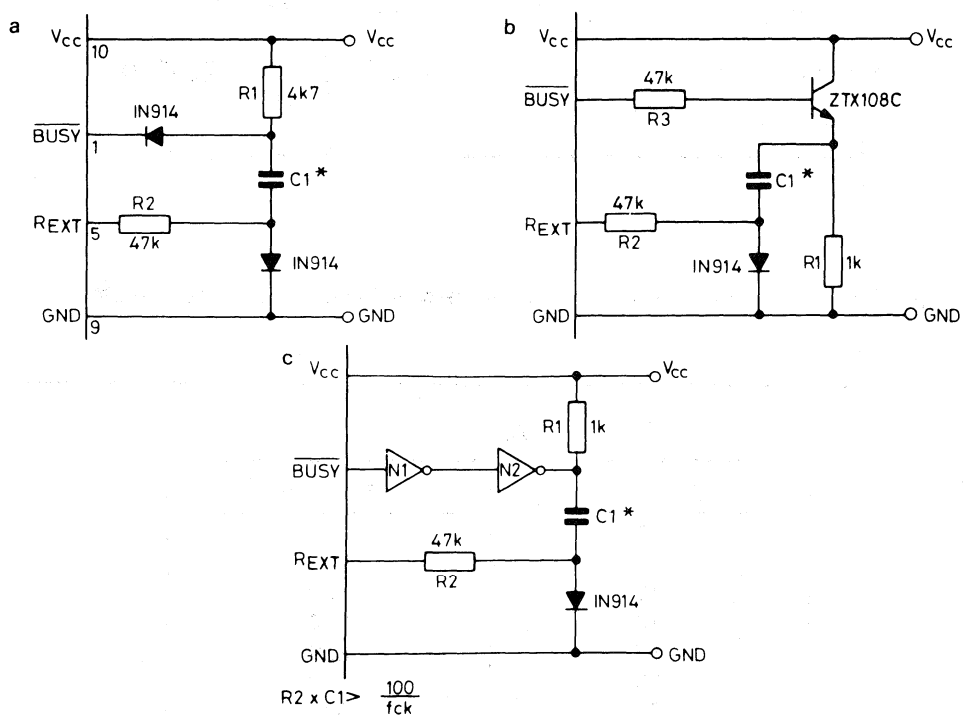



**Fig. 12 Diode pump circuits to supply comparator tail current**

Several suitable circuits are shown in Fig. 12. The principle of operation is the same in each case. Whilst the $\overline{\text{BUSY}}$ output is high, capacitor C1 is charged to about 4-4.5V. During a conversion the $\overline{\text{BUSY}}$ output goes low and the upper end of C1 is thus also pulled low. The lower end of C1 therefore applies about −4V to R2, thus providing the tail current for the comparator. The time constant R2. C1 is chosen according to the clock frequency so that droop of the capacitor voltage is not significant during a conversion.

The constraint on using this type of circuit is that C1 must be recharged whilst the $\overline{\text{BUSY}}$ output is high. If the $\overline{\text{BUSY}}$ output is high for greater than one converter clock period then the circuit of Fig. 12a will suffice. If this is not the case, for example, in the continuous conversion mode, then the circuits of Figs. 12b and 12c are recommended, since these can pump more current into the capacitor.

Where several ZN447's are used in a system the self-oscillating diode pump circuit of Fig. 13 is recommended. Alternatively, if a negative supply is available in the system then this may be utilised. A list of suitable resistor values for different supply voltages is given in table 1.

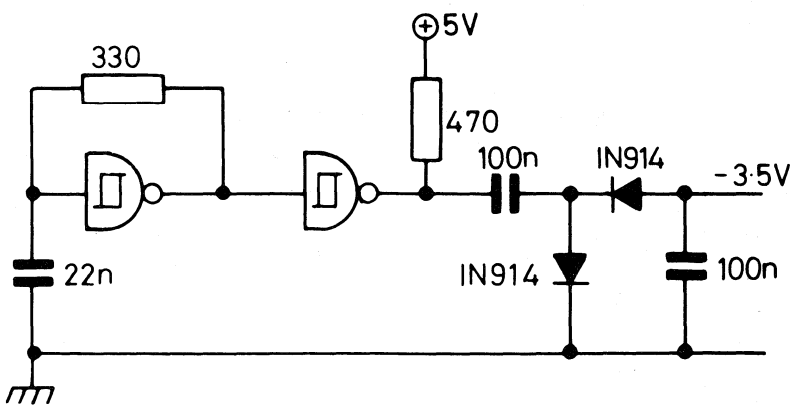



**Fig. 13 Diode pump circuit to supply comparator tail current for up to five ZN447's**

**Table 1**

| V− (volts) | $R_{EXT}$ (kΩ) |
|---|---|
| 3 | 47 |
| 5 | 82 |
| 10 | 150 |
| 12 | 180 |
| 15 | 220 |
| 20 | 330 |
| 25 | 390 |
| 30 | 470 |

## ANALOGUE INPUT RANGES

The basic connection of the ZN447 shown in Fig. 14 has an analogue input range 0 to $V_{REF\,IN}$ which, in some applications, may be made available from previous signal conditioning/ scaling circuits. Input voltage ranges greater than this are accommodated by providing an attenuator on the comparator input, whilst for smaller input ranges the signal must be amplified to a suitable level.

Bipolar input ranges are accommodated by off-setting the analogue input range so that the comparator always sees a positive input voltage.

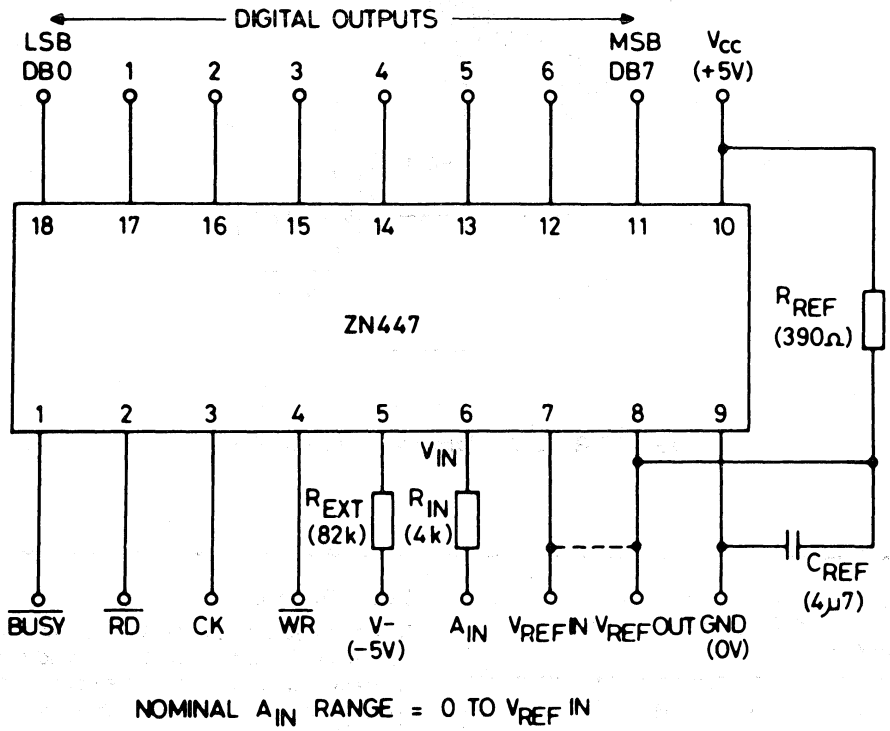



Fig. 14 External components for basic operation

## UNIPOLAR OPERATION

The general connection for unipolar operation is shown in Fig. 15.

The values of $R_1$ and $R_2$ are chosen so that $V_{IN} = V_{REF\ IN}$ when the Analogue Input ($A_{IN}$) is at full-scale.

The resulting full-scale range is given by $A_{IN}\ FS = (1 + \frac{R1}{R2})$, $V_{REF\ IN} = G.V_{REF\ IN}$.

To match the ladder resistance R1/R2 ($R_{IN}$) = 4k.

The required nominal values of $R_1$ and $R_2$ are given by $R_1 = 4G$ k, $R_2 = \frac{4G}{G-1}$ k

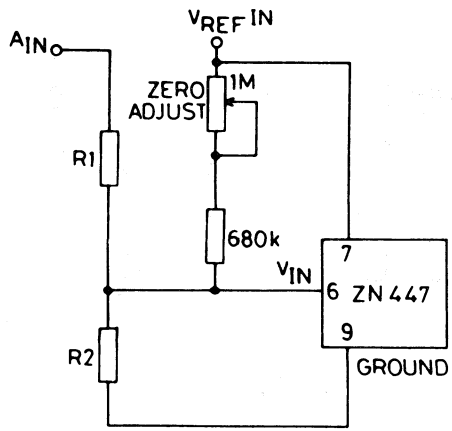



**Fig. 15 General unipolar input connections**

Using these relationships a table of nominal values of $R_1$ and $R_2$ can be constructed for $V_{REF\ IN} = 2.5V$.

| Input range | G | $R_1$ | $R_2$ |
|---|---|---|---|
| +5V | 2 | 8k | 8k |
| +10V | 4 | 16k | 5.33k |

### Gain adjustment

Due to tolerances in $R_1$ and $R_2$, tolerances in $V_{REF}$ and the gain (full-scale) error of the DAC, some adjustment should be incorporated into $R_1$ to calibrate the full-scale of the converter. When used with the internal reference and 2% resistors a preset capable of adjusting $R_1$ by at least ±5% of its nominal value is suggested.

### Zero adjustment

Due to offsets in the DAC and comparator the zero (0 to 1) code transition would occur with typically 15mV applied to the comparator input, which corresponds to 1.5LSB with a 2.56V reference.

Zero adjustment must therefore be provided to set the zero transition to its correct value of +0.5LSB or 5mV with a 2.56V reference. This is achieved by applying an adjustable positive offset to the comparator input via P2 and R3. The values shown are suitable for all input ranges greater than 1.5 times $V_{REF\ IN}$.

Practical circuit values for +5 and +10V input ranges are given in Fig. 16, which incorporates both zero and gain adjustments.

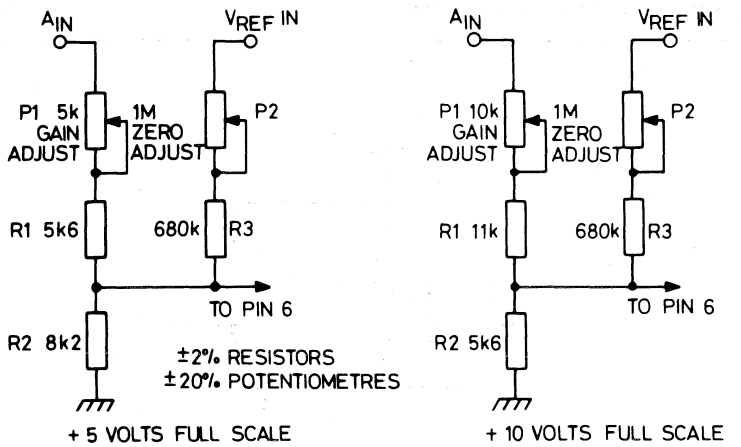



**Fig. 16 Unipolar component values**

**Unipolar adjustment procedure**

(i) Apply continuous convert pulses at intervals long enough to allow complete conversion and monitor the digital outputs.

(ii) Apply full-scale minus 1.5LSB to $A_{IN}$ and adjust gain until bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 1.

(iii) Apply 0.5LSB to $A_{IN}$ and adjust zero until bit 8 just flickers between 0 and 1 with all other bits at 0.

**Unipolar setting up points**

| Input range, +FS | 0.5LSB | FS - 1.5LSB |
|---|---|---|
| +5V | 9.8mV | 4.9707V |
| +10V | 19.5mV | 9.9414V |

$$1LSB = \frac{FS}{256}$$

**Unipolar logic coding**

| Analogue input ($A_{IN}$) (Nominal code centre value) | Output code (Binary) |
|---|---|
| FS - 1LSB | 11111111 |
| FS - 2LSB | 11111110 |
| 0.75FS | 11000000 |
| 0.5FS + 1LSB | 10000001 |
| 0.5FS | 10000000 |
| 0.5FS - 1LSB | 01111111 |
| 0.25FS | 01000000 |
| 1LSB | 00000001 |
| 0 | 00000000 |

## BIPOLAR OPERATION

For bipolar operation the input to the ZN447 is offset by half full-scale by connecting a resistor $R_3$ between $V_{REF\ IN}$ and $V_{IN}$ (Fig. 17).

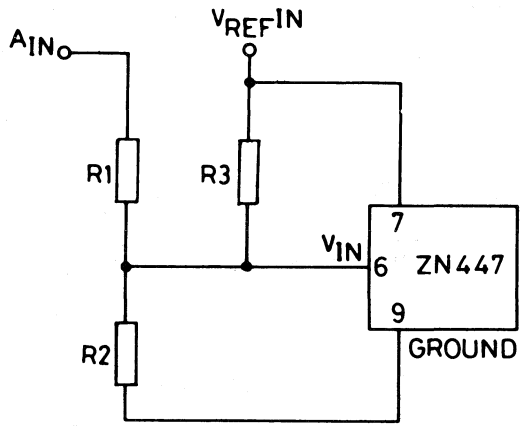



**Fig. 17 Basic bipolar input connection**

When $A_{IN} = -FS$, $V_{IN}$ needs to be equal to zero.

When $A_{IN} = +FS$, $V_{IN}$ needs to be equal to $V_{REF\ IN}$.

If full-scale range is $\pm G$. $V_{REF\ IN}$ then $R_1 = (G - 1)$. $R_2$ and $R_1 = G$. $R_3$ fulfil the required conditions.

To match the ladder resistance, $R_1/R_2/R_3$ $(= R_{IN}) = 4k$.

Thus the nominal values of $R_1$, $R_2$, $R_3$ are given by $R_1 = 8\ Gk$, $R_2 = 8G/(G - 1)k$, $R_3 = 8k$.

A bipolar range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $+V_{REF\ IN}$) results if $R_1 = R_3 = 8k$ and $R_2 = \infty$.

Assuming that $V_{REF\ IN} = 2.5V$ the nominal values of resistors for $\pm 5$ and $\pm 10V$ input ranges are given in the following table.

| Input range | G | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|---|
| $\pm 5V$ | 2 | 16k | 16k | 8k |
| $\pm 10V$ | 4 | 32k | 10.66k | 8k |

Minus full-scale (offset) is set by adjusting $R_1$ about its nominal value relative to $R_3$. Plus full-scale (gain) is set by adjusting $R_2$ relative to $R_1$.

Practical circuit realisations are given in Fig. 18.

Note that in the $\pm 5V$ case $R_3$ has been chosen as 7.5k (instead of 8.2k) to obtain a more symmetrical range of adjustment using standard potentiometers.

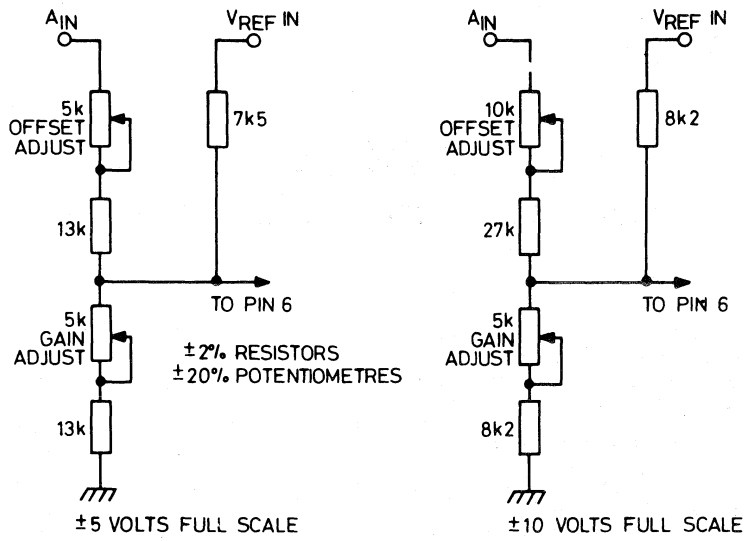



**Fig. 18 Bipolar operation - component values**

**Bipolar adjustment prodedure**

(i) Apply continuous SC pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

(ii) Apply −(FS - 0.5LSB) to $A_{IN}$ and adjust offset until the bit 8 (LSB) output just flickers between 0 and 1 with all other bits at 0.

(iii) Apply +(FS - 1.5LSB) to $A_{IN}$ and adjust gain until bit 8 just flickers between 0 and 1 with all other bits at 1.

(iv) Repeat step (ii).

**Bipolar setting up points**

| Input range, ±FS | −(FS −0.5LSB) | +(FS −1.5LSB) |
|---|---|---|
| ±5V | −4.9805V | +4.9414V |
| ±10V | −9.9609V | +9.8828V |

$$1LSB = \frac{2FS}{256}$$

**Bipolar logic coding**

| Analogue input ($A_{IN}$) (Nominal code centre value) | Output code (Offset binary) |
|---|---|
| +(FS - 1LSB) | 11111111 |
| +(FS - 2LSB) | 11111110 |
| +0.5FS | 11000000 |
| +1LSB | 10000001 |
| 0 | 10000000 |
| −1LSB | 01111111 |
| −0.5FS | 01000000 |
| −(FS - 1LSB) | 00000001 |
| −FS | 00000000 |

# ZN454E

## TRIPLE 4-BIT VIDEO D-A CONVERTER

The ZN454 consists of three 4-bit D-A converters, providing a colour palette of 4096 possible display colours. The required logic translators, control logic, a reference voltage source and reference amplifier are also integrated on-chip.

Each D-A converter accepts 4-bit digital video data and SYNC/BLANK signals directly from a TTL source and produces a composite video output to directly drive a 75Ω line terminated by a 75Ω load at both ends.

The ZN454 is ideally suited for pixel colour generation in graphics display systems requiring 4-bit colour resolution. The high linearity of each DAC ensures excellent colour contrast and the fast update rate allows the device to be interfaced to monitors with a resolution of up to 1024 x 1280 pixels assuming a standard refresh rate of 60Hz.

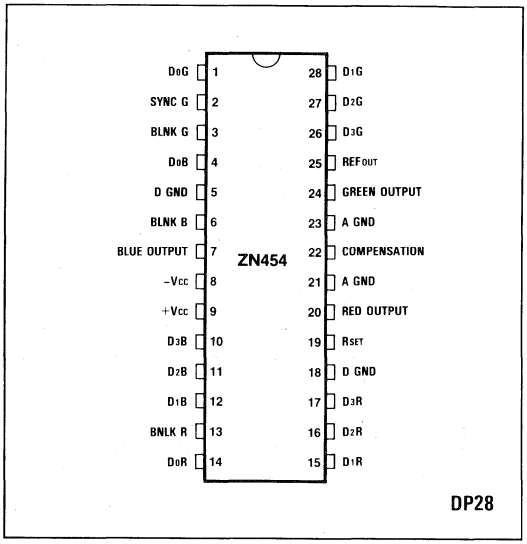



*Fig.1 Pin connections - top view*

### FEATURES

- 3 Video DAC's - Ideal for Colour Graphics
- Fast, 8ns Settling Time
- Update Rates to 100MHz
- Low Glitch Energy
- ¼ LSB Linearity Error
- On-Chip Reference Source
- Composite Sync and Blank Inputs
- TTL Compatible Inputs
- Generates Standard Video Signal Output Across a Doubly Terminated 75 Ohm Load
- 28 Pin DIL Package

### GENERAL CIRCUIT DESCRIPTION

Each D-A converter of the ZN454 uses high speed switches to steer current from precision current sources to either analog ground or to the analog output - as governed by the digital inputs (see Fig.4). The analog output voltage is now obtained from these weighted current sources producing the desired voltage drop across the 37.5Ω load impedance. The gain of the D-A converters is adjustable via RSET.

Since the ZN454 utilises current output DAC's the output impedance is inherently high. Thus a 75Ω resistance is required (adjacent to each DAC output) to shunt this high impedance and provide the correct impedance for driving a 75Ω line terminated in 75Ω at the monitor. The desired 1V p-p composite signal will now be developed across this effective 37.5Ω output impedance.

The grey scale output current of each DAC has 16 levels from 0 to -17mA nominally (see Fig.3). This develops 16 levels of output voltage from 0 to -643mV across the specified 37.5Ω load impedance. the 'REFERENCE WHITE' level (0V) corresponds to the digital input code 1111 and the 'REFERENCE BLACK' (-643mV) to 0000.

A logic '1' on the BLANK input overrides the data inputs and drives the output to 71mV more negative than the 'REFERENCE BLACK' level. This corresponds to the 'BLANKING' (or 'blacker-than-black') level.

Activating the SYNC input (logic '1') with the BLANK input 'high' drives the output to 286mV more negative than the 'BLANKING' level. This voltage (nominally -1V) corresponds to the 'SYNC' level.

### GAIN ADJUSTMENT (RSET)

RSET provides a means of adjusting the current in the weighted current sources. An amplifier compares the voltage developed across RSET, with the reference voltage. If RSET is increased/decreased the amplifier output causes the current through RSET to decrease/increase (to bring the voltage across RSET back in line with the reference voltage). This also causes the current in each of the current sources to decrease/increase (see Fig.3). In this manner the magnitude of the output waveform can be varied to obtain the desired levels.

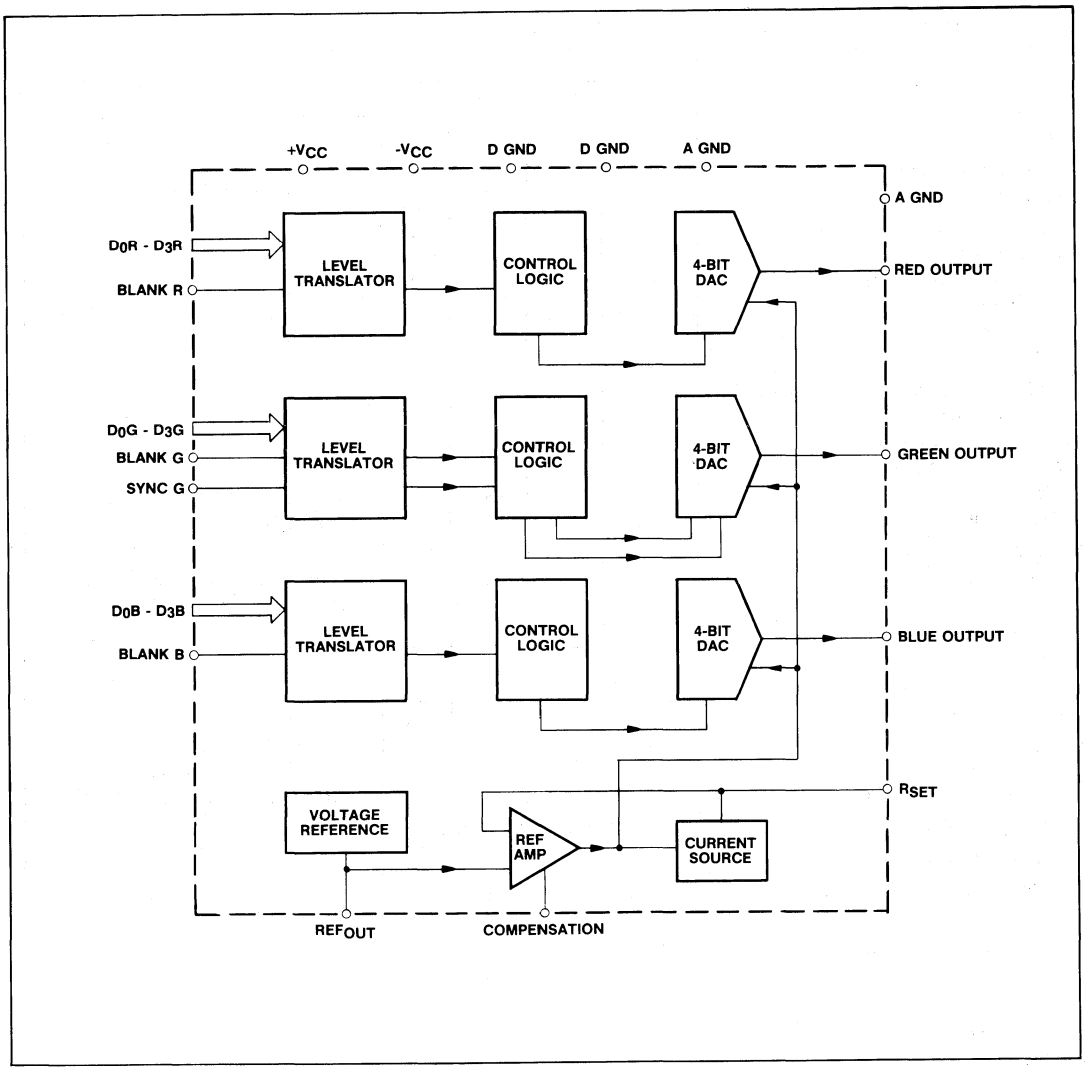



*Fig.2 Block diagram*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, +Vcc | +6V |
| Supply voltage, -Vcc | -6V |
| Logic input voltage | +Vcc |
| Operating temperature range | 0°C to 70°C |
| Storage temperature range | -55°C to +125°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 25°C, $V_{CC}$ = ±5V, $R_L$ = 37.5Ω and $R_{SET}$ = 180Ω

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Resolution | | 4 | | | Bits | |
| LSB weight (current) | | | 1.13 | | mA | Note 1 |
| LSB weight (voltage) | | | 43 | | mV | |
| **Accuracy** | | | | | | |
| Linearity error | | | ±0.25 | ±0.5 | LSB | |
| Differential linearity error | | | | ±0.5 | LBS | Note 2 |
| Offset error | | | -5.0 | -15.0 | mV | |
| Gain error | | | | ±5 | % of nom.FSR | |
| **Speed performance - Grey scale output** | | | | | | |
| Rise/fall times (voltage) | | | 3 | | ns | 10-90% of final value |
| Settling time (voltage) | | | 8 | | ns | Note 3 |
| Maximum update rate | | | 100 | | MHz | Note 4 |
| Slew rate | | | 180 | | V/μs | 10-90% of final value |
| Glitch energy | | | 60 | | pV-s | Note 5 |
| **Temperature coefficient** | | | | | | |
| Offset | | | 10 | | ppm/°C | Measured with |
| Gain | | | 500 | | ppm/°C | internal reference |
| **Data, sync and blank inputs** | | | | | | |
| Logic compatibility | | | **TTL** | | | |
| High level input voltage | $V_{IH}$ | 2.0 | | | V | |
| Low level input voltage | $V_{IL}$ | | | 0.8 | V | |
| High level input current | $I_{IH(1)}$ | | | +20 | μA | $V_{CC}$ = max, $V_{in}$ = 5.5V |
| | $I_{IH(2)}$ | | | ±10 | μA | $V_{CC}$ = max, $V_{in}$ = 2.4V |
| Low level input current | $I_{IL}$ | | | -1.6 | mA | $V_{CC}$ = max, $V_{in}$ = 0.4V |
| Coding (see Fig.2) | | | **Complementary binary** | | | |
| **Output - Grey scale** | | | | | | |
| Voltage range | | | 0.64 | | V | Note 1 |
| Current range | | | 17 | | mA | |
| **Output - Composite sync** | | | | | | |
| Voltage range | | | 286 | | mV | |
| Current range | | | 7.6 | | mA | |
| **Output - Composite blanking** | | | | | | |
| Voltage range | | | 71 | | mV | |
| Current range | | | 1.9 | | mA | |
| **Output voltage compliance** | | 0 | | 1.5 | V | |
| **Internal voltage reference** | | | | | | |
| Output voltage | $V_{REF}$ | | -1.26 | | V | |
| Output voltage tolerance | | | | ±5.0 | % | |
| Output voltage TC | | | 200 | | ppm/°C | 0°C to 70°C |
| **Power supply requirements** | | | | | | |
| Supply voltage | $+V_{CC}$ | 4.5 | 5.0 | 5.5 | V | |
| | $-V_{CC}$ | -4.5 | -5.0 | -5.5 | V | |
| Supply current | $+I_{CC}$ | | 22.5 | | mA | |
| | $-I_{CC}$ | | 136.0 | | mA | |

NOTES
1. LSB and full-scale output levels adjustable with $R_{SET}$. 2. Monotonicity guaranteed over full operating temperature range.
3. The settling time was measured as the time between the start of the output rising/falling edge to where the output entered and remained within ±½ LSB of the final value. The value quoted is for a transition from reference white to reference black and vice versa, and does not include the inherent input propagation delay (2-3ns). See section describing settling time measurement.
4. The maximum update rate is limited by the full-scale settling time to rated accuracy.
5. Measurement of glitch energy is discussed in a later section of this data sheet.

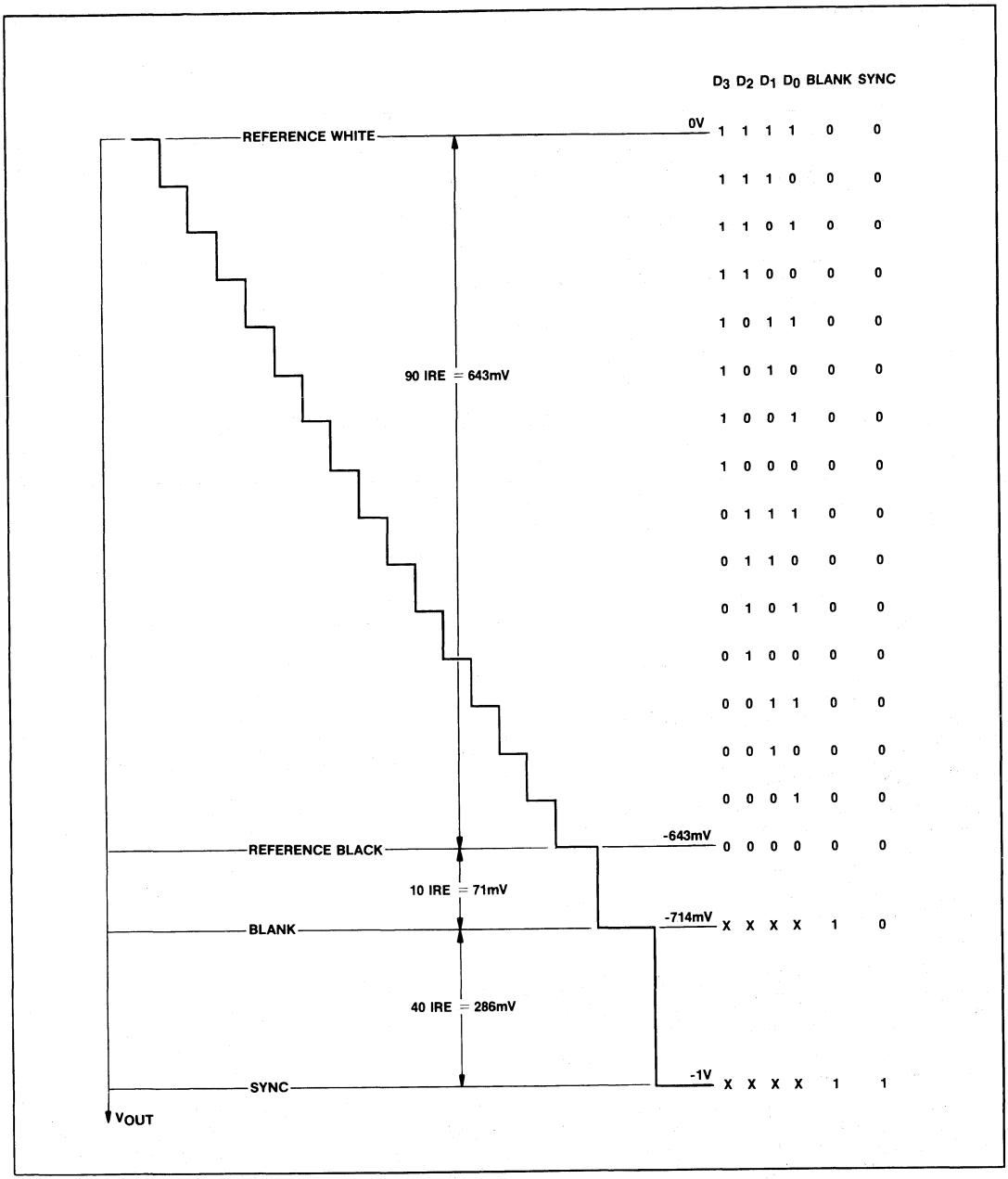



*Fig.3 Typical composite video output waveform*

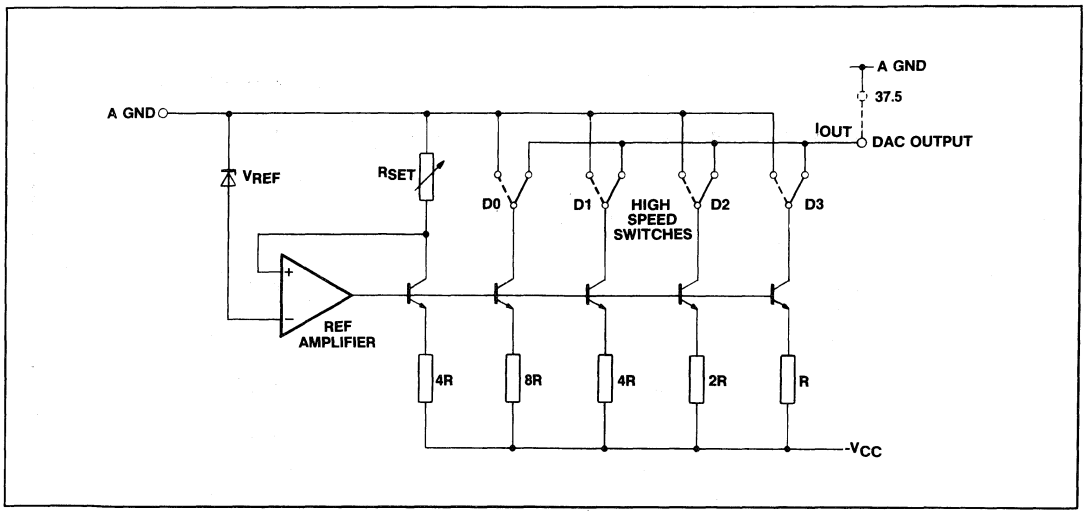



*Fig.4 Current source array (schematic)*

## DIGITAL INPUTS

The digital inputs are high speed level translators (see Fig.5).

The ZN454 requires very few external components for normal operation. Fig.6 illustrates the external component connections.

## LAYOUT CONSIDERATIONS

When using the ZN454, as with any other device of this kind, certain precautions must be taken to obtain the best performance.

Some of the requirements are:

1. A ground plane board providing a good earth and with good power supply connections, to keep noise to a minimum.

2. Good decoupling - especially around all the fast switching circuits - including a 0.1$\mu$F capacitor from both the +5V and -5V supplies positioned close to the ZN454. The ground connections for these capacitors should be adjacent.

3. Some physical separation between the digital input tracks to minimise crosstalk.

4. Matched digital input signal paths to avoid introducing any unnecessary time skew between the inputs. This would cause glitches on the DAC outputs with changing codes. Also the outputs from the driving device will have to be well matched for the same reason.

5. 75Ω resistors close to the DAC outputs, to provide the correct impedance for driving 75Ω lines.

## SETTLING TIME AND GLITCH ENERGY MEASUREMENT

In a finished design the ZN454 would be soldered directly into the board to obtain the best performance possible. However for evaluation purposes a socket really needs to be used. This will give some degradation in performance but useful results can still be obtained.

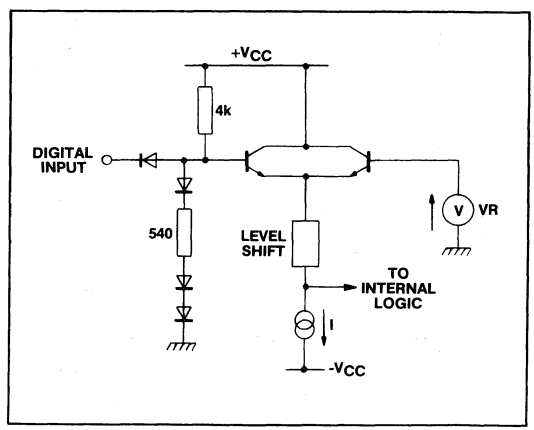



*Fig.5 Equivalent circuit of sync, blank and data inputs*

Measurement of settling time and glitch energy is not a straightforward task and all of the recommendations previously noted must be adhered to. If these parameters are to be measured using an oscilloscope, great care must be taken to avoid corrupting the analog outputs e.g. conventional probes cannot simply be clipped onto the outputs as this would cause reflections giving rise to errors. Instead the ZN454 needs a 75Ω termination near the chip, a 75Ω cable - also grounded close to the chip - connecting to a 75Ω lead through termination at the oscilloscope. Optimum cable length is about 6 inches but it may need trimming around this. Also the oscilloscope obviously needs to have sufficient bandwidth to cope with the rise and fall times encountered.

The digital circuits driving the DAC's must not introduce too much noise, or time skew between the bit inputs. This

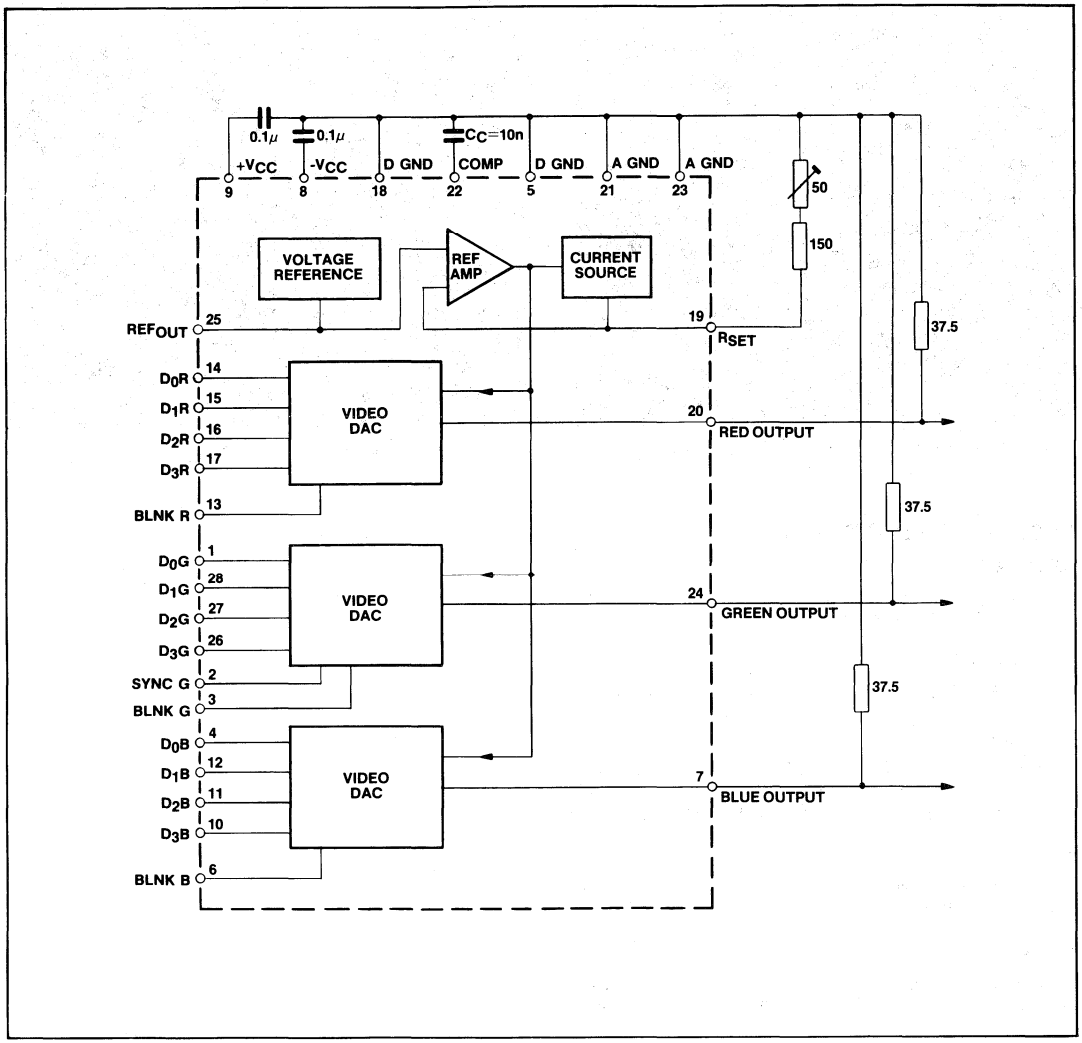



*Fig.6 External component connections*

can considerably affect the results. However, a convenient way of minimising these problems for evaluation purposes, is to drive the digital inputs directly from a pulse generator. Full-scale transitions of the grey scale can now be monitored by wiring the inputs to a given DAC in parallel (terminating in 50Ω) and clocking with the pulse generator. Each output can now be examined in turn. The circuit diagram is as in Fig.6 except that the sync and blank inputs will be tied low. The 37.5Ω terminations on the DAC output, and the digital input signals are provided as described above. Fig.7 shows an actual full-scale (grey scale) output transition measured using the above procedure, giving a settling time of 5.12ns.

Glitch energy measurements, at the major transition for example, can also be measured by driving the digital inputs directly from a pulse generator but it will need to have well matched complementary outputs. Also the lead lengths from the generator to the digital inputs will have to be well matched (and terminated in 50Ω). This is so because this measurement is especially critical of any time skew between the input signals. Indeed even an ideal DAC would produce glitches if there were timing differences between these changing input signals. These time skew errors which would manifest themselves as exaggerated glitches on the DAC output, are referred to the point at which the input signals cross the digital input thresholds (≏1.5V nom.). Thus the characteristics of the driving signals will have some effect on the amplitude of the glitches, which may be minimised by careful design. The circuit arrangement for measuring the glitch energy is as above but with the digital inputs being switched through different codes. Fig.8 shows an actual mid-scale glitch, measured using the above procedure.

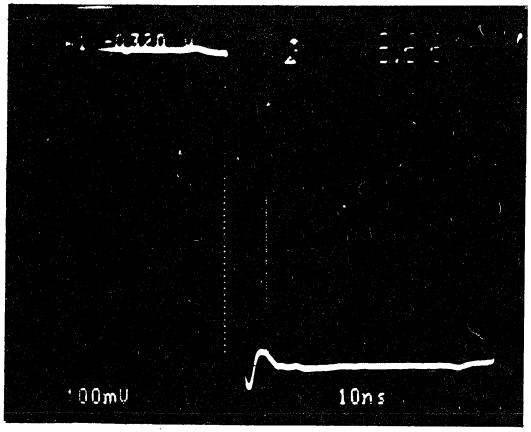



*Fig.7 Full-scale output transition - settling time*

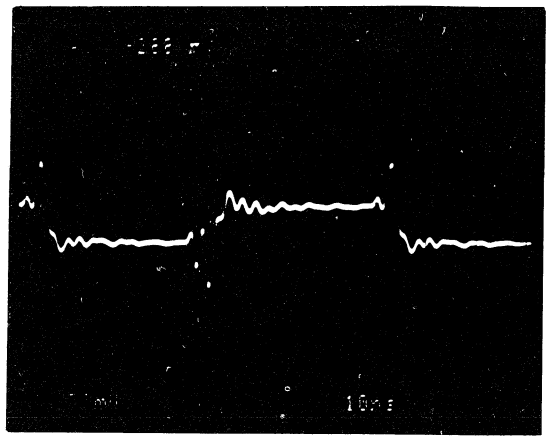


*Fig.8 Mid-scale output glitch*

## GLOSSARY OF VIDEO TERMS

### Raster scan

The method of sweeping a CRT one line at a time to generate and display images.

### Composite video signal

The VIDEO signal plus the BLANK and SYNC signals.

### Video signal

The portion of the composite VIDEO SIGNAL which varies in grey scale levels between 'reference white' and 'reference black' - this is the portion which is visually observed.

### Sync signal

The portion of the video waveform that synchronises the raster scanning process.

### Grey scale

The discrete levels between and including 'reference white' and 'reference black' - there are 16 levels for a 4-bit DAC.

### Blanking level

The level separating the SYNC portion from the VIDEO portion. Usually referred to as the FRONT PORCH or BACK PORCH, this is the level which will shut off the electron guns resulting in the blackest possible display.

### Sync level

The negative peak level of the sync signal.

### Reference black level

The maximum negative level of the VIDEO signal.

### Reference white level

The maximum positive level of the VIDEO signal.

# ZN455

## 100MHz TRIPLE 4-BIT RAM DAC

The ZN455 consists of three 4-bit video D to A converters, each with a 16x4 palette RAM allowing the simultaneous display of 16 colours from a palette of 4096. Writing data to the device during blanking or synchronisation does not affect the outputs, which allows the RAM to be reprogrammed during the retrace period to give more than 16 colours on-screen at one time. To ease the system timing requirements and allow a higher pixel rate, a two level internal pipeline has been incorporated.

The ZN455 offers a versatile microprocessor and video controller interface, and each output will drive a doubly terminated 75Ω transmission line. The incorporation of a bandgap reference source, composite video controls and pipeline latches makes this device the ideal choice for high performance bit-mapped colour graphics systems.

### FEATURES

- 100 MHz Pipeline Operation
- Triple 4-Bit Digital to Analog Converters
- On-Chip Palette
- On-Chip Bandgap Voltage Reference
- TTL / ECL10K Inputs
- Fast Settling Time
- Low Glitch Error
- $\frac{1}{4}$ LSB Linearity Error Max
- Composite Sync and Blank
- Generates Standard (RS330, RS343) Video across a Doubly Terminated 75Ω Load
- Choice of 28-Pin DIL or PLCC Package

### APPLICATIONS

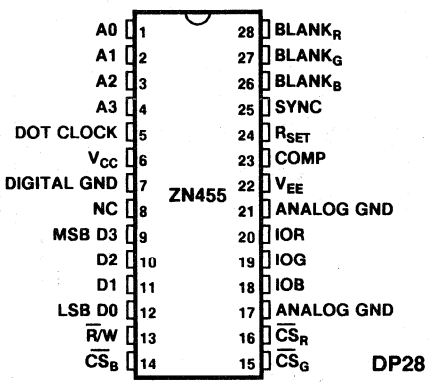
- Personal Computer Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Instrumentation

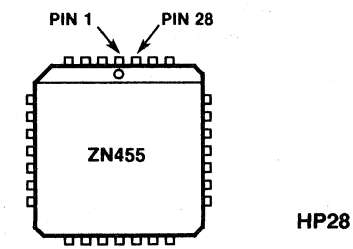
### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Operating temperature | 0°C to +70°C |
| Storage temperature | −55°C to +125°C |
| TTL input voltage range | 0V to $V_{CC}$ |
| ECL Input voltage range | $V_{EE}$ to 0V |
| $V_{CC}$ | +6V |
| $V_{EE}$ | −6V |

### ORDERING INFORMATION

**ZN455E** (Commercial - Plastic DIL Package)
**ZN455Q** (Commercial - PLCC Package)




**HP28 PINOUT**

| Pin | Description | Pin | Description |
|---|---|---|---|
| 1 | A0 | 15 | $\overline{CS}_G$ |
| 2 | A1 | 16 | $\overline{CS}_R$ |
| 3 | A2 | 17 | ANALOG GND |
| 4 | A3 | 18 | IOB |
| 5 | DOT CLOCK | 19 | IOG |
| 6 | $V_{CC}$ | 20 | IOR |
| 7 | DIGITAL GND | 21 | ANALOG GND |
| 8 | NC | 22 | $V_{EE}$ |
| 9 | MSB D3 | 23 | COMP |
| 10 | D2 | 24 | $R_{SET}$ |
| 11 | D1 | 25 | SYNC |
| 12 | LSB D0 | 26 | $BLANK_B$ |
| 13 | R/W | 27 | $BLANK_G$ |
| 14 | $\overline{CS}_B$ | 28 | $BLANK_R$ |

*Fig.1 Pin connections - top view*

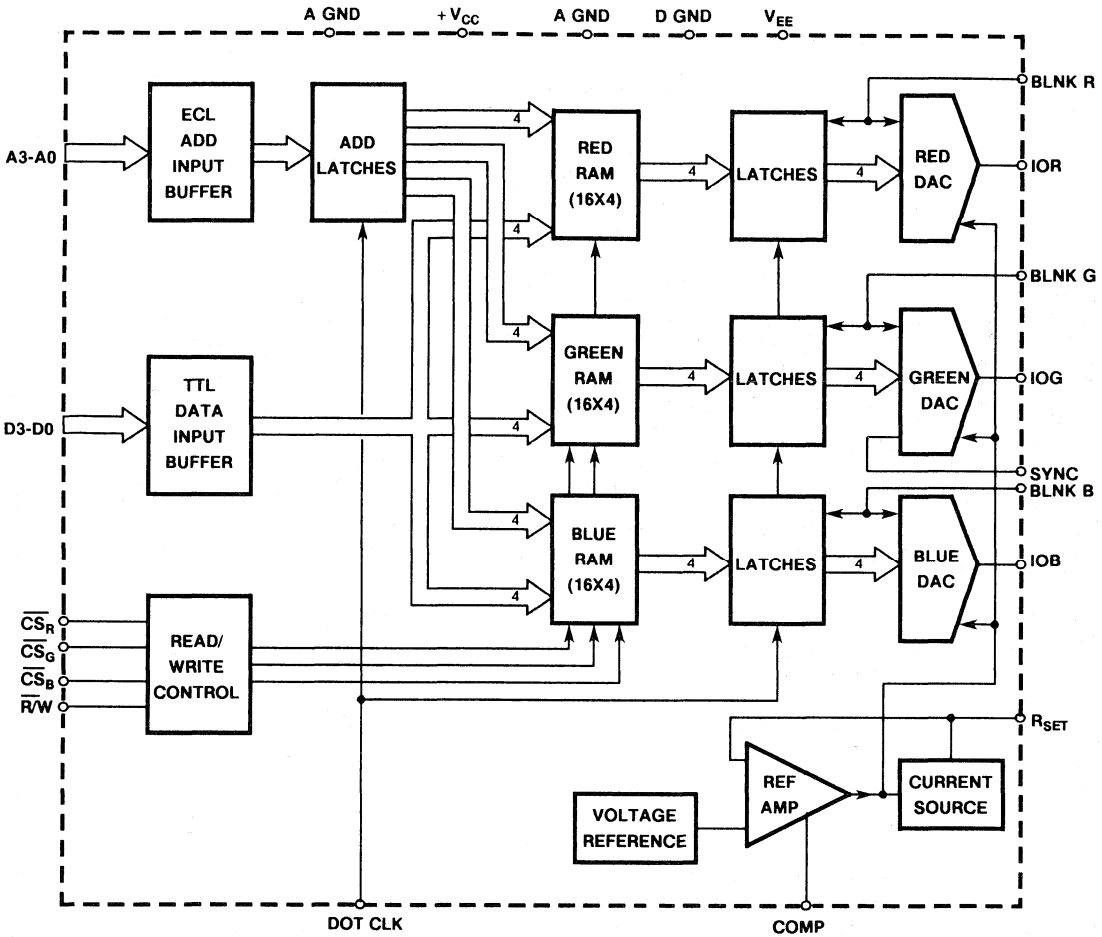



*Fig.2 ZN455 block diagram*

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| $V_{CC}$ | 5.0V ± 0.5V |
| $V_{EE}$ | −5.0V ± 0.5V |
| $R_{LOAD}$ | 37.5Ω |
| $R_{SET}$ | 180Ω |
| Operating temperature | 0°C to + 70°C |

## THERMAL CHARACTERISTICS

| Thermal resistance | DP | HP |
|---|---|---|
| Chip-to-case $\theta_{JC}$ | 15 | 15 |
| Chip-to-ambient $\theta_{JA}$ | 60 | 70 |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**
As specified in Recommended Operating Conditions

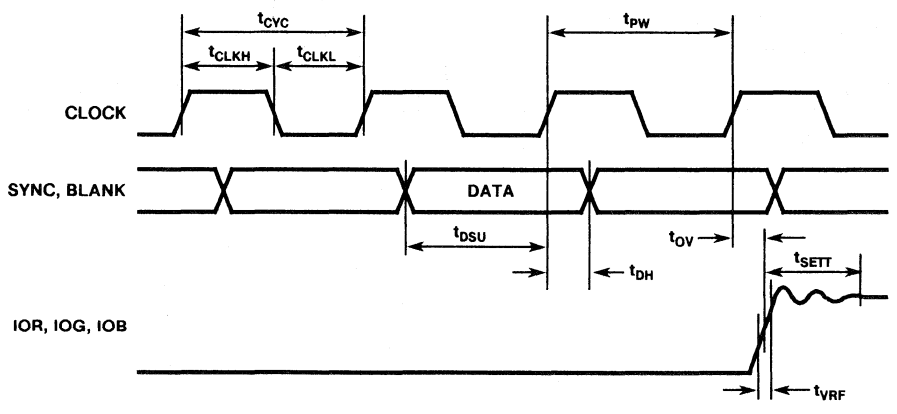
**DC CHARACTERISTICS**

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Resolution (each DAC) | | | 4 | | Bits | |
| LSB weight (current) | | | 1.14 | | mA | Note 1 |
| LSB weight (voltage) | | | 42.7 | | mV | Note 1 |
| **Accuracy (each DAC)** | | | | | | |
| Linearity error | | | 0.1 | 0.25 | LSB | |
| Differential linearity | | | ±0.1 | ±0.25 | LSB | |
| Offset error | | 0.12 | 0.56 | 1.45 | mV | |
| Gain error | | | | ±5% | Nom | |
| Temp. coefficient of gain error | | | | 500 | ppm/°C | |
| **Digital Inputs** | | | | | | |
| TTL input low voltage | $V_{IL}$ | | | 0.8 | V | |
| TTL input high voltage | $V_{IH}$ | 2.0 | | | V | |
| TTL input low current | $I_{IC}$ | -80 | -116 | -150 | μA | $V_{IL}$ = 0.4V |
| TTL input high current | $I_{IH}$ | | ±10 | | μA | $V_{IH}$ = 2.4V |
| ECL input low voltage | $V_{IL}$ | -1.4 | -1.32 | -1.3 | V | |
| ECL input high voltage | $V_{IH}$ | -1.1 | -1.05 | -0.9 | V | |
| ECL input low current | $I_{IL}$ | | 61 | | μA | $V_{IL}$ = -1.4V |
| ECL input high current | $I_{IH}$ | | 83 | | μA | $V_{IN}$ = 0.9V |
| **Analog OutputCurrents** | | | | | | |
| White level relative to blank level | | | 19.05 | | mA | Note 1. |
| White level relative to black level | | | 17.14 | | mA | |
| Black level relative to blank level | | | 1.89 | | mA | |
| Blank level relative to sync level (green only) | | | 7.62 | | mA | |
| DAC to DAC matching | | | 1 | | % | |
| Output compliance | | -1.0 | | +1.5 | V | |
| Internal voltage reference | $V_{REF}$ | | -1.26 | | V | |
| $V_{REF}$ temperature coefficient | | | 200 | | ppm/°C | |
| **Supply** | | | | | | |
| Positive rail | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V | |
| Negative rail | $V_{EE}$ | -4.5 | -5.0 | -5.5 | V | |
| Positive supply current | $I_{CC}$ | | 15.6 | 33 | mA | |
| Negative supply current | $I_{EE}$ | | 156 | 180 | mA | |
| Power dissipation | | | 0.86 | 1.09 | W | $V_{CC}$ = -$V_{EE}$ = 5V |

NOTES
1. Output levels adjustable with $R_{SET}$
2. Monotonicity guaranteed over full operating temperature range

## AC CHARACTERISTICS

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Clock rate (max.) | $f_{MAX}$ | 100 | | | MHz | |
| Clock cycle time | $t_{CYC}$ | 10 | | | ns | |
| Clock pulse width high time | $t_{CLCKH}$ | 4 | | | ns | |
| Clock pulse width low time | $t_{CLCKL}$ | 4 | | | ns | |
| **Write cycle timing** | | | | | | |
| Dot clock period | $t_{DC}$ | 10 | | | ns | |
| Address set up time | $t_{ASU}$ | 1.2 | 3.6 | 5.9 | ns | |
| Address hold time | $t_{AH}$ | 1.0 | 1.7 | 2.8 | ns | |
| Address stabilisation for write | $t_{ASW}$ | | | 10 | ns | |
| Data set up time | $t_{DSU}$ | 2.0 | 2.9 | 3.5 | ns | |
| Data hold time | $t_{DH}$ | 2.8 | 3.0 | 3.3 | ns | |
| $\overline{CS}$ high before R/$\overline{W}$ low | $t_{WL}$ | 2.0 | 4.5 | 7.5 | ns | |
| $\overline{CS}$ high after R/$\overline{W}$ high | $t_{WH}$ | 6.9 | 7.4 | 8.6 | ns | |
| $\overline{CS}$ write pulse width | $t_{WPW}$ | 20 | | | ns | |
| Delay between chip selects | $t_{DWP}$ | 20 | | | ns | |
| **Read cycle timing** | | | | | | |
| Dot clock period | $t_{DC}$ | 10 | | | ns | |
| Address set up time | $t_{ASU}$ | 1.2 | 3.6 | 5.9 | ns | |
| Address hold time | $t_{AH}$ | 1.0 | 1.7 | 2.8 | ns | |
| Sync set up time | $t_{SSU}$ | 6.1 | 7.0 | 10.0 | ns | |
| Sync hold time | $t_{SH}$ | 0 | 0.2 | 1.0 | ns | |
| Blank set up time | $t_{BSU}$ | 1.4 | 4.0 | 5.7 | ns | |
| Blank hold time | $t_{BH}$ | 0 | 0.2 | 1.0 | ns | |
| Output delay for Video | $t_{OV}$ | 6.25 | 7.3 | 8.2 | ns | |
| Output delay for Sync | $t_{OS}$ | 8.2 | 9.2 | 11.0 | ns | |
| Output delay for Blank | $t_{OB}$ | 7.8 | 9.1 | 11.0 | ns | |
| **DAC speed performance** | | | | | | |
| Rise/fall times | $t_{VRF}$ | | 6.0 | | ns | 10 to 90% to $\frac{1}{2}$ LSB |
| Settling times | $t_{SETT}$ | | | 10.0 | ns | |
| Slew rate | | | 100 | | V/$\mu$s | |
| Glitch energy | | | 60 | | pV-s | |
| Pipeline delay | $t_{PD}$ | 2 | 2 | 2 | Clock cycles | |




NOTES
1. Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
2. Settling time measured from the 50% point of full scale transition to the output remaining within ± 1/8 LSB.
3. Output rise/fall time measured between the 10% and 90% points of full scale transition.

*Fig.3 Timing diagram*

## CIRCUIT DESCRIPTION

Each D-A converter uses high speed switches to steer current from high precision sources to either analog ground or to the analog output depending on the input to the DAC. The output voltage is obtained from the current sources as the voltage drop across an external 37.5Ω load impedance.

Since current source output DACs are used, the output impedance is inherently high. A 75Ω shunt impedance is required to give the correct impedance to drive a 75Ω load terminating a 75Ω transmission line. The 1V p-p voltage is developed across this net 37.5Ω load.

The DACs produce a 16 level grey scale with a nominal current range of 0 to 17mA which gives 16 output voltages between 0 and -643mV across a 37.5Ω load. Reference white (0V) is produced by the digital code $1111_2$ and reference black (-643 mV) by the code $0000_2$. A logic '1' on the blank input overrides the data inputs and drives the output 71mV below reference black ('blacker than black'). The green DAC also has a sync input to allow the generation of composite synchronisation. A logic '1' on this input drives the output 286mV below the blanking level.

The full scale output voltage of the DACs are set using $R_{SET}$ which adjusts the current in the binary weighted sources. The voltage across the resistor between $R_{SET}$ and ground is compared with an internal reference and the current through it is adjusted until the voltages are equal.

The change in current through $R_{SET}$ is mirrored by the change in current through the current sources, and hence by the magnitude of the output voltage. Reducing the resistance between $R_{SET}$ and ground increases the current produced by the current sources and hence the output voltage.

To increase the throughput of the system, a two stage pipeline is used with the result that any output is delayed two clock cycles with respect to the input that caused it. On the blank and sync inputs, the pipeline consists of two latches in series to give the appropriate delay. The first stage of the pipeline is an address latch that holds the address input to the RAM stable for 1 clock cycle. In this time, the output of the RAM becomes stable and is latched by the data latch that forms the second stage of the pipeline, ready for output through the DAC.

The three blocks of RAM share a common address bus, but separate data buses. To reduce the pin count, the buses are multiplexed onto a single 4-bit bus under the control of four signals. $\overline{R}/W$ controls the flow of data into and out of the RAM. While $\overline{R}/W$ is low, data is transferred from RAM into the data latches for output. If $\overline{R}/W$ is high, the RAMs are enabled for the transfer of data from the data inputs into the RAMs. During this period, a low on one of the select lines $\overline{CS}_R$, $\overline{CS}_G$ or $\overline{CS}_B$ while the data inputs are stable writes that data into the red, green or blue RAM.

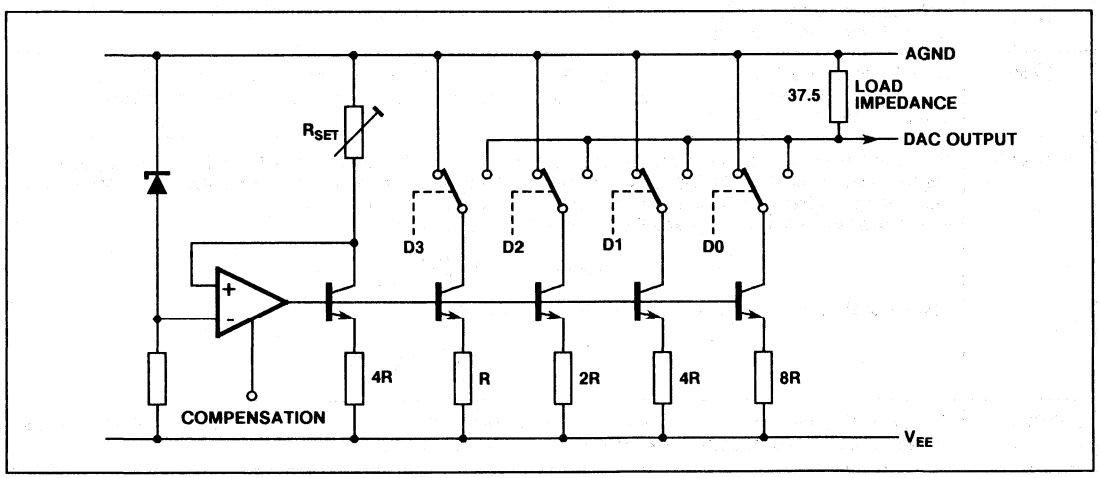



*Fig.4 Current switching DAC schematic*

| Description | IOG (mA) | IOR, IOB (mA) | SYNC | BLANK | DAC Input Data |
|---|---|---|---|---|---|
| WHITE | 0.00 | 0.00 | 0 | 0 | $F |
| DATA | Data | Data | 1 | 1 | Data |
| BLACK | -17.14 | -17.14 | 0 | 0 | $0 |
| BLANK | -19.05 | -19.05 | 0 | 1 | $x |
| SYNC | -26.66 | -119.05 | 1 | 1 | $x |

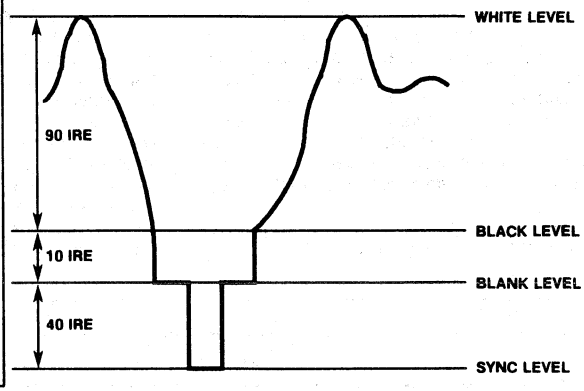
NOTE: Typical with full scale IOG = 26.67mA. $R_{SET}$ = 180Ω

*Table 1*

## PIN DESCRIPTIONS

| Pin name | Description |
|---|---|
| **BLANK** | Composite blank control input. A logic '1' forces the IOR, IOG and IOB outputs to the blanking level, as illustrated in Table 1. It is latched on the falling edge of CLOCK. When BLANK is a logic '1', the DATA inputs are ignored. |
| **SYNC** | Composite sync control input. A logic '1' on this input switches off a 40 IRE current source on the IOG output. SYNC does not override any other control or data input, as shown in Table 1; therefore it should be asserted only during the blanking interval. It is latched on the falling edge of CLOCK. |
| **DATA D0-D3** | Data bus (TTL compatible). D0 is the least significant data bit. They are latched on the falling edge of CLOCK. Coding is binary. Unused inputs should be connected to either the regular PCB power or ground plane. |
| **CLOCK** | Clock input (ECL compatible). The falling edge of CLOCK latches the D0-D3, A0-A3, SYNC and BLANK inputs. It is typically the pixel clock rate of the video system. |
| **IOR, IOG, IOB** | Red, Green and Blue current outputs. These high impedance current sources are capable of directly driving a doubly terminated 75Ω co-axial cable. All outputs, whether used or not, should have the same output load. (Note: A DC path to ground must be maintained) |
| **A0-A3** | Address select inputs (ECL compatible). These inputs specify the location of one of the 16 entries in the colour palette RAM. They are latched on the falling edge of the clock. A0 is the least significant bit. |
| $\overline{CS}_R$, $\overline{CS}_B$, $\overline{CS}_G$ | Chip select control inputs (TTL compatible). One of these inputs must be a logic'0' to enable data to be written to the device. Data can be written to one or more of the colour palette RAMs by asserting the relevant chip select input(s). |
| $\overline{R}/W$ | Read/Write control input (TTL compatible). To write data to the device, at least one of the $\overline{CS}$ inputs must be a logic '0' and $\overline{R}/W$ must be a logic '1'. To read data from the device, all $\overline{CS}$ inputs must be at logic '1' and $\overline{R}/W$ must be at logic '0'. |
| **FS ADJUST** | Full scale adjust control. A resistor ($R_{SET}$) connected between this pin and AGND controls the magnitude of the full video signal (Fig. 5). The current flowing in the $R_{SET}$ resistor is equal to 32 LSBs. Note that the IRE relationships in Fig. 5 are maintained, regardless of the full scale output current.<br>The relationship between $R_{SET}$ and the full scale current on IOG is:<br>$R_{SET}(\Omega) = 3810 \times \frac{V_{REF}\ (V)}{IOG\ (mA)}$<br>The full scale output current on IOR and IOB for a given $R_{SET}$ is defined as:<br>$IOR, IOB\ (mA) = 2721 \times \frac{V_{REF}\ (V)}{R_{SET}\ (\Omega)}$ |
| **COMP** | Compensation pin. This pin provides compensation for the internal loop amplifier. A 0.01μF ceramic capacitor must be connected between this pin and the nearest AGND pin. |
| $V_{CC}$ | Digital power, positive supply |
| $V_{EE}$ | Negative supply, combined analog and digital |
| **DGND** | Digital ground |
| **AGND** | Analog ground |

| Red/Blue | | Green | |
|---|---|---|---|
| mA | V | mA | V |
| 00.00 | 00.00 | 00.00 | 0.00 |
| -17.14 | -0.643 | -17.14 | -0.643 |
| -19.05 | -0.714 | -19.05 | -0.714 |
| | | -26.66 | -1.000 |




NOTE : 75Ω doubly terminated load, $R_{SET}$ = 180Ω, $V_{REF}$ = 1.26V, RS-343A levels assumed

*Fig.5 Composite video output waveform*

| A3 | A2 | A1 | A0 | RAM location |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Colour palette $0 |
| 0 | 0 | 0 | 1 | Colour palette $1 |
| 0 | 0 | 1 | 0 | Colour palette $2 |
| 0 | 1 | 1 | 1 | Colour palette $3 |
| 0 | 0 | 0 | 0 | Colour palette $4 |
| ↓ | ↓ | ↓ | ↓ | ↓ |
| 1 | 1 | 1 | 0 | Colour palette $14 |
| 1 | 1 | 1 | 1 | Colour palette $15 |

*Table 2 Read and Write address truth table*

## APPLICATION NOTES

### Microprocessor Interface

The microprocessor interface is used to write palette information into the ZN455. It is not possible to read this data back to the microprocessor so the system should keep a separate record of what is stored in the palette.

The address to be accessed is latched onto the inputs of the RAM by Dot Clock as the first stage of the pipeline. The write cycle can be performed asynchronously to the Dot Clock by allowing $t_{DC} + t_{ASW}$ between the address becoming stable and one of the select lines going low.

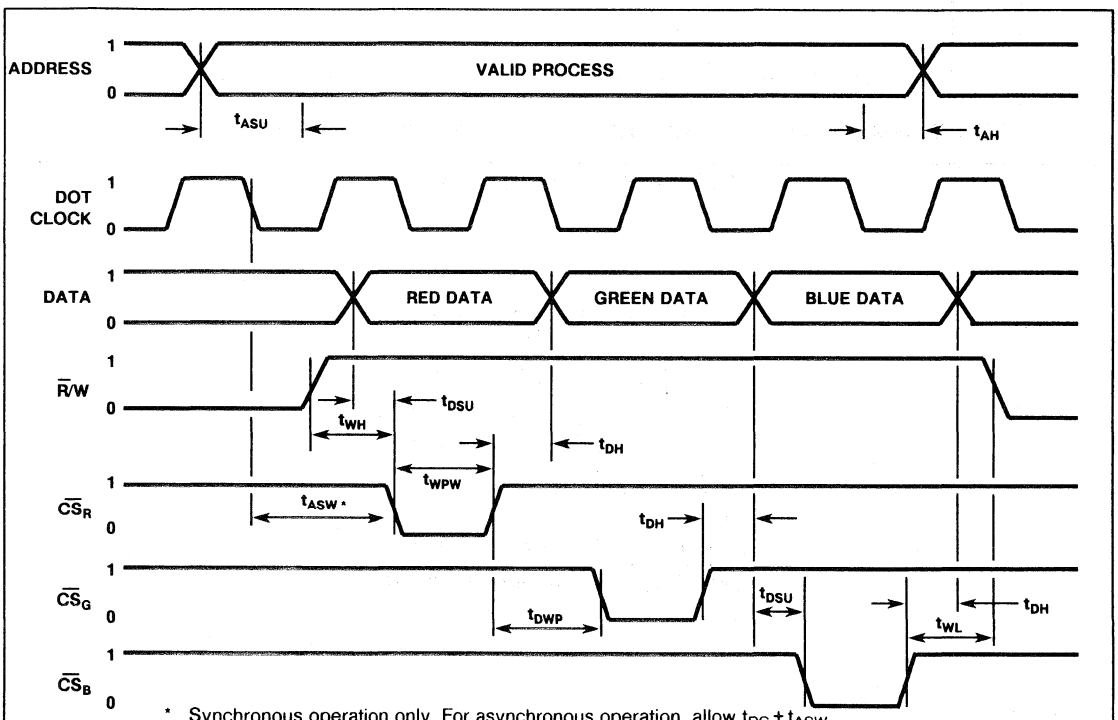
This guarantees that the address inputs have been stable over an active clock edge to latch them and the latch outputs and address decode have had time to stabilise. The address must be held stable over the whole of the write cycle.

$\overline{R}/W$ should be taken high to initiate a write cycle at least $t_{WH}$ before any of the selects go low.

If more than one address is to be written into, $\overline{R}/W$ can be left high provided $t_{DC} + t_{ASW}$ is allowed after the new address become stable and before any of the selects go low, and $t_{DWP}$ is allowed between subsequent selects.

The red, green and blue components can be written in any order or can be left unwritten if required. For example it is possible to modify only the green components of the palette without having to access the red and blue components.

Taking $\overline{R}/W$ low places the ZN455 into read mode where video data is output to the monitor. All address, sync and blank operations are carried out synchronously to Dot Clock. If the palette is to be updated it must be performed while either or both of sync and blank are high and $\overline{R}/W$ must return low before either of them return low to prevent corruption of the image.




* Synchronous operation only. For asynchronous operation, allow $t_{DC} + t_{ASW}$

Dot clock is asynchronous to the write cycle and no relation between it and the other Write cycle signals exist except where indicated.

*Fig.6 Write cycle timing*

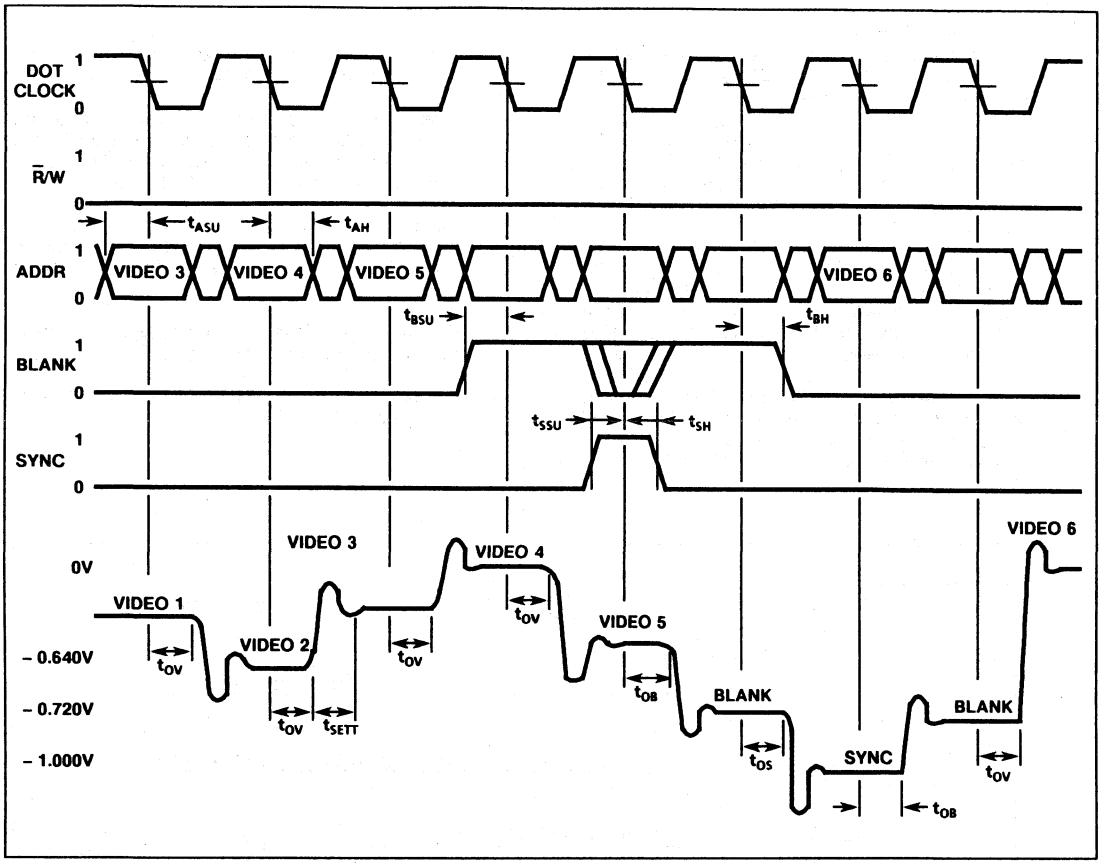



*Fig.7 Read cycle timing*

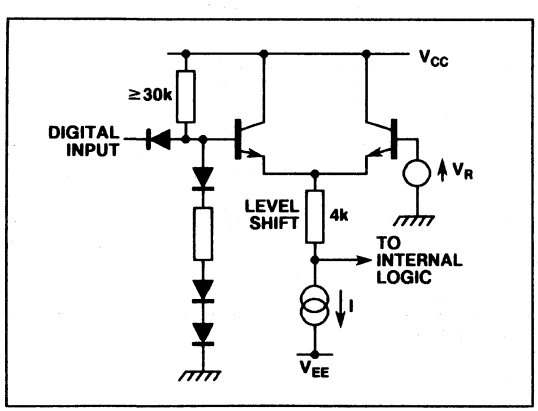



*Fig.8 Equivalent circuit of TTL inputs*

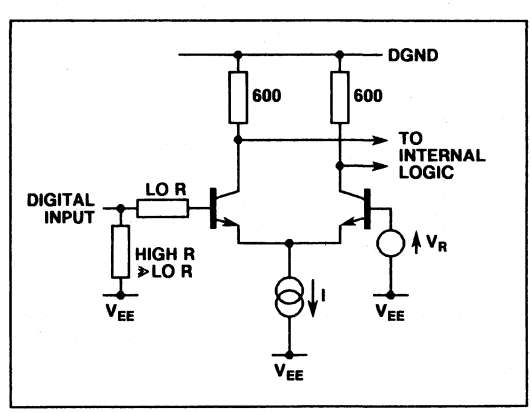



*Fig.9 Equivalent circuit of ECL inputs*

## LAYOUT CONSIDERATIONS

As with any high speed system, special care must be taken when laying out a PCB for the ZN455. A number of points require special consideration.

1. The analog and digital ground planes should be kept separate as far as possible. If possible connect them only at the ground terminal of the PSU. The ground planes should be as large as possible.

2. $V_{EE}$ and $V_{CC}$ should be decoupled to Digital Ground not Analog Ground by a 0.1μF ceramic capacitor in parallel with a 10μF 16V tantalum capacitor. These should be mounted as close as possible to the device.

3. The circuitry for the $R_{SET}$ pin, Comp pin and Analog outputs must connect to the analog ground only, as should the ground lines to the monitor. This will minimise noise on the analog lines.

4. The 75Ω pull-ups on the DAC outputs should be mounted as close as possible to the device.

5. Whenever possible, solder the device into the board. If a socket must be used, ensure it is a high quality part with low capacitance. The use of a socket is not recommended for this device.

6. Keep all lines as short as possible and as well separated as possible. It is especially important to keep the digital lines separate from the analog lines.

7. Keep the digital lines as well matched as possible to minimise skew between signals.

8. The outputs should be used to drive a 75Ω load to analog ground only.

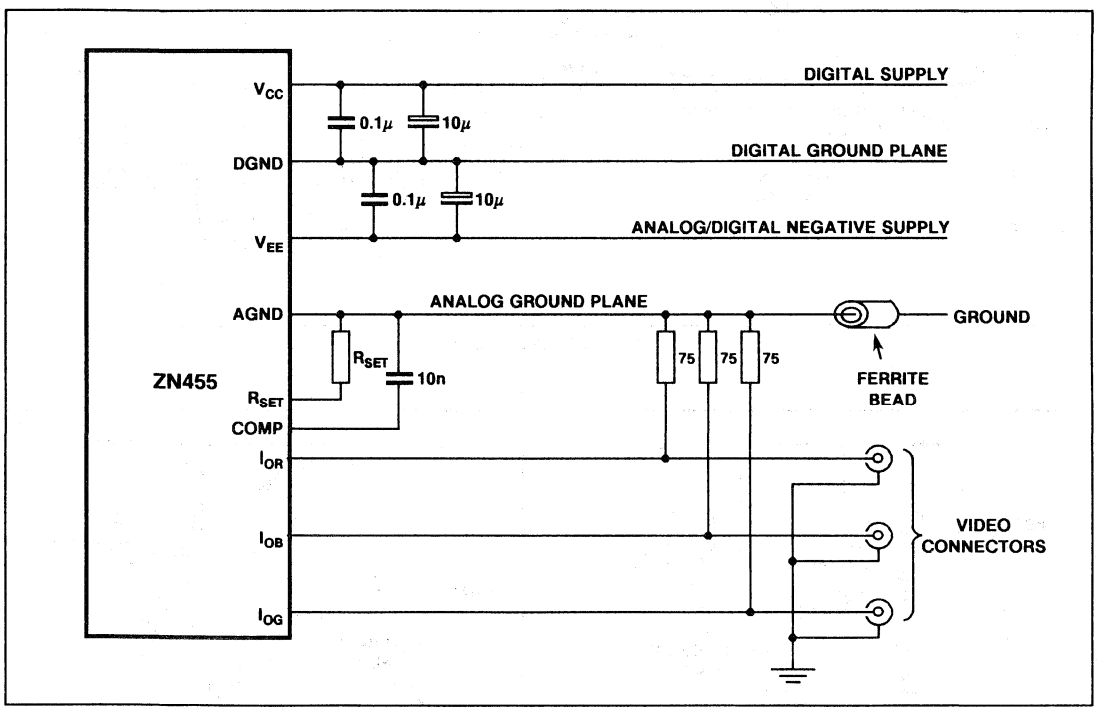



*Fig.10 Recommended analog circuitry*

# ZN501AJ

## 10-BIT MICROPROCESSOR COMPATIBLE A-D CONVERTERS

The ZN501 successive approximation A-D converter combines several innovations. The chip consists of a current switching array (requiring no trim), successive approximation logic, 2.5V precision reference, reference amplifier comparator and three-state output buffers.

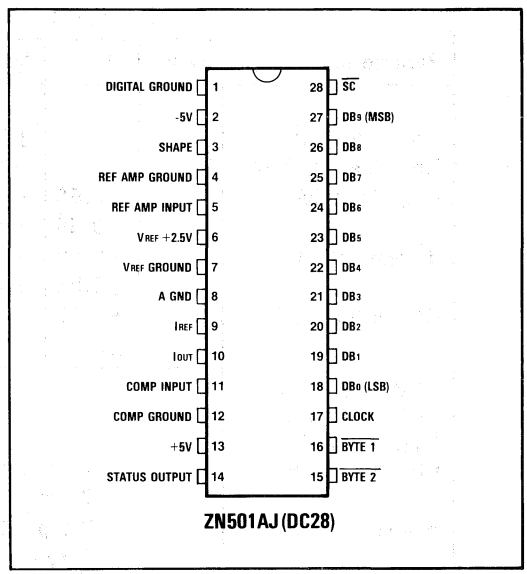
With the aid of $\overline{\text{BYTE1}}$ and $\overline{\text{BYTE2}}$, the 10 bits of output data can be read as a 10-bit word or as 8-bit and 2-bit words.

### FEATURES

- Linearity ±0.5 LSB
- Three-State Outputs, TTL Compatible
- 15μs Typ., 20μs Guaranteed Conversion Time
- Input Range as Desired
- Asynchronous Start Convert
- +5V, -5V Supplies
- Military Temperature Range
- Full 8-Bit or 16-Bit Micro Bus Interface

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| ZN501AJ | -55°C to +125°C | DC28 |




Pin connections - top view

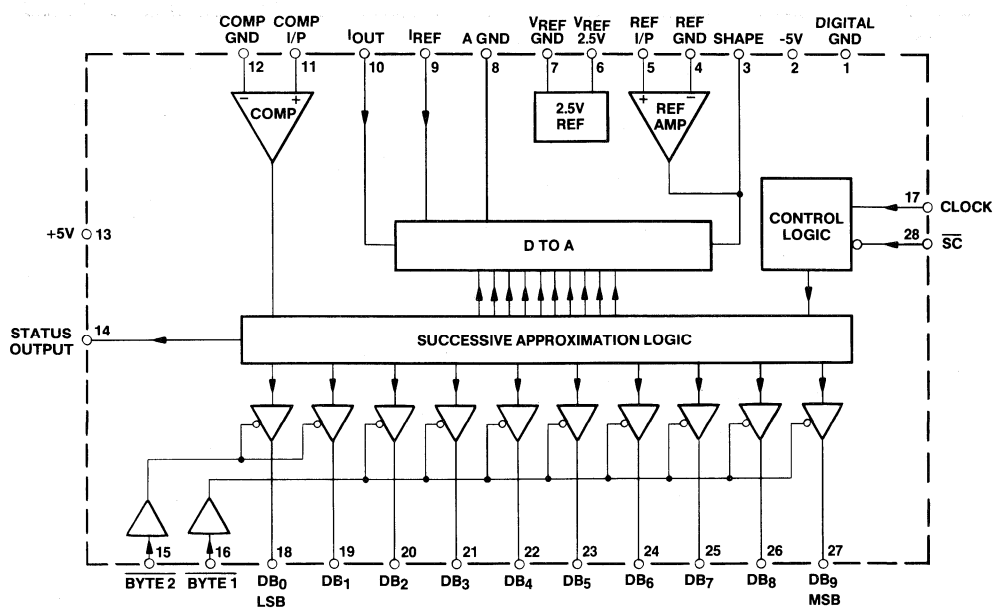



Fig.1 System diagram

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}+$ | +7V |
| Supply voltage $V_{CC}-$ | -7V |
| Logic input voltage | $+V_{CC}$ and 0V |
| Operating temperature range | -55°C to +125°C (ZN501AJ) |
| Storage temperature range | -55°C to +125°C |

**ELECTRICAL CHARACTERISTICS** (at +5 and −5V supplies and internal reference unless otherwise specified).

| Parameter | $T_{amb}$ = +25°C Min. | Typ. | Max. | Over Spec Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| Linearity error | | | ±0.5 | | ±0.5 | LSB | |
| Diff. linearity error | | | ±0.75 | | ±0.75 | LSB | Note 1 |
| Unipolar offset | | ±0.55 | ±1.0 | | ±1.0 | LSB | Ext. Ref. |
| | | ±0.55 | ±1.0 | | ±1.0 | LSB | Int. Ref. |
| Bipolar offset | | ±0.55 | ±1.0 | | ±1.0 | LSB | Ext. Ref. |
| | | ±0.55 | ±1.0 | | ±1.0 | LSB | Int. Ref. |
| Gain error | | ±0.55 | | | | LSB | Ext. Ref.* |
| | | ±3 | | | | LSB | Int. Ref.* |
| TEMPERATURE COEFFICIENTS ($T_{min}$ to $T_{max}$) | | | | | | | |
| Unipolar offset | | 7 typ., 10 max. | | | | ppm/°C | Ext. Ref. |
| | | 7 typ., 10 max. | | | | ppm/°C | Int. Ref. |
| Bipolar offset | | 7 typ., 10 max. | | | | ppm/°C | Ext. Ref. |
| | | 7 typ., 10 max | | | | ppm/°C | Int. Ref. |
| Gain | | 10 typ. | | | | ppm/°C | Ext. Ref. |
| | | 50 typ. | | | | ppm/°C | Int. Ref. |

*See note 4

**ELECTRICAL CHARACTERISTICS** (Cont.)

| Parameter | $T_{amb} = +25°C$ Min. | Typ. | Max. | Over Spec Min. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|---|
| Resolution | 10 | – | – | – | – | bits | |
| Conversion time (min) | 10 | 15 | 20 | 15 | 20 | μs | Note 2 |
| DAC reference $I_{ref}$ | 0.25 | 0.5 | 1.0 | 0.25 | 1.0 | mA | Note 5 |
| Nominal analogue input range | −2.5 | – | +2.5 | – | – | V | Note 3 |
| Supply rejection | – | 0.1 | – | – | – | % per V | |
| Supply voltage $+V_{CC}$ | +4.5 | +5 | +5.5 | +4.5 | +5.5 | V | |
| $-V_{CC}$ | −4.5 | −5 | −5.5 | −4.5 | −5.5 | V | |
| Supply current $+I_{CC}$ | – | 30 | 40 | – | – | mA | $+V_{CC} = +5V$ |
| $-I_{CC}$ | – | 21 | 28 | – | – | mA | $-V_{CC} = -5V$ |
| Power consumption | – | 255 | 340 | – | – | mW | |
| INTERNAL VOLTAGE REFERENCE | | | | | | | |
| Output voltage | – | 2.480 | – | – | – | V | |
| Output voltage tolerance | – | – | ±3.0 | – | – | % | |
| $V_{REF}$ temp. coeff. | – | – | – | 26 | 50 | ppm/°C | |
| Slope impedance | – | 0.75 | – | – | – | Ω | |
| Max. load current | – | ±2.0 | – | – | – | mA | |
| LOGIC | | | | | | | |
| $\overline{START\ CONVERT}$ $\overline{SC}$ | | | | | | | |
| High level inpV $V_{ih}$ | 2.0 | – | – | 2.0 | – | V | |
| Low level inpV $V_{il}$ | – | – | 0.8 | – | 0.8 | V | |
| High level inpI $I_{ih}$ | – | 18.0 | – | – | – | μA | $V_{CC} = \pm 5.5V$ $V_{in} = 5.5V$ |
| High level inpI $I_{ih}$ | – | 8.0 | – | – | – | μA | $V_{CC} \pm 5.5V$ $V_{in} = 2.4V$ |
| Low level inpI $I_{il}$ | – | 4.0 | – | – | – | μA | $V_{CC} \pm 5.5V$ $V_{in} + 0.4V$ |

*See note 4

**ELECTRICAL CHARACTERISTICS** (Cont.)

| Parameter | $T_{amb}$ = +25°C | | | Over Spec | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| LOGIC | | | | | | | |
| $\overline{BYTE}$ 1 and 2 | | | | | | | |
| High level inpV $V_{ih}$ | 2.0 | – | – | 2.0 | – | V | |
| Low level inpV $V_{il}$ | – | – | 0.8 | – | 0.8 | V | |
| High level inpI $I_{ih}$ | – | 18.0 | – | – | – | μA | $V_{CC}$ = ±5.5V<br>$V_{in}$ = 5.5V |
| High level inpI $I_{ih}$ | – | 12.0 | – | – | – | μA | $V_{CC}$ = ±5.5V<br>$V_{in}$ = 2.4V |
| Low level inpI $I_{il}$ | – | 2.0 | – | – | – | μA | $V_{CC}$ = ±5.5V<br>$V_{in}$ = 0.4V |
| CLOCK | | | | | | | |
| CLOCK high period | 0.5 | – | – | – | – | μs | |
| Max. clock frequency | 550 | 730 | 1100 | 550 | 730 | KHz | |
| High level inpV $V_{ih}$ | 2.0 | – | – | 2.0 | – | V | |
| Low level inpV $V_{il}$ | – | – | 0.8 | – | 0.8 | V | |
| High level inpI $I_{ih}$ | – | 15.0 | – | – | – | μA | $V_{CC}$ = ±5.5V<br>$V_{in}$ = 5.5V |
| High level inpI $I_{ih}$ | – | 5.0 | – | – | – | μA | $V_{CC}$ = ±5.5V<br>$V_{in}$ = 2.4V |
| Low level inpI $I_{il}$ | – | 3.0 | – | – | – | μA | $V_{CC}$ = ±5.5V<br>$V_{in}$ = 0.4V |
| High level OPV $V_{oh}$ | 2.4 | – | – | 2.4 | – | V | $V_{CC}$ = ±5V |
| Low level OPV $V_{ol}$ | – | – | 0.4 | – | 0.4 | V | |
| High level OPI $I_{oh}$ | – | – | −700 | – | – | μA | |
| Low level OPI $I_{ol}$ | – | – | 2.0 | – | – | mA | |
| Three-state DISABLE output leakage | – | – | ±2.0 | – | – | μA | $V_{out}$ = 1.3V |
| $\overline{BYTE}$ input to data output delays | – | 200 | 260 | – | – | ns | |
| ENABLE/DISABLE | | | | | | | |
| Delay time TE1 | 100 | 220 | 260 | – | – | ns | Note 6 |
| TEO | 60 | 80 | 100 | – | – | ns | |
| TD1 | 100 | 120 | 140 | – | – | ns | |
| TDO | 30 | 60 | 100 | – | – | ns | |
| $\overline{SC}$ pulse width | 100 | – | – | – | – | ns | |
| $\overline{SC}$ input to STATUS | – | 180 | – | – | – | ns | |

Note 1 No missing codes over full temperature range at appropriate accuracy.

Note 2 The maximum conversion time is 20μs. This corresponds to a clock rate of 550KHz based on 11 clock periods per conversion cycle (see timing diagram). This provides an update rate of 50KHz.

Note 3 Single polarity and other input ranges may be provided by different input resistor values.

Note 4 Gain error is trimmable to zero with the aid of R3.

Note 5 The full scale D-A output current $I_{out}$ = 4 times $I_{ref}$. For optimum performance $I_{ref}$ = 0.5mA.

Note 6 Refer to Fig. 9.

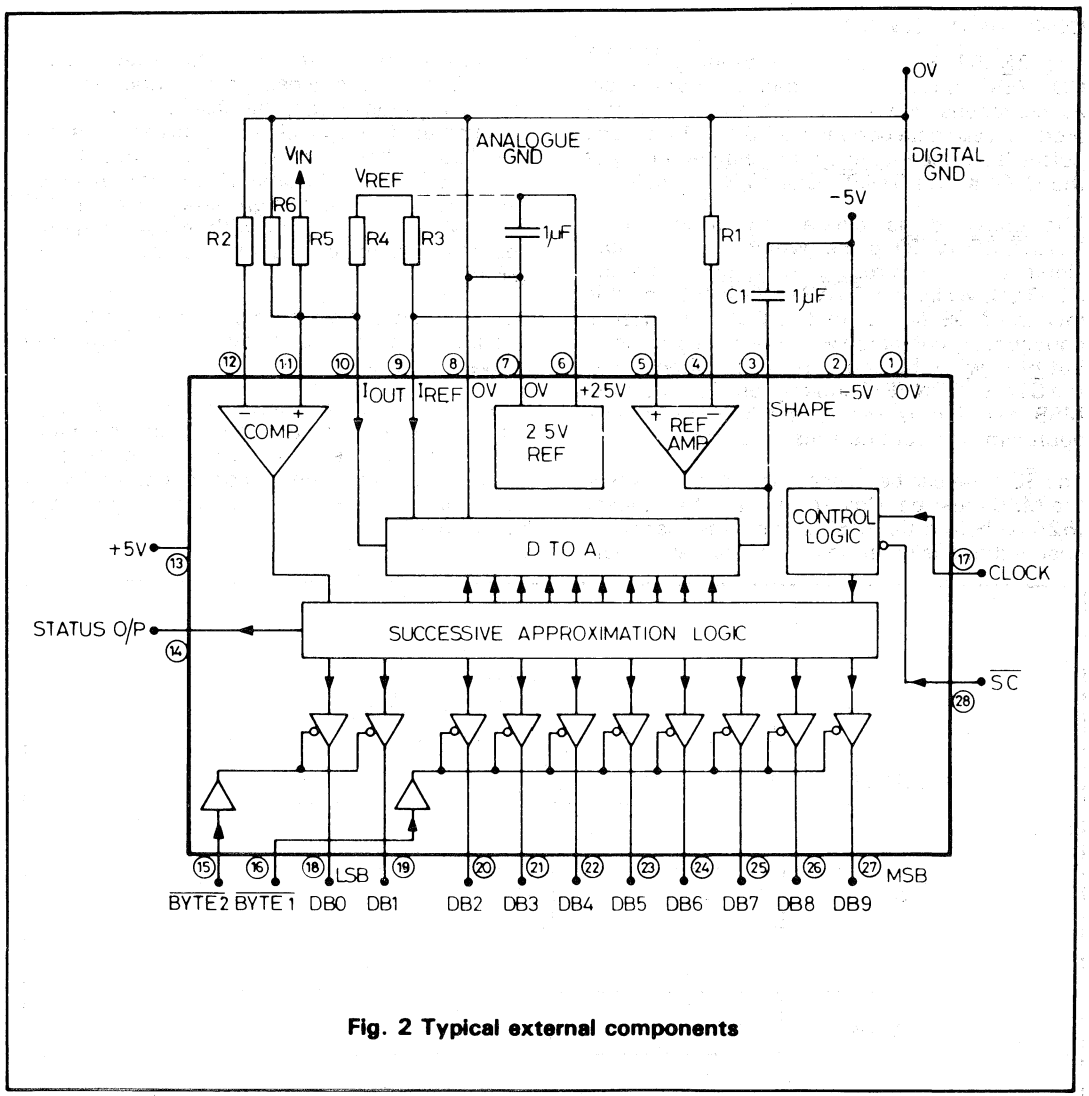



**Fig. 2 Typical external components**

## GENERAL CIRCUIT OPERATION

The ZN501 utilises the successive approximation technique. Upon receipt of a negative-going pulse at the $\overline{SC}$ input the STATUS output goes low, and the D-A converter input is set to the MSB. The resulting analogue output is compared with the unknown analogue input signal by means of the comparator. So if the analogue input is the larger, the MSB is left in circuit and if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all the 10-bits have been compared. On the 11th negative clock edge STATUS goes high indicating that the conversion is complete.

During a conversion $\overline{BYTE}$ 1 and $\overline{BYTE}$ 2 will normally be held high to keep the 3-state buffers in their high impedance state. Data can be read out by taking either $\overline{BYTE}$ 1 or $\overline{BYTE}$ 2 low, thus enabling the three-state outputs. $\overline{BYTE}$ 1 controls the 8 MSB's and $\overline{BYTE}$ 2 controls the 2 LSB's. Readout is non-destructive.

## CONVERSION TIMING

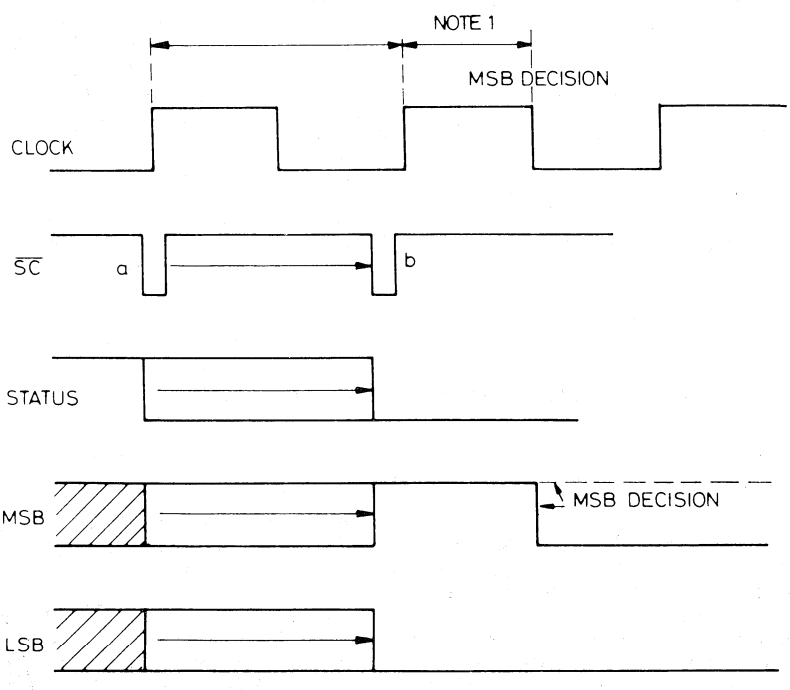
The ZN501 will accept a low-going $\overline{\text{START CONVERT}}$ pulse, which can be completely asynchronous with respect to the clock, and will produce valid data between 10.5 and 11.5 clock pulses later depending on the relative timing of the CLOCK and $\overline{\text{START CONVERT}}$ signals.

The converter is cleared by a low-going $\overline{\text{START CONVERT}}$ pulse, which sets the most significant bit and resets all the other bits and STATUS. Whilst the $\overline{\text{START CONVERT}}$ input is low the MSB output of the D-A converter is continuously compared with the analogue input, but otherwise the converter is inhibited. After the $\overline{\text{START CONVERT}}$ input goes high again the MSB decision is made and the successive approximation routine runs to completion.

The $\overline{\text{SC}}$ pulse can be as short as 100ns; however the MSB must be allowed to settle for at least (625ns) before the MSB decision is made. To ensure that this criterion is met even with short $\overline{\text{SC}}$ pulses the converter waits, after the $\overline{\text{SC}}$ input goes high, for a rising clock edge followed by a falling clock edge, the MSB decision being taken on the falling clock edge. This ensures that the MSB is allowed to settle for at least half a clock period, or (625ns) at maximum clock frequency. The clock high period and the $\overline{\text{SC}}$ pulse width must comply with this settling time i.e. clock high period + $\overline{\text{SC}}$ pulse width $\geqslant$625ns.

During a conversion the $\overline{\text{SC}}$ input is not locked out and if it is pulsed low at any time the conversion will restart.

At the end of a conversion STATUS waits 1 clock cycle before going high, so indicating that data is valid. The data outputs can be thus enabled anytime during a conversion and valid data will be available on the rising edge of the STATUS signal.




(Expanded inset)

**Fig. 3 Expanded timing diagram**

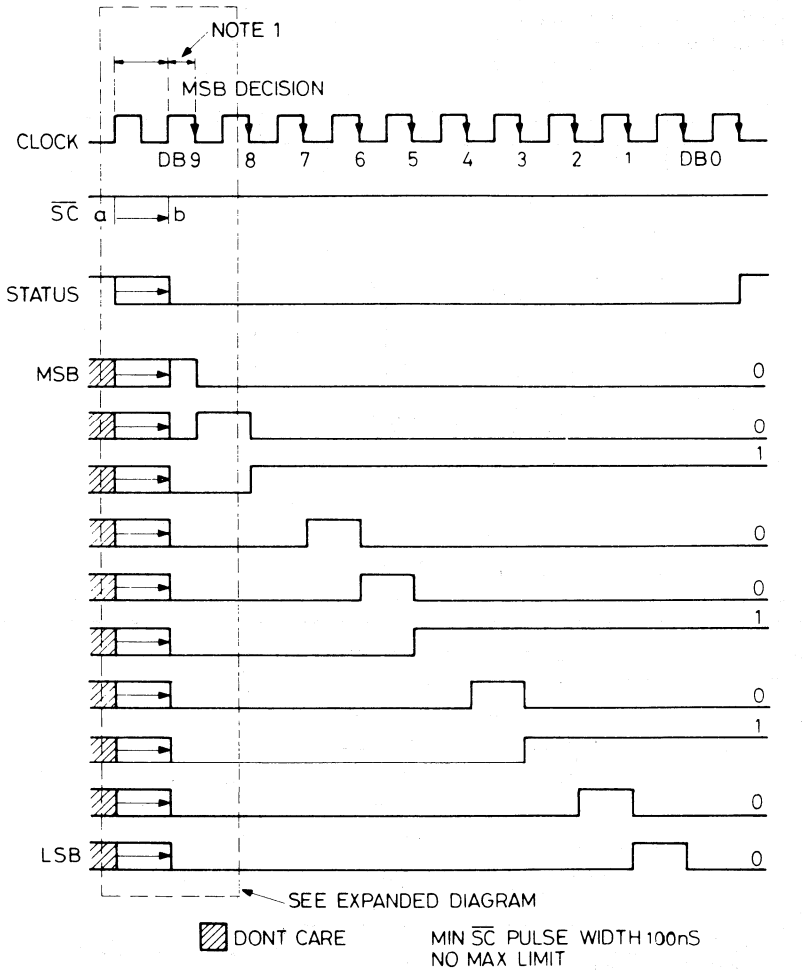



**Fig. 4 Timing diagram**

## CONTINUOUS CONVERSION

The converter can be made to cycle by inverting the STATUS output and feeding back to the $\overline{SC}$ input. To ensure that the converter starts reliably after power up an initial start pulse is required. This can be ensured by using a NOR gate instead of an inverter and feeding it with a positive going pulse which can be derived from a simple RC network that gives a single pulse when power is applied.

The propagation delay of the NOR gate determines the period over which STATUS remains high, during which time the data can be stored into latches. The time available for storing the data can be increased by inserting delays into the inverter path.

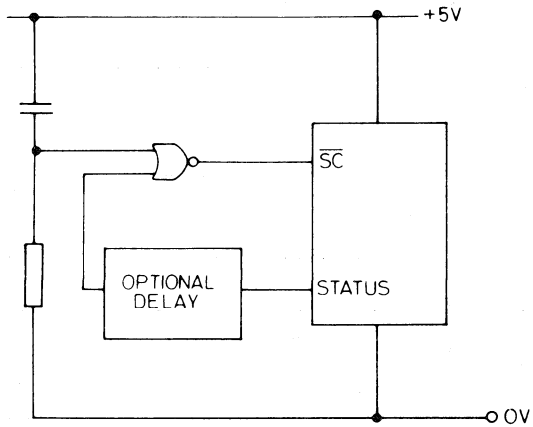



Fig. 5 Circuit for continuous conversion

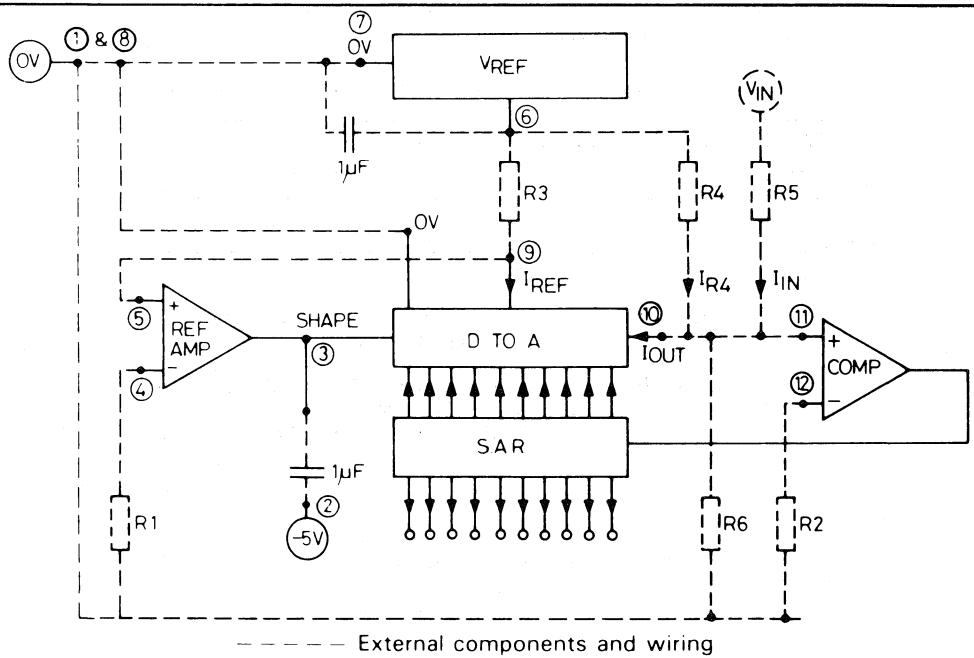



Fig. 6 External component connections

## CALCULATION OF EXTERNAL RESISTORS

If $V_{in\ max}$ is the voltage for the logic output to be all 1's.

$V_{in\ min}$ is the voltage for the logic output to be all 0's.

$$I_{out} = I_{R4} + I_{in}$$

$$I_{out} = \frac{V_{ref}}{R4} + \frac{V_{in}}{R5}$$

$I_{out} = 0$ (When $V_{in} = V_{in\ min}$)

$$\frac{V_{in\ min}}{R5} = -\frac{V_{ref}}{R4}$$

$$R4 = -\frac{V_{ref}\ R5}{V_{in\ min}}$$

$I_{out}$(f.s.) = 2mA: (When $V_{in} = V_{in\ max}$)

$$\frac{V_{in\ max}}{R5} + \frac{V_{ref}}{R4} = I_{out}(f.s.)$$

$$-\frac{V_{in\ min}}{R5} + \frac{V_{in\ max}}{R5} = I_{out}(f.s.)$$

$$R5 = \frac{V_{in\ max} - V_{in\ min}}{I_{out}(f.s.)}$$

It is important for gain stability that $I_{out}$(f.s.) of 2mA be kept constant, and this is done by the reference amplifier loop.

The current sources in the D-A itself cannot be checked directly so a number of reference current sources are distributed across the chip to monitor conditions all along the array.

$$\text{So } I_{ref} = 0.5mA$$

$$R3 = \frac{V_{ref}}{0.5mA}$$

$I_{out}$(f.s.) is four times $I_{ref}$.

R3 can affect gain stability and thus requires to be of high quality.
(Also slight variation in its value can act as a gain control).

R4 and R5 can affect offset stability and thus requires to be of high quality.
(Also slight variations in the value of R4 can act as an offset control).

R1 and R2 supply the bias currents of the reference amplifier and comparator.

$$\text{So } R1 = R3$$

and R2 = parallel combination of R4, R5 and R6

R6 should be chosen such that the parallel combination of R4, R5 and R6 is about 1.25KΩ as this determines the D-A time constant and hence conversion time.

**(THE FOLLOWING IS A TABLE OF VALUES TO GIVE EXAMPLES OF THE ABOVE EQUATIONS):**

| $V_{in\ max}$ | $V_{in\ min}$ | $V_{ref}$ | R1 (1) | R2 (1) | R3 | R4 | R5 | R6 (1) |
|---|---|---|---|---|---|---|---|---|
| + 2.5 | - 2.5 | 2.5 | 5K | 1.25K | 5K | 2.5K | 2.5K | ∞ |
| + 2.5 | 2.5 | 5* | 10K | 1.25K | 10K | 5.0K | 2.5K | 5.0K |
| + 2.5 | 0 | 2.5 | 5K | 1.25K | 5K | ∞ | 1.25K | ∞ |
| + 5.0 | 0 | 2.5 | 5K | 1.25K | 5K | ∞ | 2.5K | 2.5K |
| + 4.0 | 2.0 | 2.5 | 5K | 1.25K | 5K | 3.75K | 3.0K | 5.0K |
| + 4.0 | 2.0 | 12* | 24K | 1.25K | 24K | 3.75K | 3.0K | 5.0K |
| + 10 | 10 | 2.5 | 5K | 1.25K | 5K | 2.5K | 10K | 3.33K |
| + 10 | 0 | 2.5 | 5K | 1.25K | 5K | ∞ | 5K | 1.66K |

Note 1 Nearest prefered value may be used for R1, R2 and R6.

*Note 2 External reference.

For unipolar operation where R4 approaches (∞) and a zero adjustment is required, the following offset circuit is suggested in place of R4.

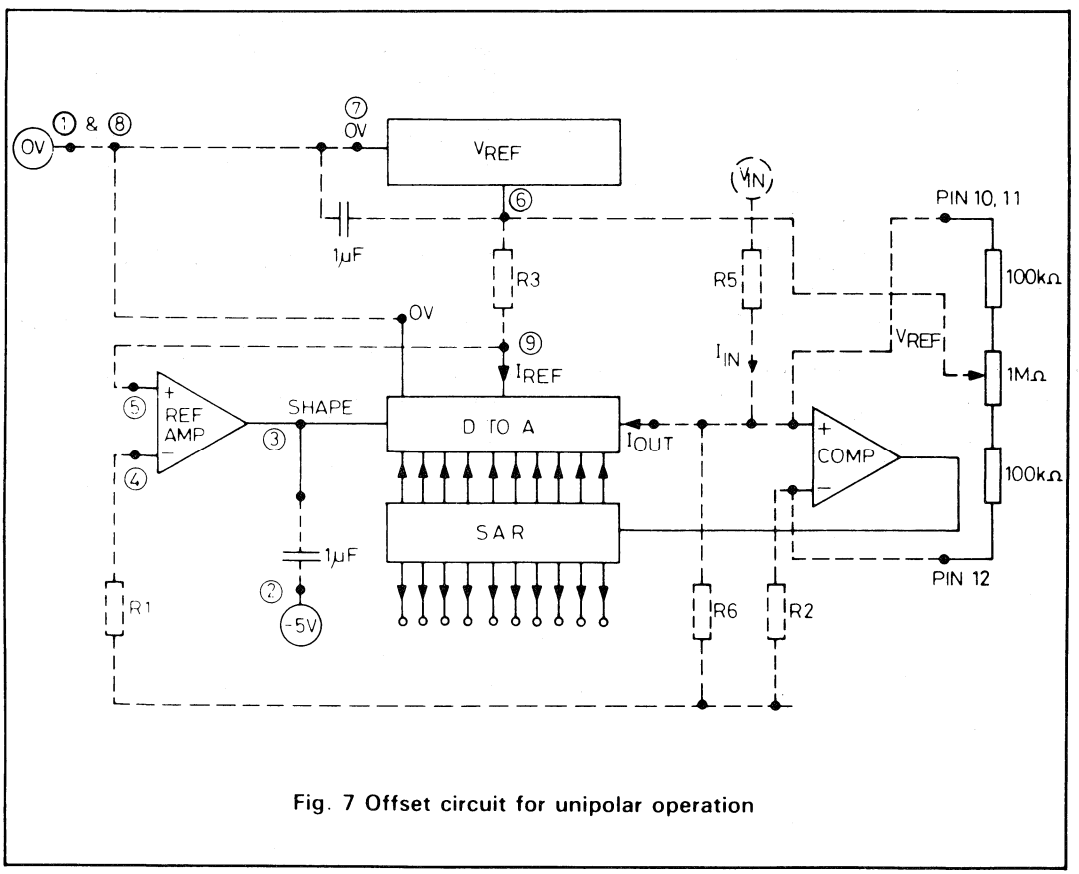



Fig. 7 Offset circuit for unipolar operation

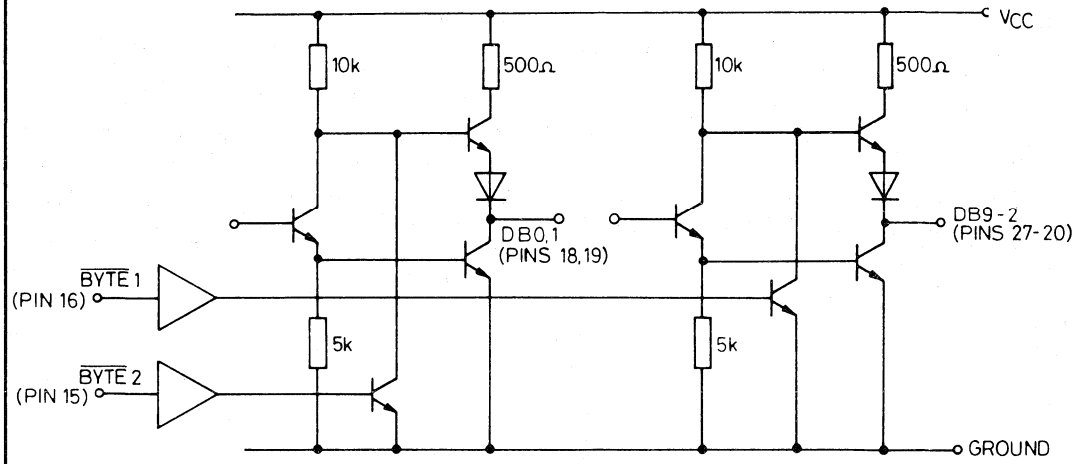
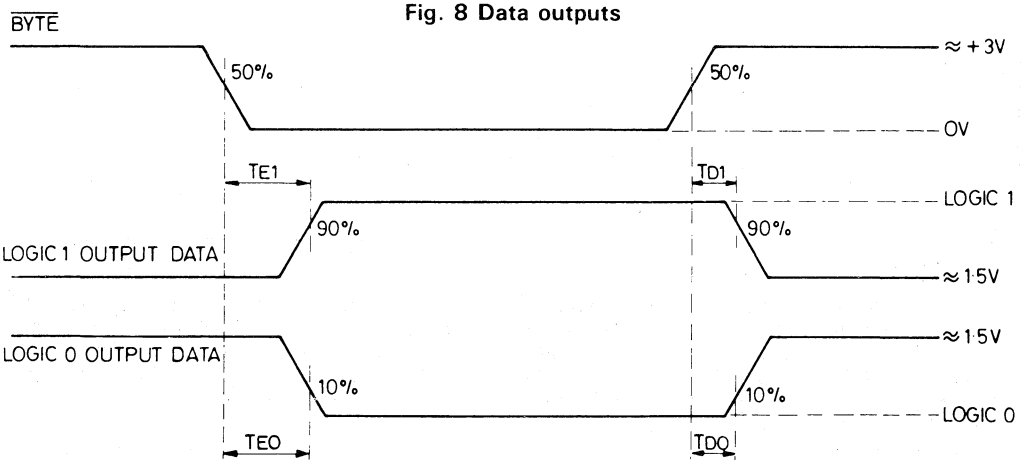



Fig. 8 Data outputs




TE = BYTE ENABLE DELAY TIME (CL = 50pF)
TD = BYTE DISABLE DELAY TIME (CL = 10pF)

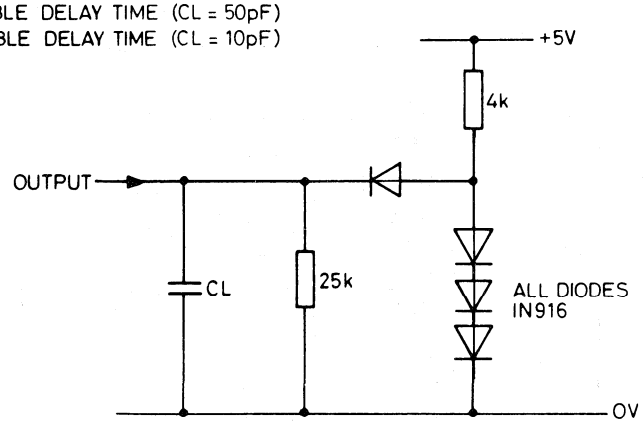



Fig. 9 Output enable/disable delays

## DATA OUTPUTS

The ZN501 has true three-state output buffers on chip, hence eliminating the need for external buffers and latch circuitry.

The two $\overline{\text{BYTE}}$ select pins $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2, control outputs DB9 to DB2, and outputs DB1 to DB0 respectively.

$\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 will normally be held high during a conversion to keep the three-state buffers in their high impedance state, and when data is ready, which will be signalled by a high going STATUS pulse, it can easily be read out by taking $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 low.

(A test circuit and timing diagram for the output enable/disable delays are given).

The STATUS output shown utilises a 5K internal pullup resistor for CMOS/TTL compatibility.

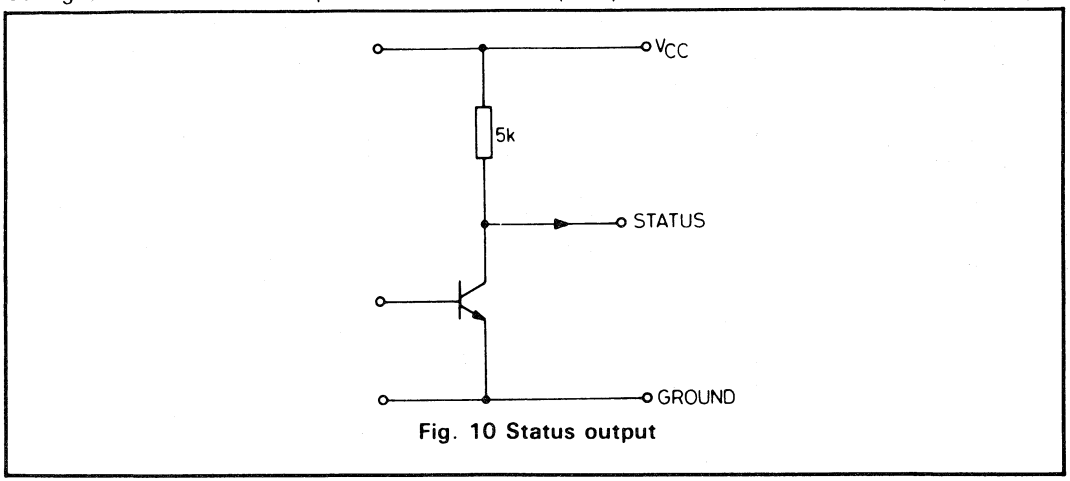



**Fig. 10 Status output**

## DATA BUS CONNECTIONS

The ZN501 can be connected directly to an 8-bit microprocessor bus, where the two LSB's would normally be hardwired to the desired upper bits, usually the 2 MSB's. Hence the data would be transferred in two words with control of them, from $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2.

For use with a 16-bit microprocessor, $\overline{\text{BYTE}}$ 1 and $\overline{\text{BYTE}}$ 2 would be tied together and all 10 bits would be enabled simultaneously. The 10-bit word could then be placed at either the higher or lower end of the 16-bit bus.

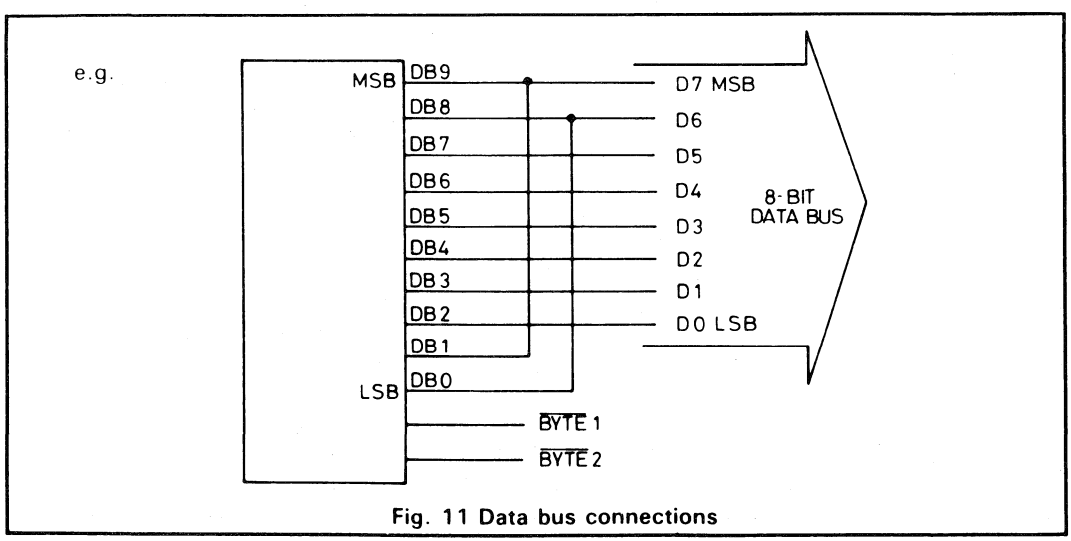



**Fig. 11 Data bus connections**

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| $\overline{\text{BYTE}}$ 1 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 |
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| $\overline{\text{BYTE}}$ 2 | DB1 | DB0 | X | X | X | X | X | X |

DATA TRANSFERRED IN TWO WORDS

**UNIPOLAR ADJUSTMENT PROCEDURE**

(i) Apply continuous $\overline{\text{START CONVERT}}$ pulse at intervals long enough to allow a complete conversion and monitor the digital outputs.

**OFFSET SETTING**

(ii) Apply ½LSB to $V_{in}$ and adjust the offset CIRCUIT until DBO (LSB) just flickers between 0 and 1 with all the other bits at 0.
i.e. for transition 0000000000 to 0000000001.

**GAIN SETTING**

(iii) Apply full-scale minus 1.½LSB to $V_{in}$ and adjust gain until DBO (LSB) just flickers between 0 and 1 with all other bits at 1.
i.e. for transition 1111111111 to 1111111110.

Note: R3 GAIN ADJUSTMENT.

**UNIPOLAR SETTING-UP POINTS**

| Input range +FS | ½LSB | F.S. – 1.½LSB |
|---|---|---|
| +2.5V<br>+5.0V | 1.22mV<br>2.441mV | 2.4963V<br>4.9926V |

$$1LSB = \frac{FS}{1024}$$

**UNIPOLAR LOGIC CODING**

| Analogue input (Nominal code centre value) | Digital output code MSB LSB |
|---|---|
| FS - 1LSB | 1111111111 |
| FS - 2LSB | 1111111110 |
| ¾.FS | 1100000000 |
| ½.FS + LSB | 1000000001 |
| ½.FS | 1000000000 |
| ½.FS - 1LSB | 0111111111 |
| ¼.FS | 0100000000 |
| 1LSB | 0000000001 |
| 0 | 0000000000 |

## BIPOLAR ADJUSTMENT PROCEDURE

(i) Apply continuous $\overline{\text{START CONVERT}}$ pulses at intervals long enough to allow a complete conversion and monitor the digital outputs.

## OFFSET SETTING

(ii) Apply −(FS − ½.LSB) to $V_{in}$ and adjust offset control until DBO (LSB) output just flickers between 0 and 1 with all other bits at 0.
i.e. for transistions 0000000000 to 0000000001.

Note: R4 OFFSET ADJUSTMENT.

## GAIN SETTING

(iii) Apply +(FS − 1½.LSB) to $V_{in}$ and adjust gain until DBO (LSB) just flickers between 0 and 1 with all cther bits at 0.
i.e. for transition 1111111111 to 1111111110.

Note: R3 GAIN ADJUSTMENT.

### BIPOLAR SETTING-UP POINTS

| Input range ±FS | −(FS − ½.LSB) | +(F.S. − 1.½.LSB) |
|---|---|---|
| ±2.5V | −2.4976V | +2.4927V |
| ±5.0V | −4.9951V | +4.9854V |

$$1LSB = \frac{2FS}{1024}$$

### BIPOLAR LOGIC CODING

| Analogue input (Nominal code centre value) | Digital output code MSB LSB |
|---|---|
| +(FS − 1LSB) | 1111111111 |
| +(FS − 2LSB) | 1111111110 |
| +(½.FS) | 1100000000 |
| +(1LSB) | 1000000001 |
| 0 | 1000000000 |
| −(1LSB) | 0111111111 |
| −(½.FS) | 0100000000 |
| −(FS − 1LSB) | 0000000001 |
| −FS | 0000000000 |

3016-1.0

# ZN508

## DUAL 8-BIT MICROPROCESSOR COMPATIBLE D-A CONVERTER

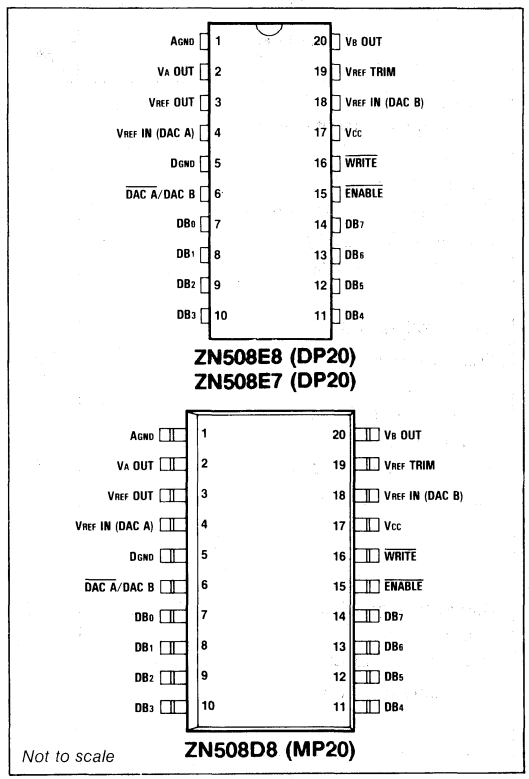
The ZN508 is a monolithic dual 8-bit DAC designed to be easily interfaced to microprocessors. Integrated on-chip are two 8-bit DAC's, a 2.5V trimmable bandgap reference, separate $V_{REF}$ inputs and data latches for each DAC. The on-chip reference not only can be used to drive the two DAC's but can be also used as a system reference. A consequence of the two DAC's being fabricated on the same chip is excellent, inherent, DAC to DAC matching.

### FEATURES

- 800ns Voltage Settling Time
- 2.5V trimmable Bandgap Reference
- Monotonic over Full Temperature Range
- Single + 5V Supply
- Excellent DAC to DAC Matching
- Separate $V_{REF}$IN for Each DAC
- Industrial Temperature Range

### ORDERING INFORMATION

| Device type | Linearity error(LSB) | Operating temperature | Package |
|---|---|---|---|
| **ZN508E7** | ±1 | –40°C to +85°C | DP20 |
| **ZN508E8** | ±0.5 | –40°C to +85°C | DP20 |
| **ZN508D8** | ±0.5 | –40°C to +85°C | MP20 |




*Pin connections - top view*

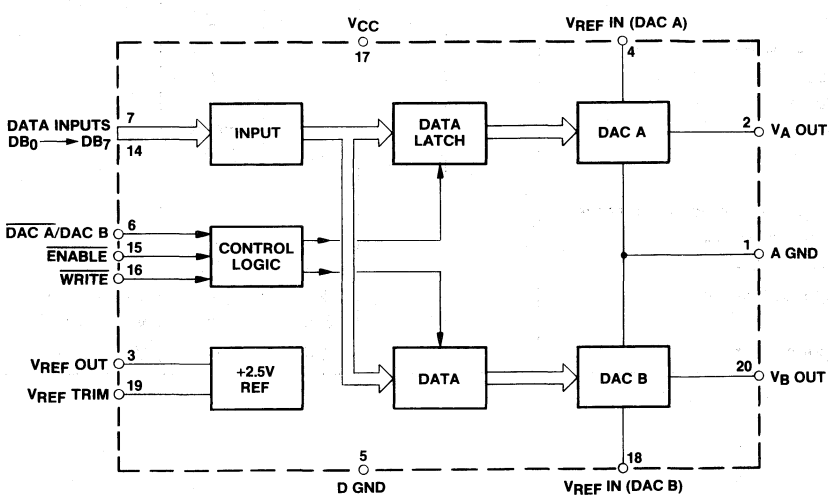



*Fig.1 System diagram*

## ABSOLUTE MAXIMUM RATINGS

Supply voltage $V_{CC}$ +7V
Max. voltage, logic and $V_{REF}$ input +$V_{CC}$
Operating temperture range
ZN508E and ZN508D -40°C to +85°C
ZN508J -55°C to 125°C
Storage temperature range -55°C to 125°C
Analog ground to digital ground ±200mV

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = 25°C

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| Linearity error | | | ±0.5 | LSB | |
| Differential linearity error | | | ±0.75 | LSB | |
| **All types** | | | | | |
| Linearity error TC | | ±3 | | ppm/°C | |
| Differential non-linearity TC | | ±6 | | ppm/°C | |
| Offset voltage ZN508E | | 2 | 5 | mV | All bits OFF |
| ZN508D | | 2 | 5 | mV | All bits OFF |
| Offset voltage TC | | ±3 | | ppm/°C | |
| Full scale output | 2.545 | 2.550 | 2.555 | V | External reference $V_{REF}$ IN = 2.560V, all bits ON |
| Full scale output TC | | 2 | | ppm/°C | |
| Analog output resistance | | 4 | | kΩ | |
| External reference voltage | 0 | | 3.0 | V | |
| Settling time to 0.5 LSB | | 800 | | ns | 1 LSB major transition (Note 1) |
| | | 1.25 | | µs | All bits ON to OFF or OFF to ON (Note 1) |
| Supply voltage ($V_{CC}$) | 4.5 | 5.0 | 5.5 | V | |
| Supply current | | 36 | | mA | |
| Power consumption | | 180 | | mW | |
| DC supply rejection | | -57 | | dB | $\Delta V_{CC}$ = 250µV p-p f ≤ 50kHz |
| Digital to analog glitch impulse | | | | nV-s | 00000000 11111111 |
| Channel to channel isolation | | | | | |
| $V_{REF\,A}$ to Out B | | -82 | | dB | f ≤ 50kHz |
| $V_{REF\,B}$ to Out A | | -82 | | dB | |
| **Internal voltage reference** | | | | | |
| Output voltage | | 2.5 | | V | |
| Slope impedance | | 1 | | Ω | |
| $V_{REF}$ OUT TC | | 50 | | ppm/°C | |
| Reference current | 1 | | 15 | mA | |
| **Logic** | | | | | |
| (over specified operating temperature range) | | | | | |
| High level input voltage $V_{IH}$ | 2.0 | | | V | |
| Low level input voltage $V_{IL}$ | | | 0.8 | V | |
| High level input current $I_{IH}$ | | | 20 | µA | $V_{IN}$ = 2.4, $V_{CC}$ = 5.5V |
| | | | 320 | µA | $V_{IN}$ = 5.5, $V_{CC}$ = 5.5V |
| Low level input current $I_{IL}$ | | | -310 | µA | $V_{IN}$ = 0.4V, $V_{CC}$ = 5.5V |

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **Switching characteristics** | | | | | |
| Chip select to write set up time $t_{CS}$ | 150 | | | ns | |
| Chip select to write hold time, $T_{CH}$ | 10 | | | ns | |
| DAC select to write set up time $t_{AS}$ | 150 | | | ns | |
| DAC select to write hold time $t_{AH}$ | 10 | | | ns | |
| Data valid to write set up time $t_{DS}$ | 100 | | | ns | |
| Data valid to write hold time $t_{DH}$ | 50 | | | ns | |
| Write pulse width $t_{WR}$ | 150 | | | ns | |

NOTE
1. $R_L$ = 10 Megohms $C_L$ = 10pF.

## D-A CONVERTER

The converters are of the voltage switching type and use an R-2R ladder network as shown in Fig.2. Each 2R element is connected to 0V or $V_{REF}$ IN by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

Analog output $= \frac{n}{256} (V_{REF}\ IN - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the data latch.

$V_{OS}$ is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of $V_{OS}$ is typically 1mV. This offset will normally be removed by the setting up procedure (see Operating Notes) and because the offset temperature coefficient is low ($\pm 6\mu V/°C$) the effect on accuracy is negligible.

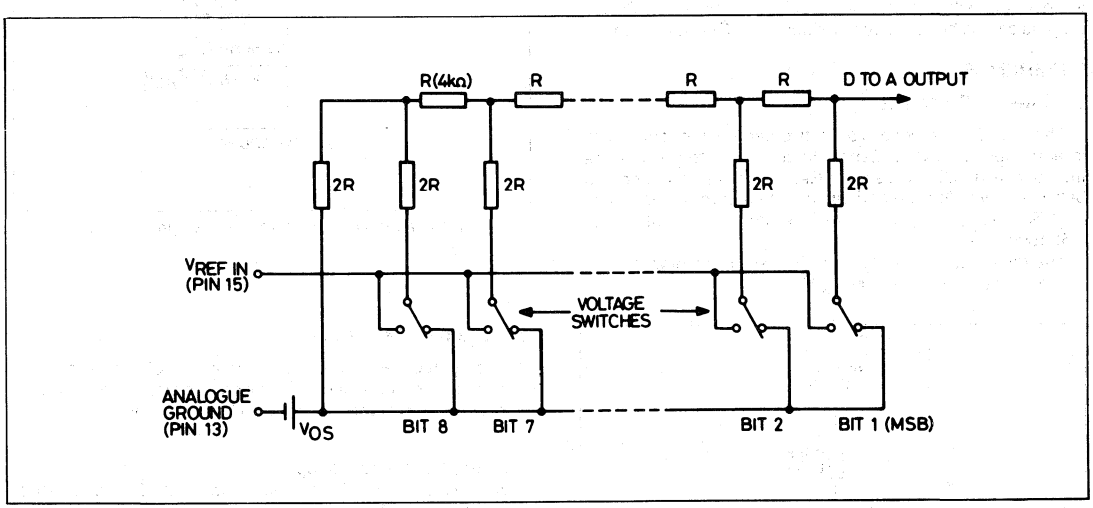



*Fig.2 The R-2R ladder network*

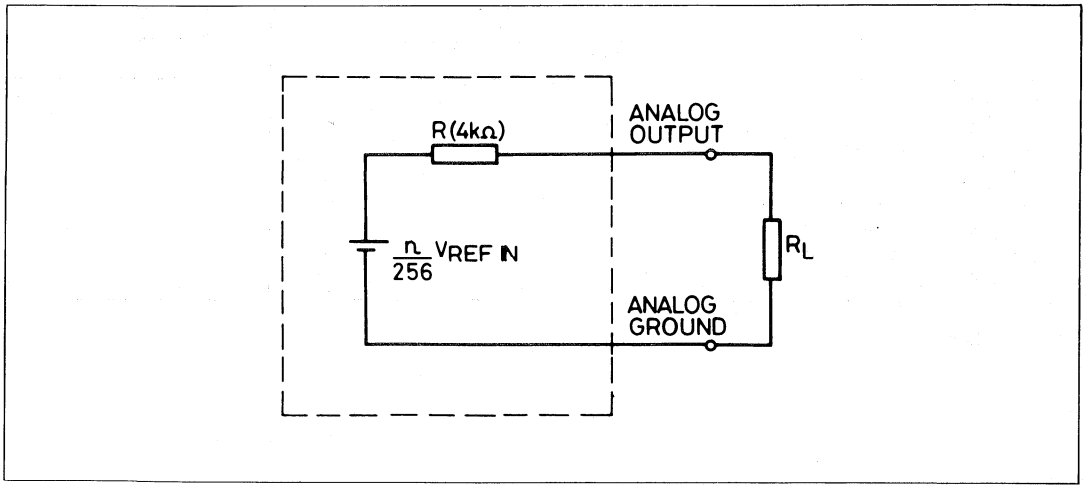



*Fig.3 Analog output equivalent circuit*

Fig.3 shows an equivalent circuit of the outputs (ignoring $V_{OS}$). The output resistance R has a temperature coefficient of ±0.2% per °C.
The gain drift due to this is $\frac{0.2R}{R + R_L}$ % per °C

$R_L$ should be chosen to be as large as possible to make the gain drift small. As an example if $R_L = 400k\Omega$ then the gain drift due to the TC of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN508 outputs can be buffered by amplifiers (see Operating Notes).

## REFERENCE

### 1. Internal Reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig.3). A resistor ($R_{REF}$), should be connected between $+V_{CC}$ (pin 11) and pin 15. The recommended value of 1.5k will supply a nominal reference current of (5-2.5)/1500 = 1.7mA.

The reference voltage can be trimmed by ±5% with a 10k potentiometer (as shown in Fig.5).

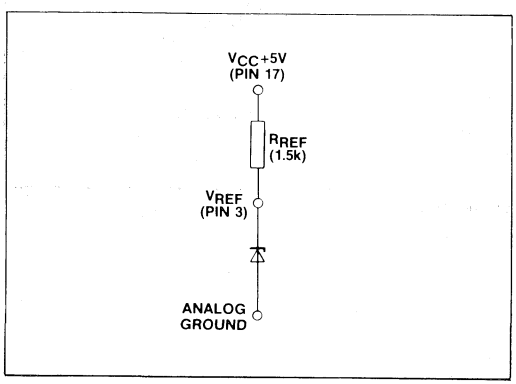



*Fig.4 Internal voltage reference*

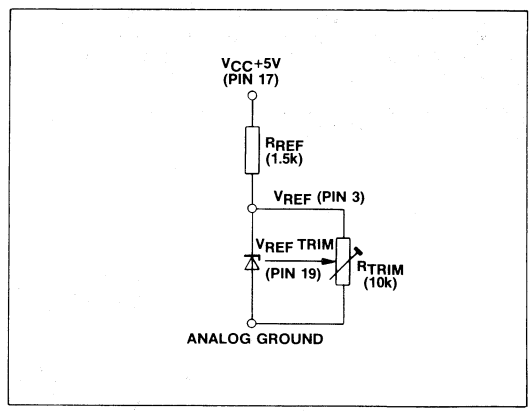



*Fig.5 Trimming circuit for the voltage reference*

### 2. External Reference

If required an external reference voltage may be connected to $V_{REF}$ IN. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

$V_{REF}$ IN can be varied from 0 to +3V for ratiometric operation. The ZN508 is guaranteed monotonic for $V_{REF}$ IN above 2V.

## LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. Both DAC A and DAC B share an internal data bus and an 8-bit input port. The DAC to be loaded with new data is chosen by $\overline{\text{DAC A}}$/DAC B select pin; DAC A when the input is low and DAC B when the input is high. When $\overline{\text{ENABLE}}$ and $\overline{\text{WRITE}}$ are both low the DAC selected is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to the data presented to the input port. The data is then latched when either $\overline{\text{ENABLE}}$ or $\overline{\text{WRITE}}$ are taken high.

| $\overline{\text{DAC A}}$/DAC B | $\overline{\text{CS}}$ | $\overline{\text{WR}}$ | DAC A | DAC B |
|---|---|---|---|---|
| L | L | L | WRITE | HOLD |
| H | L | L | HOLD | WRITE |
| X | H | X | HOLD | HOLD |
| X | X | H | HOLD | HOLD |

*Table 1 Logic truth table*

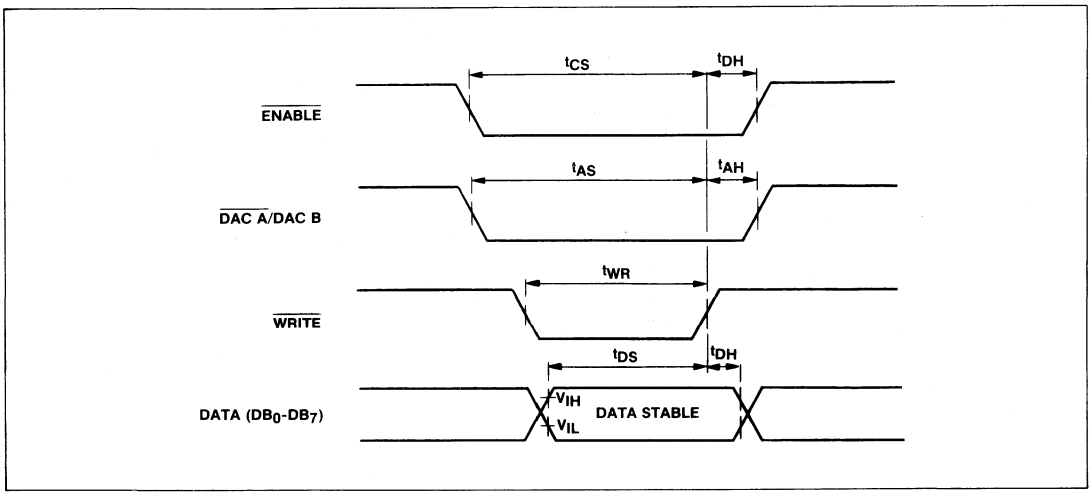



*Fig.6 Logic timing diagram*

## OPERATING NOTES

In some applications the standard 0 to $V_{REF}$ IN output voltage range and drive capability are not suitable, and other output ranges, both unipolar and bipolar are required.

To maintain flexibility two types of operational amplifier are illustrated; the industry standard 741 and a low cost pin-compatible alternative with a JFET input, the LF351. The LF351 features a high slew rate of 13V/$\mu$s, which gives a faster potential settling time than the 741. To keep drift to a minimum when using the 741, the external range setting resistors are calculated to match them to the 4kΩ ladder output impedance. This is not a consideration with the LF351, as the input offset current change with temperature is negligible for the impedances concerned. The resistor values for the LF351 were chosen to keep the output ringing to a minimum; a problem sometimes encountered with high slew rate op-amps. It is only the relative and not the absolute values of these resistors which set the range, and therefore can be changed as long as their ratios remain the same.

### Unipolar Operation

The general scheme for unipolar operation is shown in Fig.6 and is suitable for amplifiers with input bias currents less than 1.5$\mu$A.

The resulting full scale range is given by

$$V_{OUT}\,FS = 1 + \frac{R1}{R2}\,(V_{REF}\,IN - 1\,LSB)$$

$$= G\,(V_{REF}\,IN) - 1\,LSB)$$

The impedance at the inverting input is R1/R2 and for low drift with temperature (741 only), this parallel combination should be equal to the ladder resistance (4kΩ).

The required nominal values of R1 and R2 are therefore given by R1 = 4GkΩ and R2 = 4G/(G–1)kΩ.

Using these relationships a table of nominal resistance values for R1 and R2 can be constructed for $V_{REF}$ IN = 2.5V (Table 2). For gain setting R1 is adjusted about its nominal value. Practical circuit realisations for +5V and +10V output ranges are given in Figs. 8 and 9.

| Output range | G | R1 | R2 |
|---|---|---|---|
| +5V | 2 | 8kΩ | 8kΩ |
| +10V | 4 | 16kΩ | 5.33kΩ |

*Table 2 Nominal values for R1 and R2*

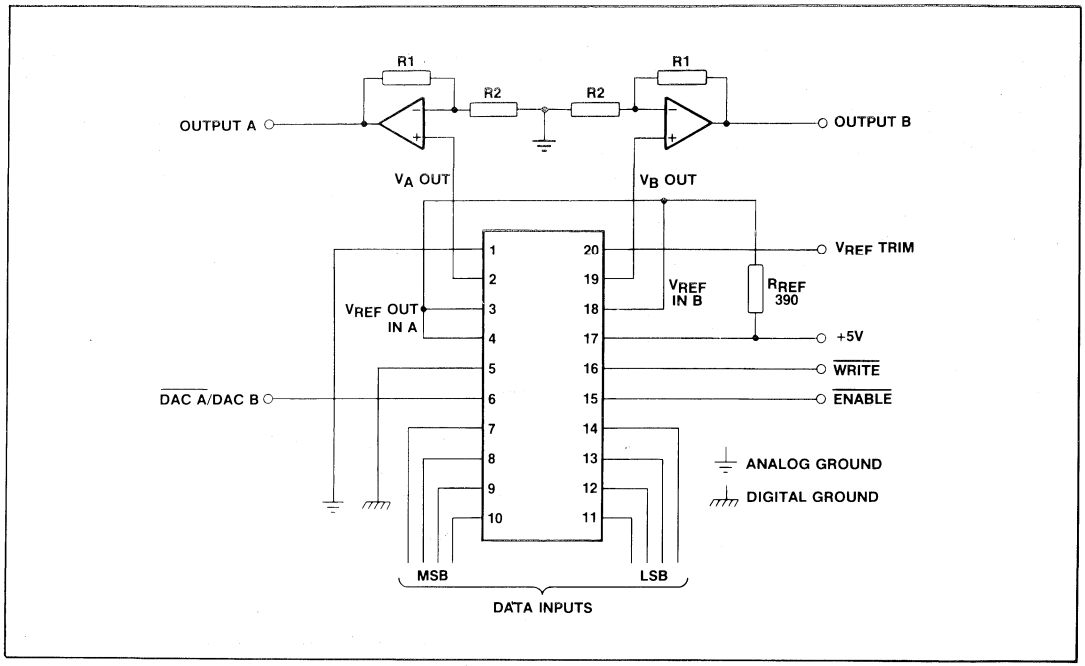



*Fig.7 Unipolar operation - basic circuit*

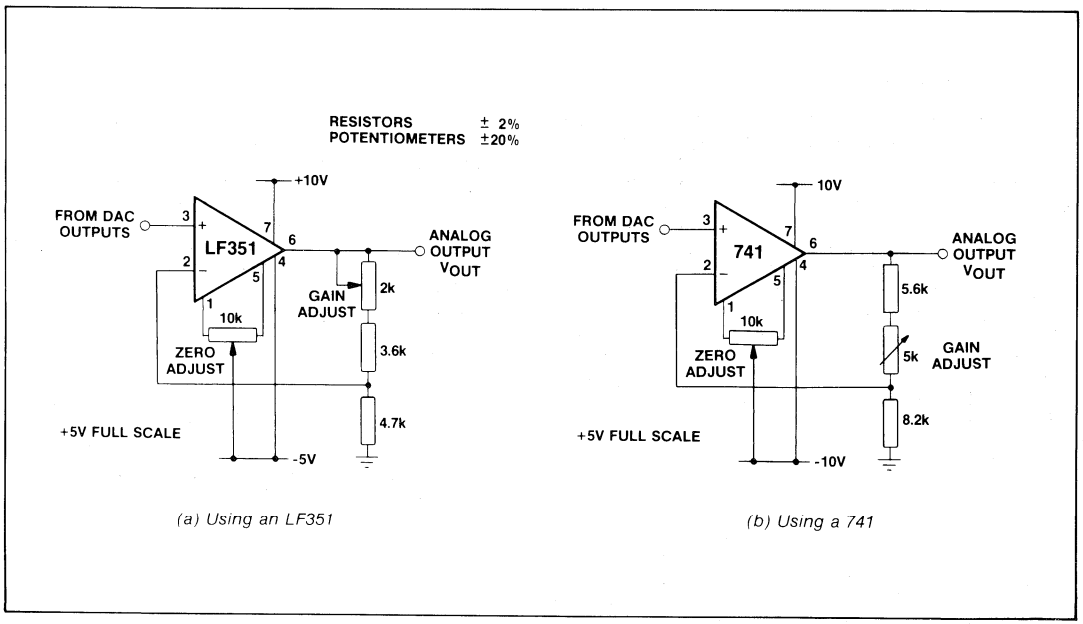
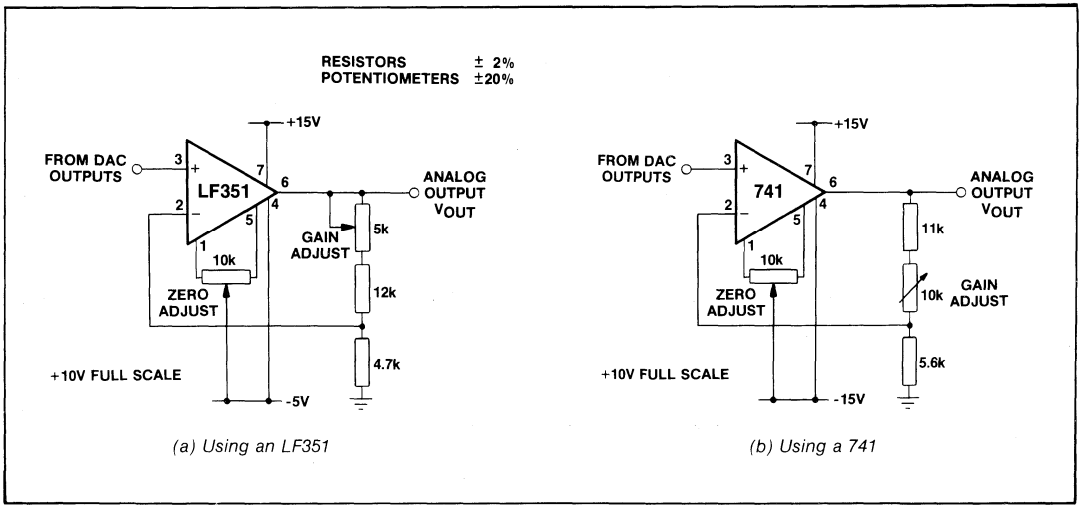



*Fig.8 +5V full scale unipolar operation - component values*




(a) Using an LF351 (b) Using a 741

*Fig.9 +10V full scale unipolar operation - component values*

## Unipolar Adjustment Procedure

1. Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust zero until $V_{OUT}$ = 0.0000V.

2. Set all bit ON (high) and adjust gain until $V_{OUT}$ = FS - 1 LSB.

| Output range, +FS | LSB | FS - 1 LSB |
|---|---|---|
| +5V | 19.5mV | 4.9805V |
| +10V | 39.1mV | 9.9609V |

$1\ LSB = \frac{FS}{256}$

*Table 3 Unipolar setting up points*

| Input code (Binary) | Analog output (nominal value) |
|---|---|
| 11111111 | FS - 1 LSB |
| 11111110 | FS - 2 LSB |
| 11000000 | ¾ FS |
| 10000001 | ½ FS + 1 LSB |
| 10000000 | ½ FS |
| 01111111 | ½ FS - 1 LSB |
| 01000000 | ¼ FS |
| 00000001 | 1 LSB |
| 00000000 | 0 |

*Table 4 Unipolar logic coding*

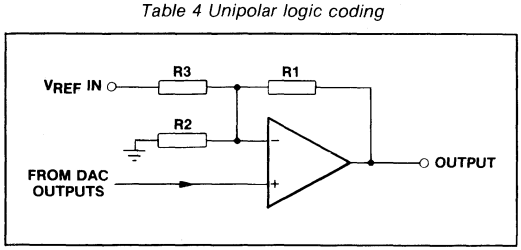



*Fig.10 Bipolar operation*

## Bipolar Operation

For bipolar operation the output from the ZN508 is offset by half full scale by connecting a resistor R3 between $V_{REF}$ IN and the inverting input of the buffer amplifier (Fig.10).

When the digital input to the ZN508 is zero the analog output is zero and the amplifier output should be - full scale. An input of all ones to the D-A will give a ZN508 output of $V_{REF}$ IN - 1 LSB and an amplifier output of + full scale. When using the 741, the parallel combination of R1, R2 and R3 should match the 4kΩ ladder resistance.

The nominal values of R1, R2 and R3 which meet these conditions are given by

R1 = 8GkΩ, R2 = 8G/(G-1)kΩ and R3 = 8kΩ,

where the resultant output range is ±G $V_{REF}$ IN.

A binary output range of ±$V_{REF}$ IN (which corresponds to the basic unipolar range 0 to $V_{REF}$ IN) is obtained if R1 = R3 = 8kΩ and R2 = ∞.

Assuming that $V_{REF}$ IN = 2.5V the nominal values of resistors for ±5V and ±10V output ranges are given in Table 5.

| Output range | G | R1 | R2 | R3 |
|---|---|---|---|---|
| +5V | 2 | 16kΩ | 16kΩ | 8kΩ |
| ±10V | 4 | 32kΩ | 10.66kΩ | 8kΩ |

*Table 5*

Minus full scale (offset) is set by adjusting R1 about its nominal value relative to R3. Plus full scale (gain) is set by adjusting R2 relative to R1.

Practical circuit realisations are given in Figs. 11 and 12. Note that in the ±5V case (741 only), R3 has been chosen as 7.5kΩ (instead of 8.2kΩ) to give a more symmetrical range of adjustment using standard potentiometers.

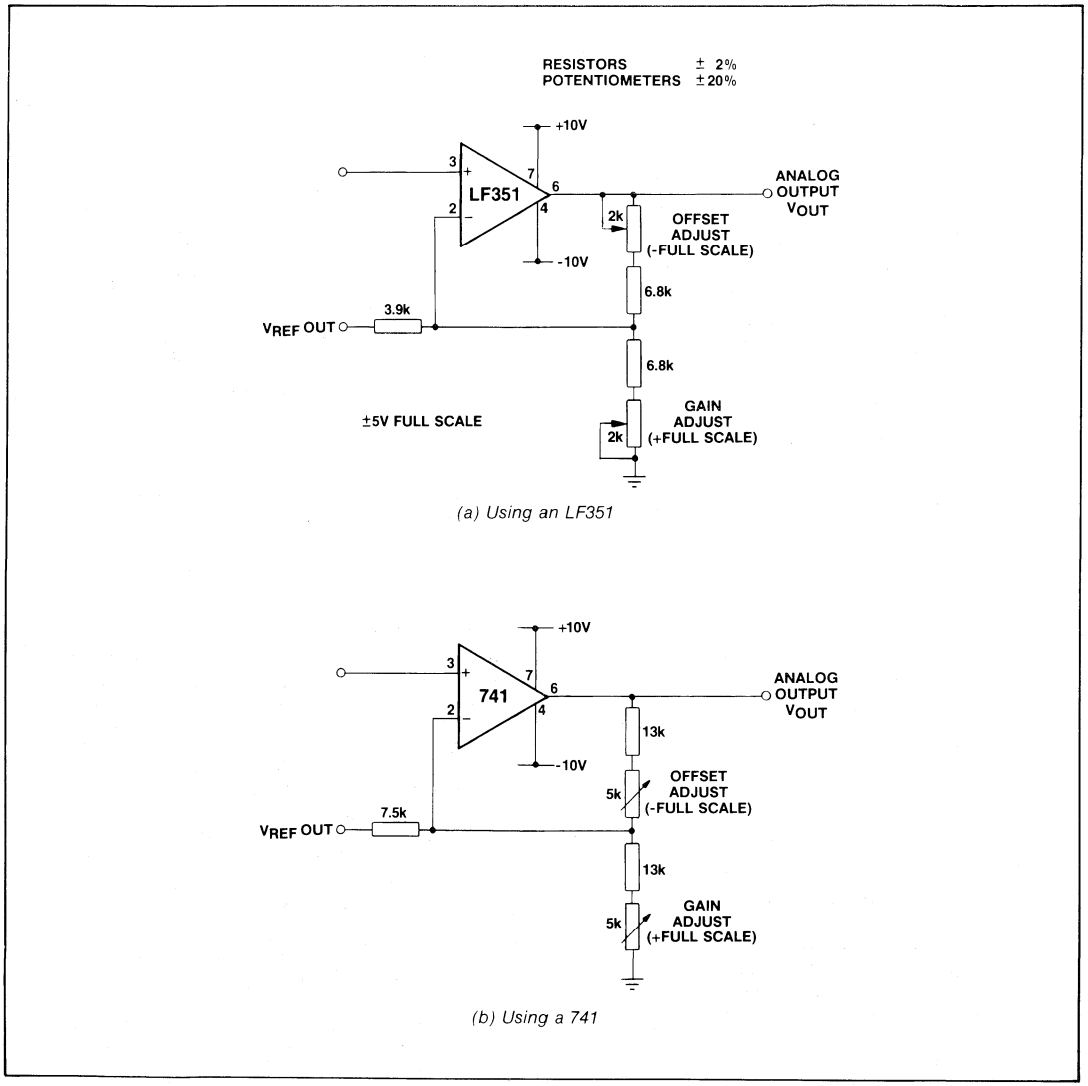



*Fig. 11 ±5V full scale bipolar operation - component values*

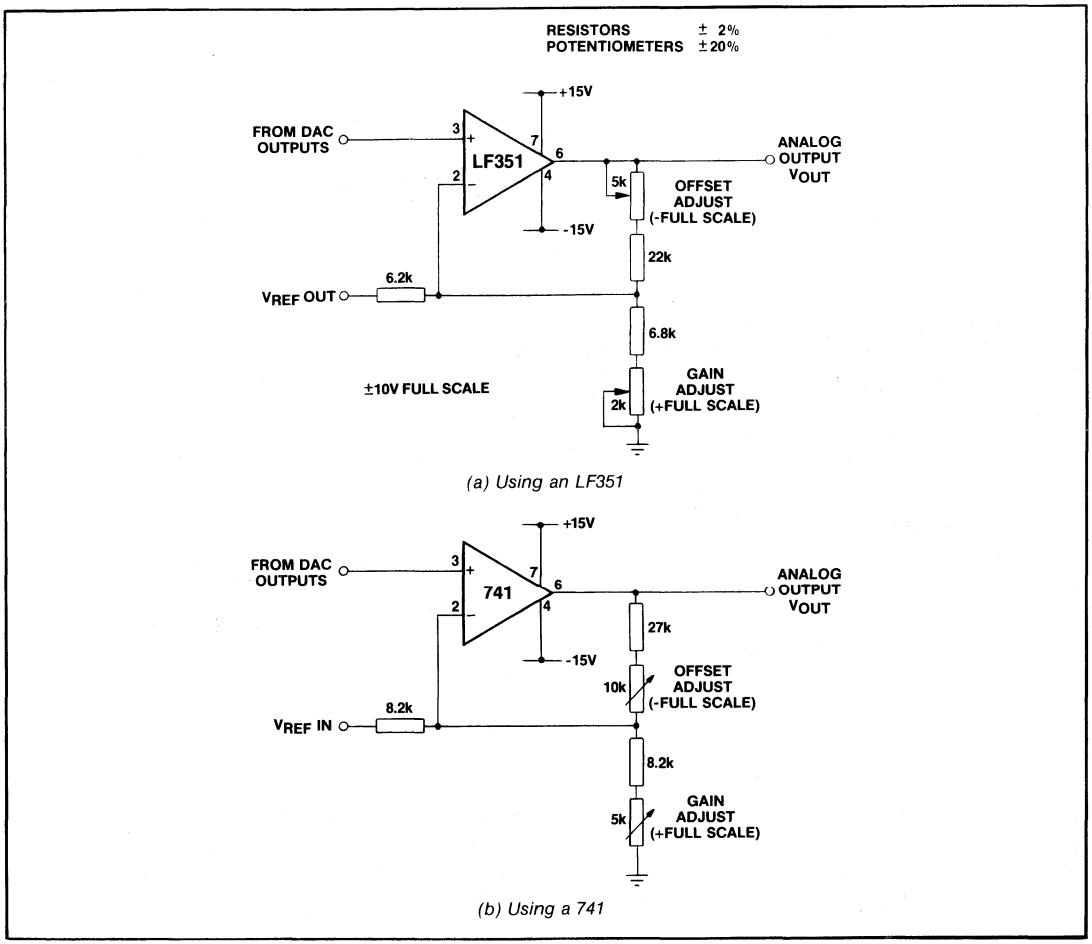



*Fig.12 ±10V full scale bipolar operation - component values*

## Bipolar Adjustment Procedure

1. Set all bits to OFF (low) with $\overline{\text{ENABLE}}$ low and adjust offset until the amplifier output reads - full scale.

2. Set all bits ON (high) and adjust gain until the amplifier output reads + (full scale - 1 LSB).

| Input range, ±FS | LSB | -FS | +(FS - 1 LSB) |
|---|---|---|---|
| ±5V | 39.1mV | -5.0000V | +4.9609V |
| ±10V | 78.1mV | -10.0000V | +9.9219V |

$$1\ \text{LSB} = \frac{2\text{FS}}{256}$$

*Table 6 Bipolar setting up points*

| Input code (offset binary) | Analog output (nominal value) |
|---|---|
| 11111111 | +(FS - 1 LSB) |
| 11111110 | +(FS - 2 LSB) |
| 11000000 | +½ FS |
| 10000001 | +1 LSB |
| 10000000 | 0 |
| 01111111 | -1 LSB |
| 01000000 | -½ FS |
| 00000001 | -(FS - 1 LSB) |
| 00000000 | -FS |

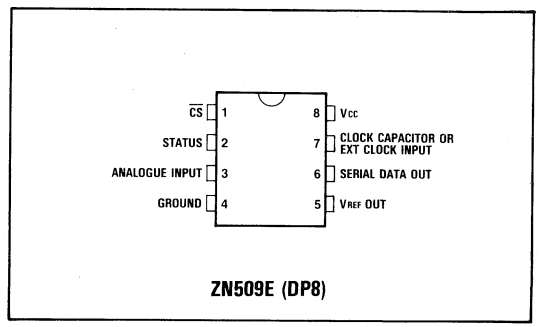
*Table 7 Bipolar logic coding*

3017-1.0

# ZN509E

## 8-BIT SERIAL A-D CONVERTER

The ZN509 is an 8-bit output, successive approximation A-D converter. Included on-chip is a clock generator which can be overdriven by an external clock, 2.5V bangap reference and 3-state output buffers. The device operates from a single +5V supply and is economically packaged in an8-pin plastic DIL. Chip select determines the start of conversion, the conversion mode (either continous or single-shot) and the 3-state control.




**Pin connections - top view**

### FEATURES

- ½ LSB Linearity
- 8 microseconds Conversion Time
- Serial Data Output - Suitable for Remote Operation
- Easy Microprocessor Interfacing
- Equally suitable for 'Stand-Alone' Applications
- Operates from a Single +5V Supply
- On-Chip Bandgap Reference
- TTL and CMOS Compatible
- Commercial Temperature Ranges

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | +7V |
| Max. voltage,logic and $V_{REF}$IN, $A_{IN}$ | $V_{CC}$–0.5V |
| Operating temperature range | 0°C to +70°C |
| Storage temperature range | –55°C to +125°C |

### ORDERING INFORMATION

| Device type | Linearity error(LSB) | Operating temperature | Package |
|---|---|---|---|
| ZN509E | ±0.5 | 0°C to +70°C | DP8 |

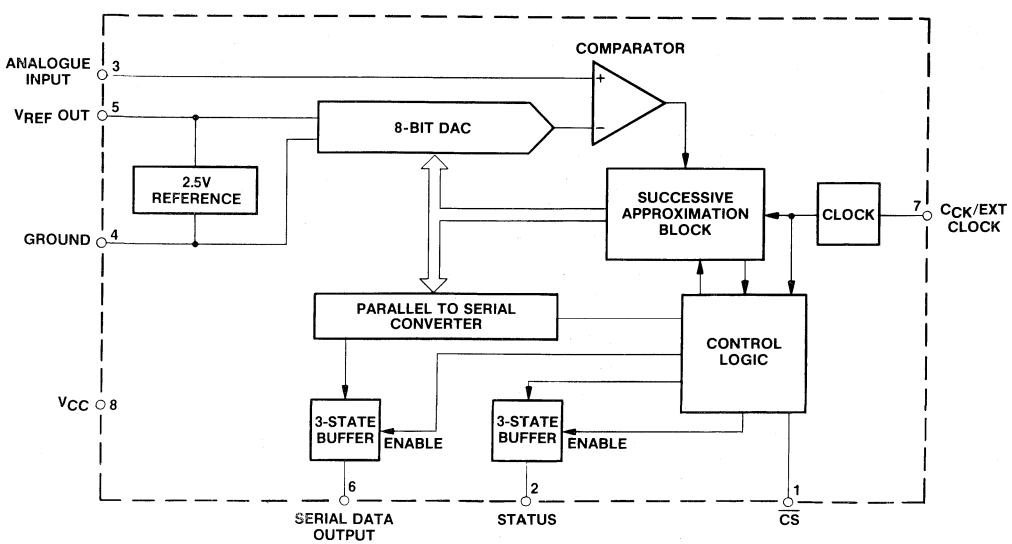



**Fig.1 Block diagram of ZN509**

**ELECTRICAL CHARACTERISTICS** (at $V_{CC} = 5V$, $T_{amb} = 25°C$ and $f_{CLK} = 1.0MHz$ unless otherwise specified).

| Parameter | $T_{amb} = +25°C$ | | | Over specified temp. range | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| Linearity error | – | – | ±0.5 | – | ±0.5 | LSB | |
| Differential linearity error | – | – | ±0.75 | – | ±0.75 | LSB | |
| Zero transition (00000000→00000001) | – | 15 | – | – | – | mV | |
| Full-scale transition (11111110→11111111) | – | 2.540 | – | – | – | V | |
| Linearity temperature coefficient | | | ±3 typ. | | | ppm/°C | |
| Differential linearity temperature coefficient | | | ±6typ. | | | ppm/°C | |
| Gain temperature coefficient | | | ±10 typ. | | | ppm/°C | |
| Offset temperature coefficient | | | ±7 typ. | | | ppm/°C | |
| Resolution | 8 | – | – | – | – | Bits | |
| Conversion time | 8 | – | – | – | – | μs | |
| Supply rejection | – | 0.2 | – | – | – | %/V | |
| Supply voltage | 4.5 | 5.0 | 5.5 | 4.5 | 5.5 | V | |
| Supply current | – | 29 | 40 | – | – | mA | |
| Power consumption | – | 145 | 200 | – | – | mW | |
| Ladder output impedance | – | 3 | – | – | – | kΩ | |
| **COMPARATOR** | | | | | | | |
| Analog input current | – | -230 | – | – | – | μA | |
| Analog input resistance | – | 13 | – | – | – | kΩ | |
| Analog input voltage | -0.5 | – | +3.5 | -0.5 | +3.5 | V | |

**ELECTRICAL CHARACTERISTICS** Cont.

| Parameter | $T_{amb} = +25°C$ | | | Over specified temp. range | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| **INTERNAL VOLTAGE REFERENCE** | | | | | | | |
| Output voltage | – | 2.535 | – | – | – | V | |
| Output voltage tolerance | – | – | ±3 | – | – | % | |
| Slope impedance | – | 0.75 | 2 | – | – | Ω | |
| Reference current | 0.75 | – | 5.2 | 0.75 | 5.2 | mA | |
| Output voltage temperature coefficient | – | 70 | – | – | – | ppm/°C | |
| **CLOCK** | | | | | | | |
| Maximum on-chip clock frequency | – | 1.0 | – | – | – | MHz | $C_{ck} = 220pF$ |
| Clock frequency tempco | – | –0.125 | – | – | – | %/°C | |
| Clock capacitor | 220 | – | – | – | – | pF | |
| Maximum external clock frequency | 1.0 | – | – | 1.0 | – | MHz | |
| Clock pulse width | 250 | – | – | – | – | ns | |
| High level I/P voltage $V_{IH}$ | 3.5 | – | – | 3.5 | – | V | |
| Low level I/P voltage $V_{IL}$ | – | – | 0.8 | – | 0.8 | V | |
| High level I/P current $I_{IH}$ | – | 850 | – | – | – | μA | $V_{CC} = 5.5V$ $V_{IN} = 4V$ |
| Low level I/P current $I_{IL}$ | – | –880 | – | – | – | | $V_{CC} = 5.5V$ $V_{IN} = 0.8V$ |
| Supply rejection | – | 3.0 | – | – | – | %/V | |
| **LOGIC $\overline{CS}$ INPUT** | | | | | | | |
| High level I/P voltage $V_{IH}$ | 2.4 | – | – | 2.4 | – | V | |
| Low level I/P voltage $V_{IL}$ | – | – | 0.8 | – | 0.8 | V | |
| High level I/P current $I_{IH}$ | – | 250 | – | – | – | μA | $V_{CC} = +5.5V$ $V_{IN} = +5.5V$ |
| High level I/P current $I_{IH}$ | – | 120 | – | – | – | μA | $V_{CC} = +5.5V$ $V_{IN} = +2.4V$ |
| Low level I/P current $I_{IL}$ | – | –350 | – | – | – | μA | $V_{CC} = +5.5V$ $V_{IN} = +0.4V$ |
| **DATA AND STATUS OUTPUTS** | | | | | | | |
| High level output voltage $V_{OH}$ | 2.4 | – | – | 2.4 | – | V | $I_{OH\ MAX}$ |
| Low level output voltage $V_{OL}$ | – | – | 0.4 | – | 0.4 | V | $I_{OL\ MAX}$ |
| High level output current $I_{OH}$ | – | – | –800 | – | – | μA | |
| Low level output current $I_{OL}$ | – | – | 2 | – | – | mA | |
| Three-state disable output leakage current | | | 2 | | 10 | μA | |

**ELECTRICAL CHARACTERISTICS** Cont.

| Parameter | $T_{amb}$ = +25°C | | | Over specified temp. range | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | Min. | Typ. | Max. | Min. | Max. | | |
| **CONTINUOUS CONVERSION** | | | | | | | |
| **Data output** | | | | | | | |
| Delay times $T_{EO}$ | – | 100 | 125 | – | 150 | ns | |
| $T_{CD}$ | – | 265 | 310 | – | 390 | ns | |
| **Status output** | | | | | | | |
| Delay times $T_{E1}$ | – | 250 | 300 | – | 430 | ns | |
| $T_{SO}$ | – | 165 | 210 | – | 260 | ns | |
| $T_{SI}$ | – | 220 | 270 | – | 370 | ns | |
| **SINGLE SHOT OPERATION** | | | | | | | |
| **Data output** | | | | | | | |
| Delay times $T_{EO}$ | – | 100 | 125 | – | 150 | ns | |
| $T_{DO}$ | – | 200 | 260 | – | 310 | ns | |
| $T_{DI}$ | – | 200 | 260 | – | 310 | ns | |
| $T_{CD}$ | – | 265 | 310 | – | 390 | ns | |
| **Status output** | | | | | | | |
| Delay times $T_{E1}$ | – | 250 | 300 | – | 430 | ns | |
| $T_{SO}$ | – | 220 | 270 | – | 300 | ns | |
| $T_{SI}$ | – | 230 | 280 | – | 320 | ns | |
| $T_{DSI}$ | – | 250 | 300 | – | 360 | ns | |

## GENERAL CIRCUIT OPERATION

The ZN509 uses the successive approximation technique to produce an 8-bit serial digital output. At the beginning of the conversion sequence the DAC input is set to the MSB. The resulting analog output is compared with the unknown analog input signal by means of the comparator. If the analogue input is larger the MSB is left in circuit, if not the MSB is removed. On the second clock pulse this sequence is repeated for the next most significant bit and so on until all 8-bits have been compared.

## CONVERSION TIMING

The ZN509 will accept a low going chip select ($\overline{CS}$) pulse, which can be completely asynchronous with respect to the clock; this pulse enables the 3-state output buffers and starts the conversion. Valid serial data will be produced between one and two clock periods later depending on the relative timing of the clock and $\overline{CS}$ signals (see Fig. 3 & 4).

Upon receipt of a low going $\overline{CS}$ pulse the ZN509 is cleared i.e. the MSB and STATUS are set to one and all other bits reset to zero. The $\overline{CS}$ pulse can be as short as 150ns and if pulsed low during a conversion the device will be cleared and the conversion will restart. Holding the $\overline{CS}$ input low will not inhibit the operation of the device.

The STATUS produces two different types of output which is dependent upon whether the device is being operated in the single shot or continuous mode.

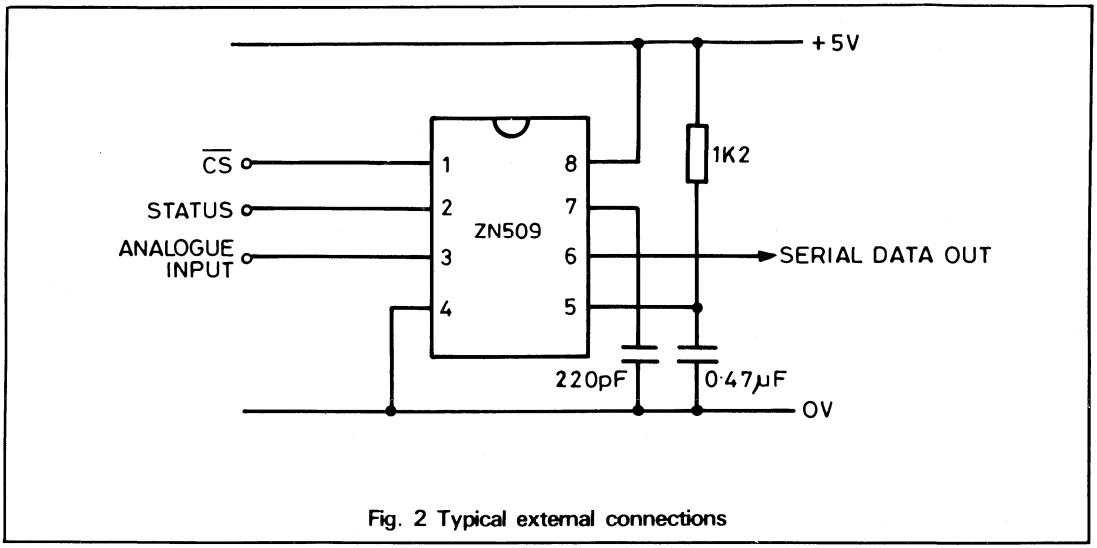



Fig. 2 Typical external connections

## CONTINUOUS MODE OF OPERATION

The ZN509 can be made to cycle by simply tying the $\overline{CS}$ input low see Fig. 3 for timing diagram. It should be noted that after power up, valid data will only be available after the voltage reference has stabilised. This time is dependent upon the reference decoupling capacitor and load resistor, but is typically 2ms for a 1K6 resistor and a 0.47μF capacitor.

The synchronising status output goes low for one clock period every eight clock periods and coincides with the MSB data output.

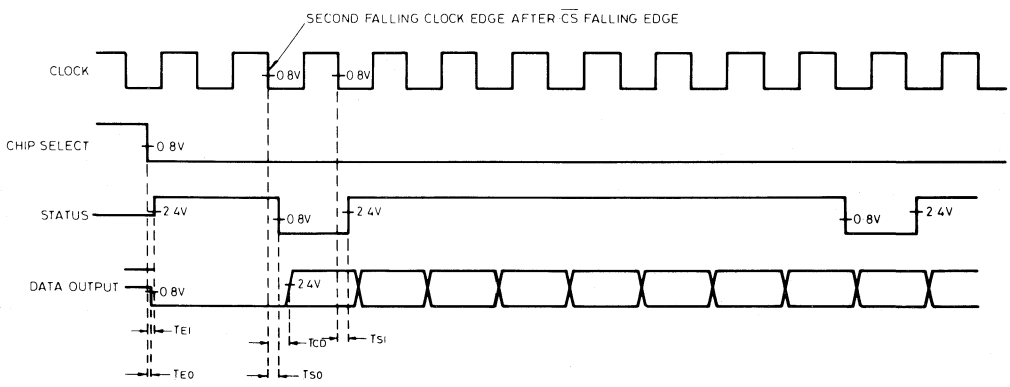



Fig. 3 Continuous (cycling) operation

## SINGLE SHOT OPERATION

The ZN509 recognises that a single shot operation is to be performed if a $\overline{CS}$ pulse of greater than 150ns, but no longer than one clock period in length is applied. Once this pulse is applied, both the Status and Data outputs come out of 3-state, the Status going high and the data output low. Between one and two clock periods later valid data, MSB first, will appear on the data output (the status goes low to indicate when the valid data is available). When all 8 bits of data have appeared, the data output returns into a high impedance state, at which point the status goes high. One clock period later the Status output also returns to a high impedance state.

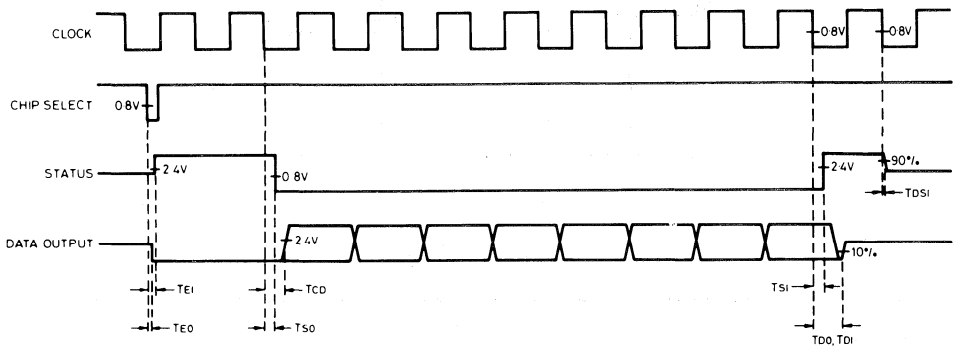



Fig. 4 Single shot operation

## DIGITAL OUTPUTS

The digital outputs are provided with 3-state buffers to allow connection to a common data bus. An equivalent circuit is shown in Fig. 5. When disabled (see timing diagrams for the conditions under which this applies) both output transistors are turned off and the device presents a high impedance load to the bus. When enabled the outputs will assume the logic states present on the input to the buffer.

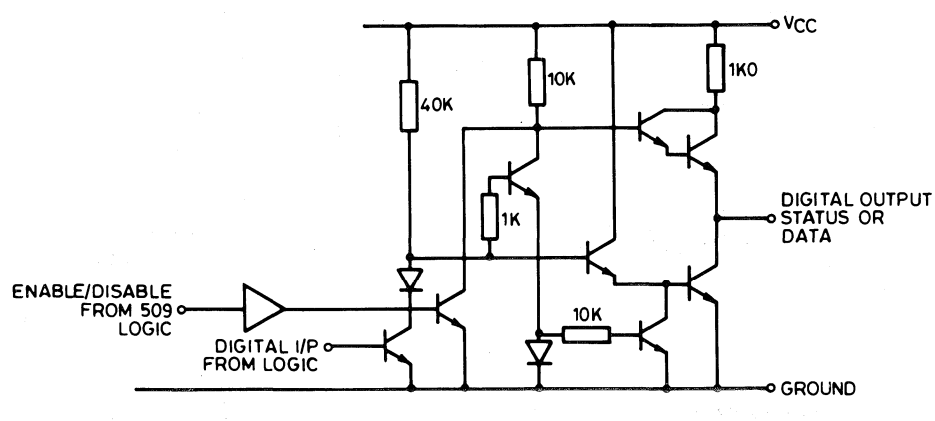



Fig. 5 Digital outputs

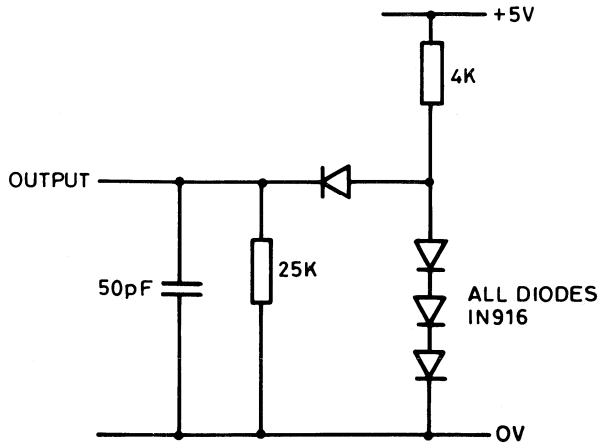



Fig. 6 Output load circuit

## ON – CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between pin 7 and ground as shown in Fig. 7(a). A graph of typical oscillator frequency versus capacitance is given in Fig. 8a. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor, as shown in Fig. 7(b). A graph of typical oscillator frequency versus resistance and capacitance is given in Fig. 8b. The oscillator input may be overdriven with an external clock signal from a TTL or CMOS gate as shown in Fig. 7(c).

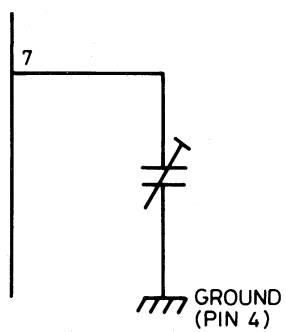



Fig. 7(a) Fixed/variable capacitor

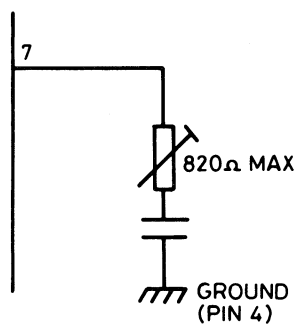



Fig. 7(b) Fixed capacitor and variable resistor

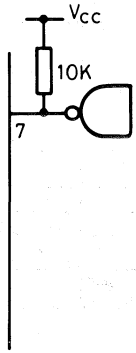



Fig. 7(c) External TTL or CMOS drive

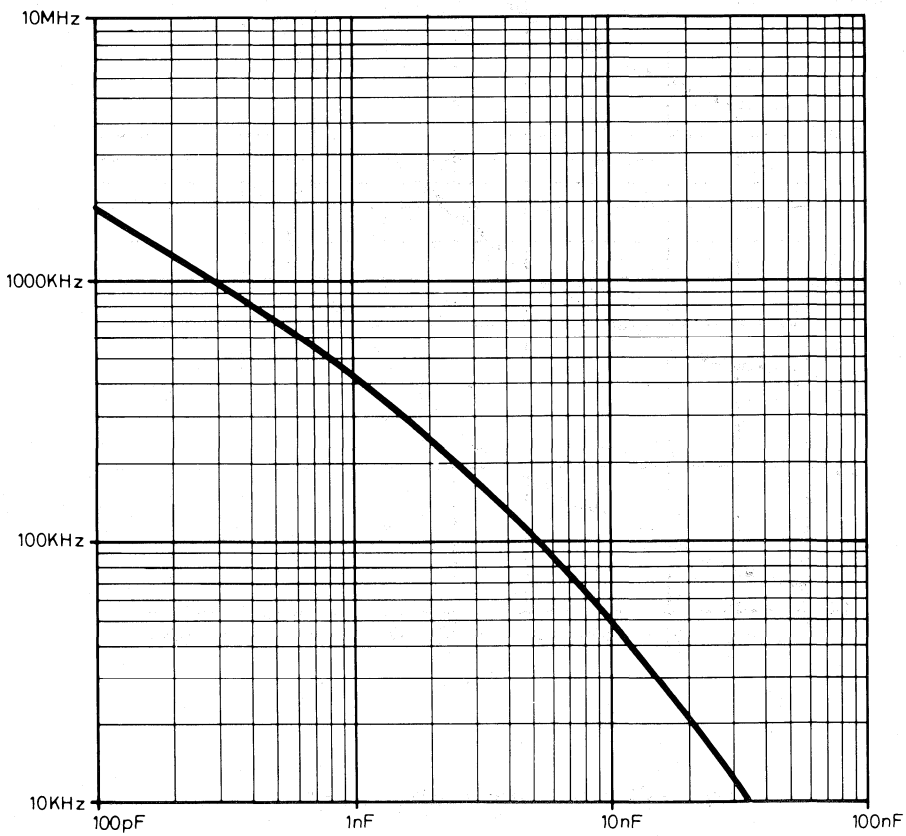



Fig. 8a Clock frequency v capacitance

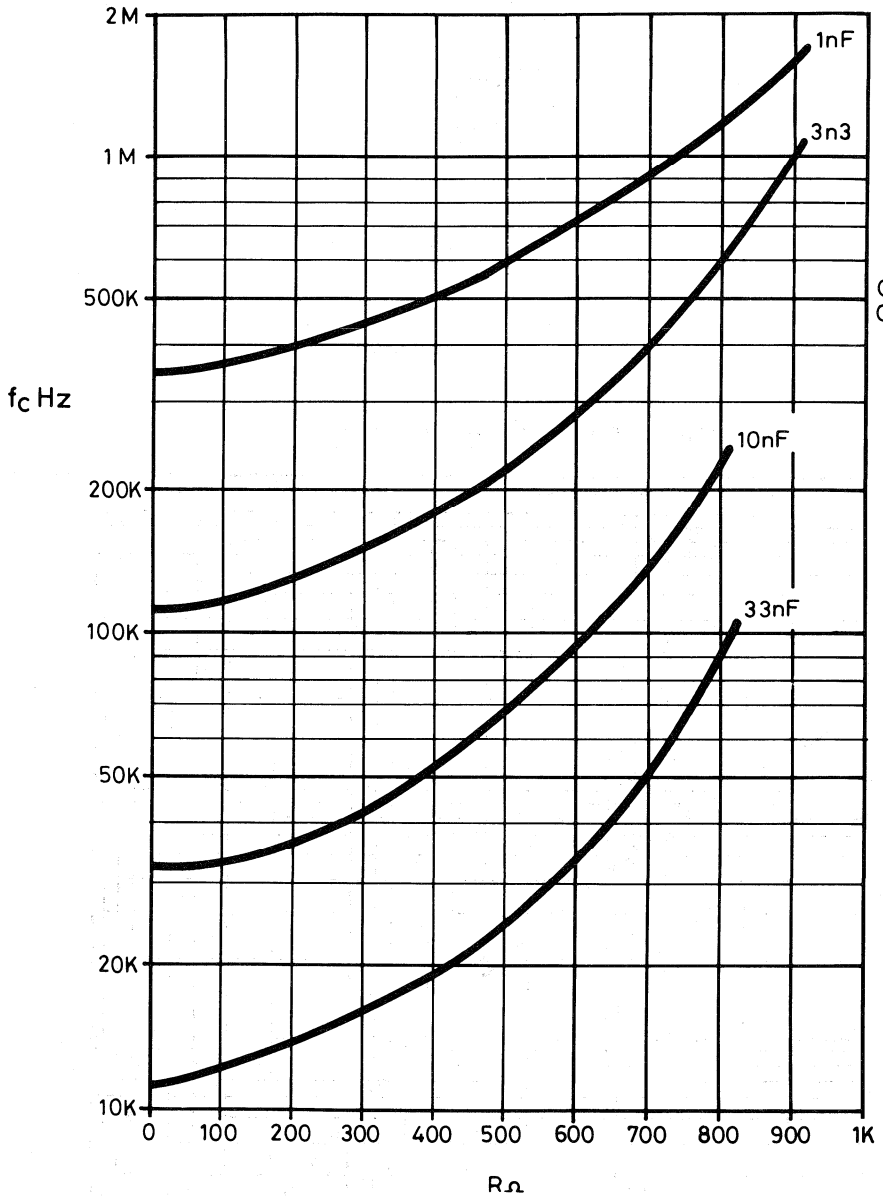



Fig. 8b Clock frequency v resistance and capacitance

## ANALOGUE CIRCUITS

### Reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 9). A resistor ($R_{ref}$) should be connected between $V_{CC}$ and $V_{REF\ OUT}$, and a decoupling capacitor, $C_{REF}$ (0.47$\mu$F), is required between $V_{REF\ OUT}$ and GND.

A suitable current to drive a ZN509 is nominally 2mA and will be supplied by an $R_{REF}$ of 1K2 [(5-2.535)/1K2 $\simeq$ 2mA].

With $R_{REF} = 620\Omega$, the ZN509 reference may also be used as the reference voltage for other external circuits and can source or sink up to 1.5mA.

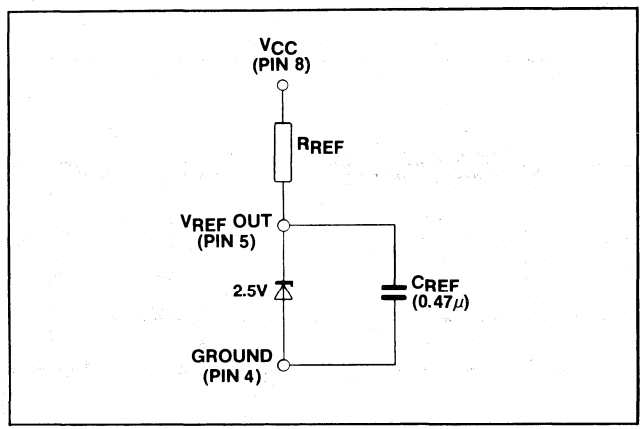



Fig. 9 Internal voltage reference

### Analogue input

The equivalent analogue input is shown in Fig. 10.

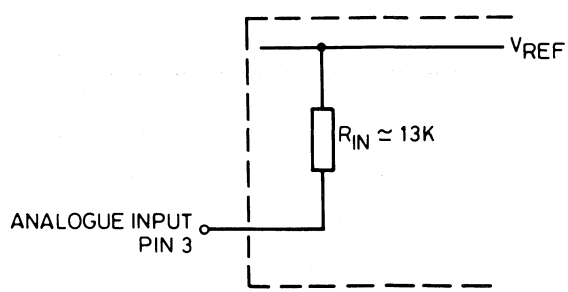



Fig. 10

## D – A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 11. Each element is connected to either 0V or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1mV).

A binary weighted voltage is produced at the output of the R-2R ladder.

$$D-A\ output = \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$$

Where n is the digital input to the D – A from the successive approximation register.

$V_{OS}$ is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (7ppm/°C) the effect on accuracy will be negligible.

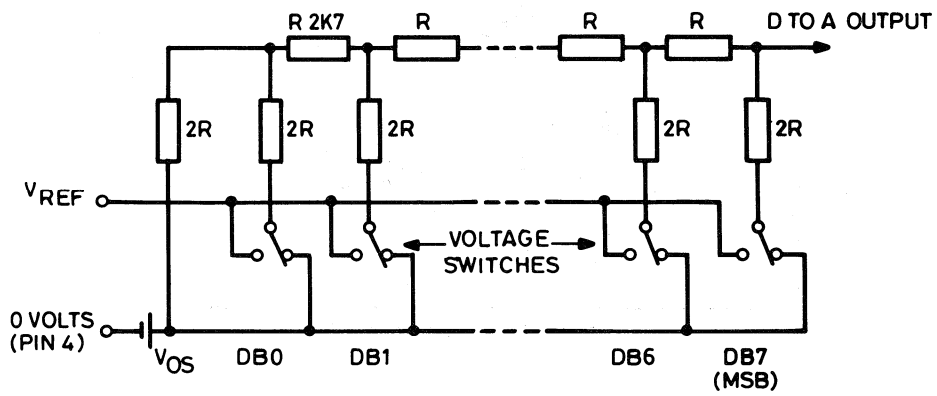



**Fig. 11 R-2R ladder network**

# ZN515

## 8-BIT 100MHz VIDEO D-A CONVERTER

The ZN515 is a monolithic video digital-to-analog converter of accepting 8 bits of ECL compatible data at update rates as high as 100MHz and converting this information to give 1 of 256 levels of grey scale. Output glitches are minimised by careful design of the switch decoding circuits and the provision of on-chip data latches.

The ZN515 incorporates complete composite video controls including sync, blanking, 10%bright and reference white and produces a composite video output to drive directly a doubly terminated 75Ω transmission line.

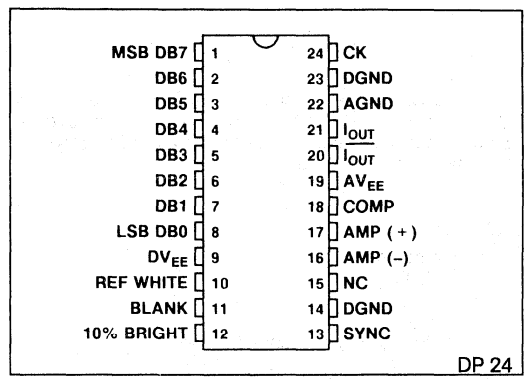



*Fig.1 Pin connections - top view*

### FEATURES

- 100MHz Update Rate
- ±0.5 LSB Linearity Error
- ±0.5 LSB Differential Linearity Error
- Low Glitch Energy
- RS-343A Compatible Levels
- Drives Doubly-Terminated 75Ω Load
- ECL Compatible Inputs

### APPLICATIONS

- High Resolution Colour Graphics
- CAE/CAD/CAM Applications
- Image Processing
- Video Reconstruction
- Instrumentation

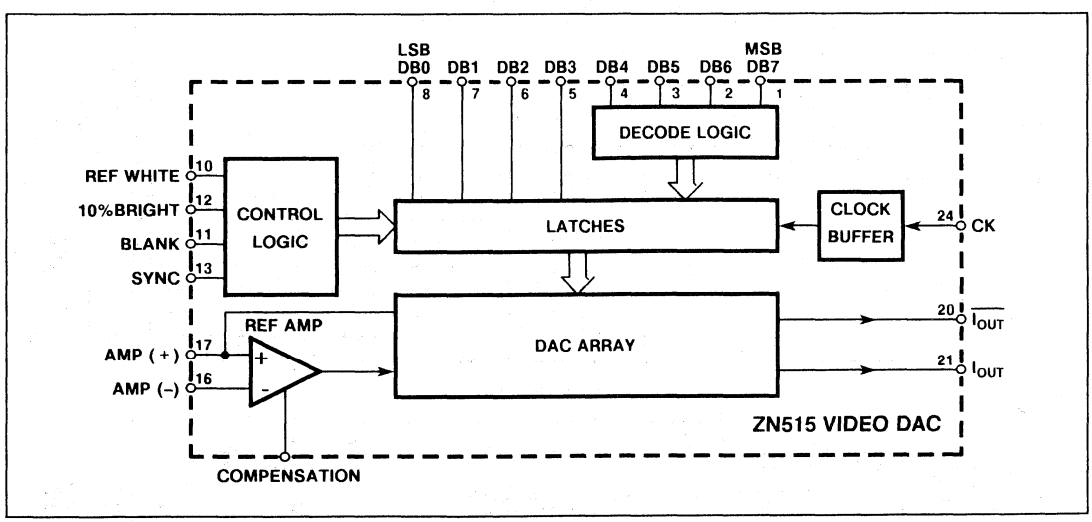


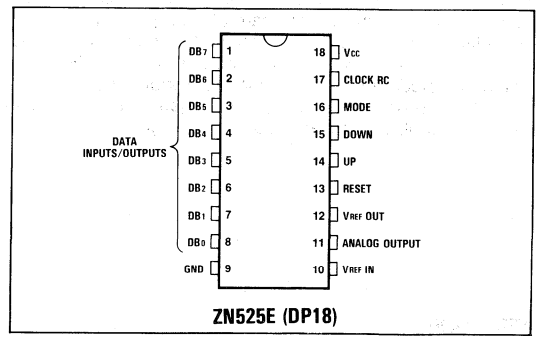

*Fig.2 Pin connections - top view*

3024-1.0

# ZN525

## 8-BIT MULTIFUNCTION DATA CONVERTER

The ZN525 is a versatile, multifunction 8-bit data conversion system. A voltage-output DAC, 8-bit up/down counter, stable 2.5V bandgap reference and clock generator are contained on a single chip.




*Pin connections (top view)*

### FEATURES

- Multimode Device Operates As:
  - DAC
  - ADC
  - Tracking ADC
  - Voltage to Frequency Converter
  - Ramp and Sawtooth Generator
  - Non-linear Waveform Generator
  - Voltage-Controlled Oscillator
  - Track-and-Hold Circuit
- 8-Bit Accuracy
- 800ns DAC Settling Time
- On-Chip Up/Down Counter
- On-Chip Clock
- On-Chip Voltage Reference
- Single +5V Supply
- Commercial or Military Temperature Range

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| ZN525E | 0°C to +70°C | DP18 |

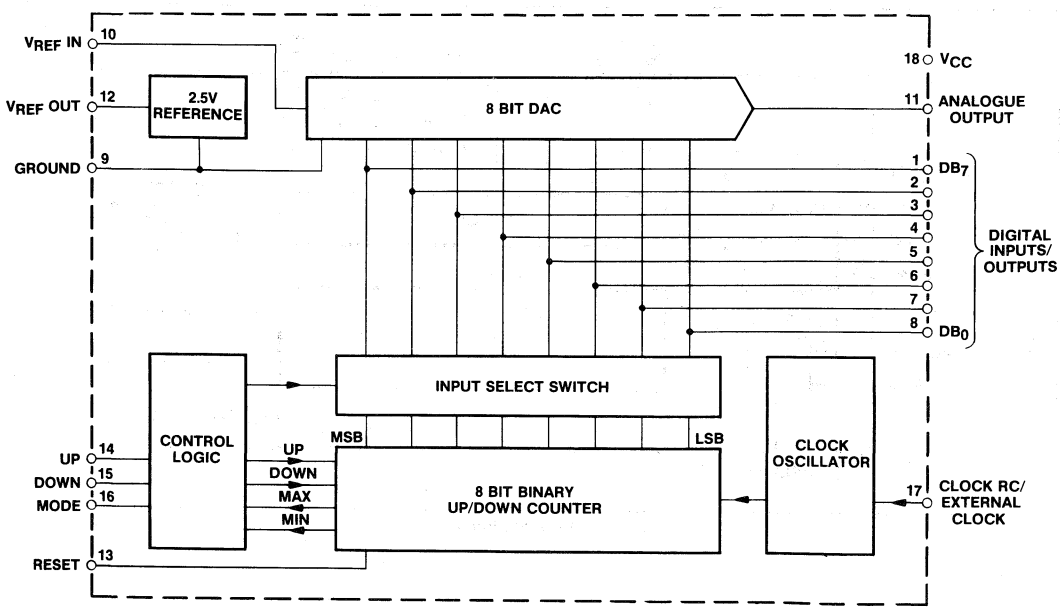



*Fig.1 System diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_{CC}$ = +5V, $V_{REF}$ = 1.5V - 3.0V, $T_{amb}$ = +25°C

| Characteristic | Value | | | Units | Conditions |
|---|---|---|---|---|---|
| | Min. | Typ. | Max. | | |
| **D to A Converter** | | | | | |
| Resolution | 8 | - | - | Bits | |
| Linearity error | - | ±0.25 | ±0.5 | LSB | $T_{min}$, $T_{amb}$, $T_{max}$ |
| Differential linearity error | ±0.25 | | ±1 | LSB | $T_{min}$, $T_{amb}$, $T_{max}$ |
| Zero error | - | 5.0 | 10.0 | mV | ZN525E All bits OFF |
| Settling time to 0.5 LSB | - | 500 | - | ns | All bits OFF to ON |
| | - | 800 | - | ns | or vise versa |
| Full-scale output | 2.545 | 2.550 | 2.555 | V | All bits ON $V_{REF}$ = 2.56V |
| Output resistance | - | 4 | - | kΩ | |
| Full-scale temperature coefficient | - | 4 | - | ppm/°C | Ext. $V_{REF}$ = 2.56V |
| Reference voltage | 0 | - | 3 | V | |
| **On-chip voltage reference** | | | | | |
| Output voltage | 2.4 | 2.59 | 2.7 | V | $R_{REF}$ = 390Ω |
| Slope resistance | - | 2 | 4 | Ω | $C_{REF}$ = 220nF |
| Temperature coefficient of $V_{REF}$ | - | 50 | - | ppm/°C | |
| Reference current | 4 | - | 15 | mA | |
| **Counter (with external clock)** | | | | | |
| High level threshold voltage $V_{T+}$ | - | - | 2.3 | V | |
| Low level threshold voltage $V_{T-}$ | 1.7 | - | - | V | |
| Maximum clock frequency | 1 | - | - | MHz | Note 1 |
| **On-chip clock** | | | | | |
| Maximum frequency | 500 | - | - | kHz | |
| Clock frequency tempco | - | 100 | - | ppm/°C | |
| Clock resistor | 3.3 | - | 100 | kΩ | |
| Clock capacitor | 100 | - | - | pF | |
| High level threshold voltage $V_{T+}$ | - | 4.6 | - | V | |
| Low level threshold voltage $V_{T-}$ | - | 1.5 | - | V | |
| Supply rejection | - | 0.8 | - | %/V | |
| **Logic circuits** | | | | | |
| **Bit Inputs** | | | | | |
| High level input voltage $V_{IH}$ | 2.0 | - | - | V | |
| Low level input voltge $V_{IL}$ | - | - | 0.8 | V | |
| High level input current $I_{IH}$ | - | - | -180 | μA | $V_{IN}$ = 2.4V |
| Low level input current $I_{IL}$ | - | - | -400 | μA | $V_{IN}$ = 0.4V |
| **Bit Outputs** | | | | | |
| High level output voltage $V_{OH}$ | - | 5.0 | - | | No load |
| Low level output voltage $V_{OL}$ | - | 0.1 | - | | No load |
| High level output voltage $V_{OH}$ | 2.4 | - | - | V | $I_{OH}$ = -40μA |
| Low level output voltage $V_{OL}$ | - | - | 0.4 | V | $I_{OL}$ = 2.5mA |
| **Control inputs** | | | | | |
| High level input voltage $V_{IH}$ | 2 | - | - | V | |
| Low level input voltage $V_{IL}$ | - | - | 0.8 | V | |
| High level input current $I_{IH}$ | - | - | -25 | μA | $V_{IN}$ = 2.4V |
| Low level input current $I_{IL}$ | - | - | -95 | μA | $V_{IN}$ = 0.4V |
| Reset pulse width | 200 | - | - | ns | |
| **Power supply** | | | | | |
| Supply voltage | 4.5 | 5 | 5.5 | V | |
| Supply current | - | 39 | 47 | mA | $V_{CC}$ = 5.5V |

NOTES 1. Speeds of up to 1.7MHz may be obtained by reducing the mark space ratio of the clock.

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | +7V |
| Max. voltage, logic and $V_{REF}$ inputs | $V_{CC}$ |
| Operating temperature range | 0°C to +70°C |
| Storage temperature range | -55°C to +125°C |

## GENERAL CIRCUIT OPERATION

The ZN525 incorporates an 8-bit DAC based on a voltage switching R-2R ladder network. The reference voltage for this ladder may be derived from the on-chip precision bandgap reference, or an external reference voltage may be supplied.

The ZN525 also contains an 8-bit up/down counter and control logic. The DAC may receive its digital input data from the counter, the counter outputs being simultaneously available at an 8-bit I/O port. Alternatively the counter outputs may be inhibited and the I/O port used to feed data direct to the DAC inputs.

An on-chip oscillator is provided to drive the clock input of the up/down counter. The on-chip clock may be overridden by an external clock signal.

## UP/DOWN COUNTER AND CONTROL LOGIC

The counter is a high-speed, synchronous up/down type, whose operation is determined by four control pins. The functions of the UP, DOWN and RESET inputs are fairly self explanatory, the MODE input determines the behaviour of the counter at zero and full-scale. When the MODE input is high the counter will reset to zero if it is clocked past full-scale in the UP direction and will reset to 255 if it is clocked past zero in the DOWN direction. When the MODE input is low the counter will stop on reaching full-scale or zero.

The normally invalid state of UP and DOWN inputs low simultaneously is also utilised in the ZN525. With the MODE input high and UP and DOWN inputs low the counter will cycle up and down continously, reversing at full-scale and zero. With all three control inputs low the counter outputs are disabled and the DAC inputs accessible from the I/O port.

A truth table for the control inputs is given in Table 1.

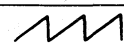
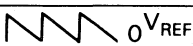
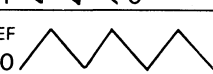
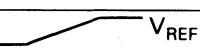
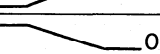
| Reset | Mode | Down | Up | Digital function | Analogue waveform |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | Counter stopped. |  |
| 1 | 1 | 1 | 0 | Count up continuously. |  |
| 1 | 1 | 0 | 1 | Count down continuously. |   |
| 1 | 1 | 0 | 0 | Count up, reverse at F.S., count down, reverse at zero. |   |
| 1 | 0 | 1 | 1 | Counter stopped. |  |
| 1 | 0 | 1 | 0 | Count up, stop at F.S. |   |
| 1 | 0 | 0 | 1 | Count down, stop at zero. |   |
| X | 0 | 0 | 0 | DAC mode, counter output disabled. Counter can still be reset by taking reset input low. |  |
| 0 | X | X | X | Counter reset. Does not affect analogue output in DAC mode. |  |

*Table 1*

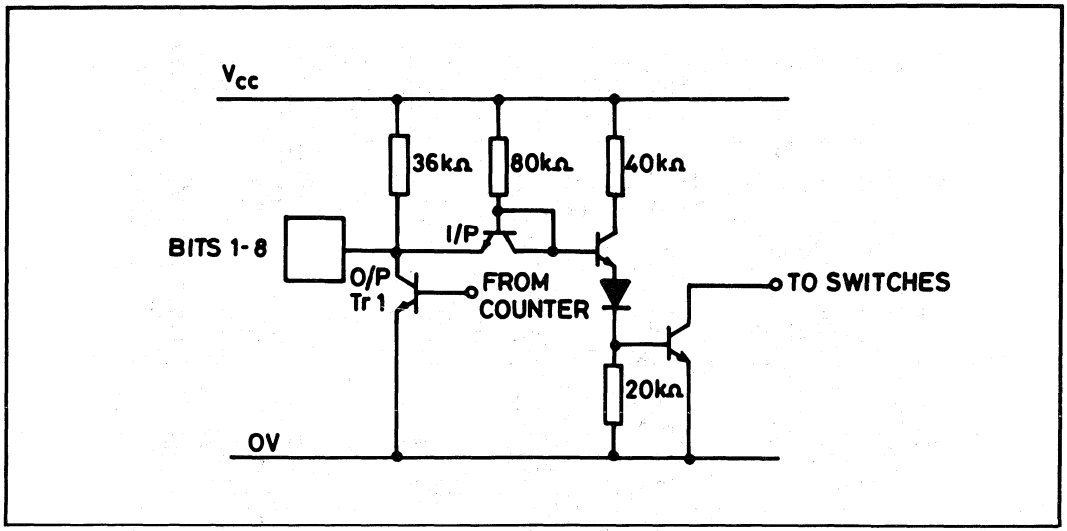



*Fig.2 Bit inputs/outputs*

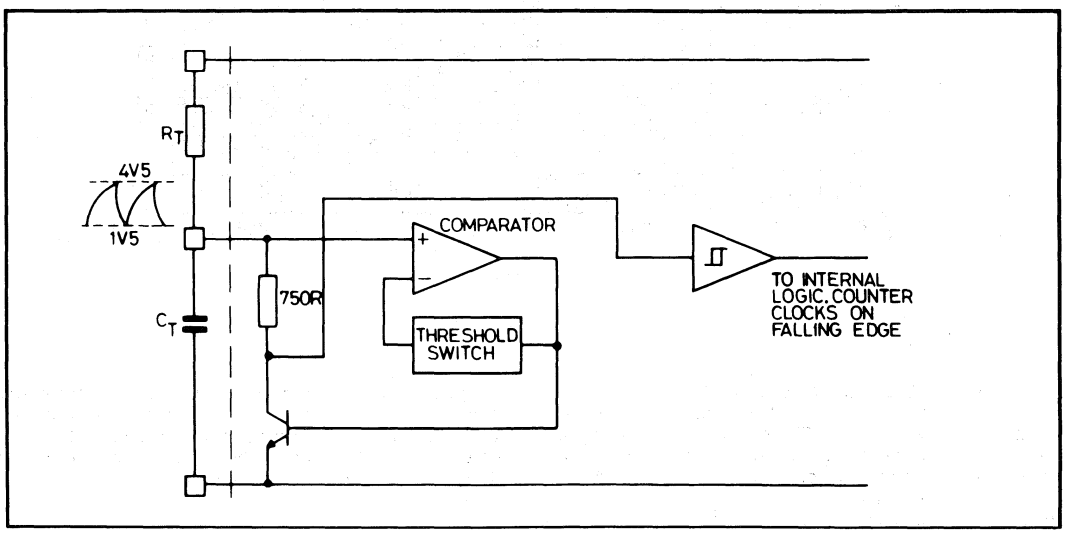



*Fig.3*

## DATA PORT

One bit of the data port is shown in Fig.2. The input/output pin is the junction of the counter output buffer and the dAC input buffer.

Normally the DAC is driven from the counter and the counter data is also available at the port. However, when the counter outputs are disabled the output transistors are turned off and the DAC inputs may be accessed from the data port.

The data port can drive or be driven from B-series CMOS and all TTL families.

## CLOCK CIRCUIT

The on-chip clock circuit of the ZN525 is shown in Fig.3. The frequency of the clock is given by

$$f_{CLK} \triangleq \frac{1}{2R_T C_C} \text{ (Hz, Ω, F)}$$

Typical graphs of oscillator frequency versus resistor and capacitor values are given in Fig.4.

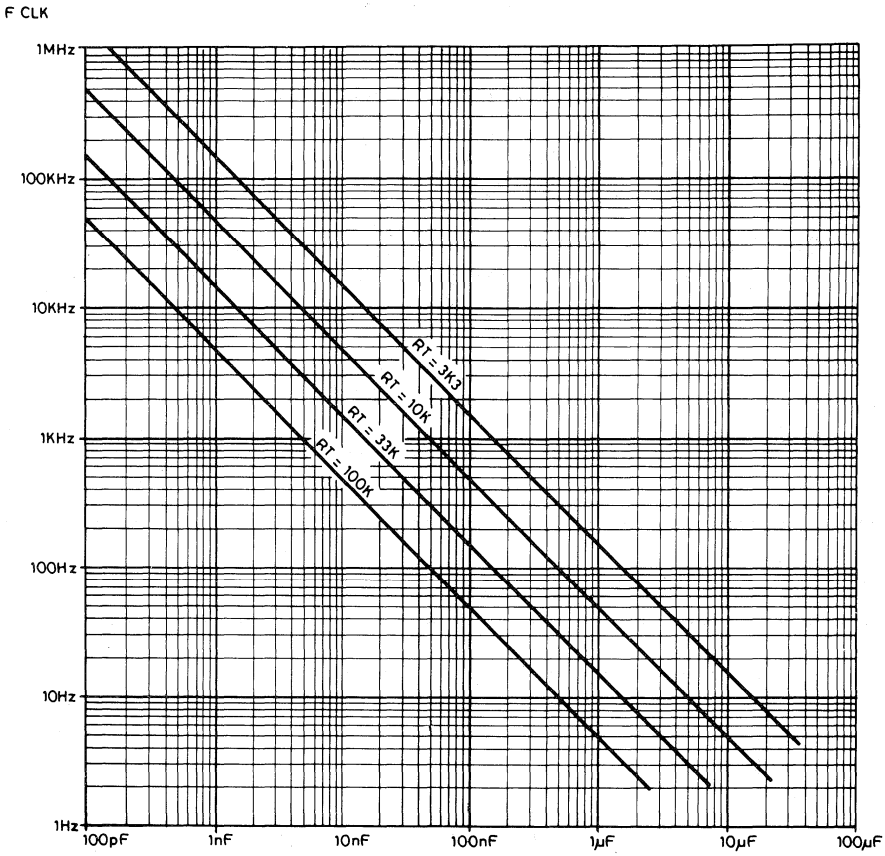



*Fig.4*

The external capacitor $C_T$ is charged via the external resistor $R_T$ to the upper threshold of the comparator (about +4.5V with $V_{CC}$ = +5V). The comparator turns on the discharge transistor to discharge $C_T$ and switches its threshold to the lower value of about 1.5V. When the voltage on $C_T$ has fallen to this level the comparator turns off the discharge transistor and the cycle repeats.

The clock can be overdriven from either a TTL totem-pole output (Fig.5(a)), an open collector output (Fig.5(b)), or a CMOS gate (Fig.5(c)). In all three cases the $V_{OH}$ of the driving gate must be attenuated to below 4V so that the internal discharge transistor is not turned on.

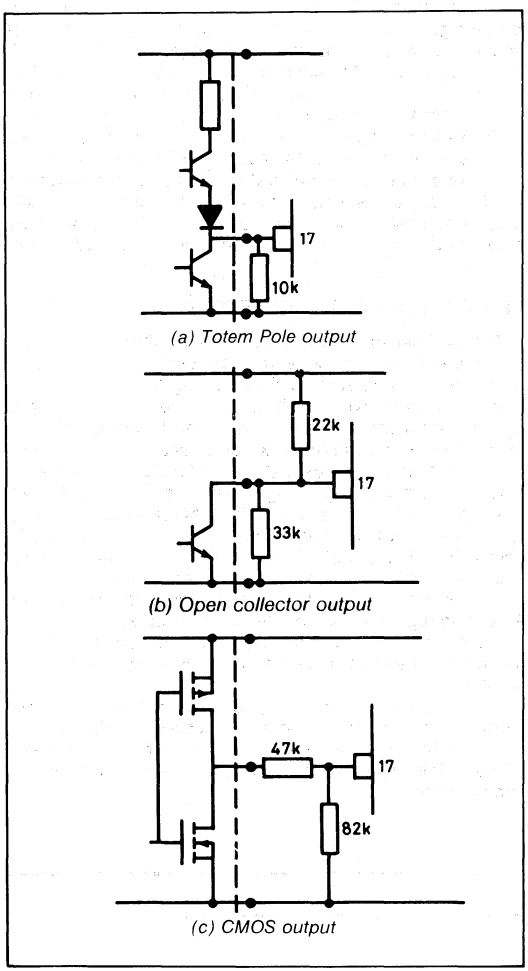



*Fig.5 Overdriving the clock input*

## ANALOG CIRCUITS

### D to A Converters

The DAC is of the voltage switching type and uses an R-2R ladder network as shown in Fig.6.

Each 2R element is connected to either 0V or $V_{REF}$ IN by transistor voltage switches specially designed for low offset voltage (<1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder.

$$V_{OUT} = \frac{n}{256} (V_{REF}\ IN - V_{OS}) + V_{OS}$$

where n is the digital input from the counter or data port.

$V_{OS}$ is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. The value of $V_{OS}$ is typically 5mV for the device in any package. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is small the zero drift will be small. The DAC output range can be considered to be 0V to $V_{REF}$ IN with an output resistance R (4kΩ).

## REFERENCE

### On-Chip Reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V zener diode with a very low slope impedance (Fig.7).

An external resistor ($R_{REF}$) should be connected between pins 12 and 18 to bias up the on-chip reference, whilst a stabilising/decoupling capacitor ($C_{REF}$) is required between pins 12 and 9.

To use the internal reference $V_{REF}$ OUT (pin 12) is connected to $V_{REF}$ IN (pin 10).

The recommended reference resistor of 390Ω will supply a nominal reference current of 6.4mA which is sufficient to drive the reference inputs of up to five ZN525s. Where several ZN525s are used in a system this useful feature can save up to four resistors and capacitors as well as reducing power consumption and giving excellent gain tracking.

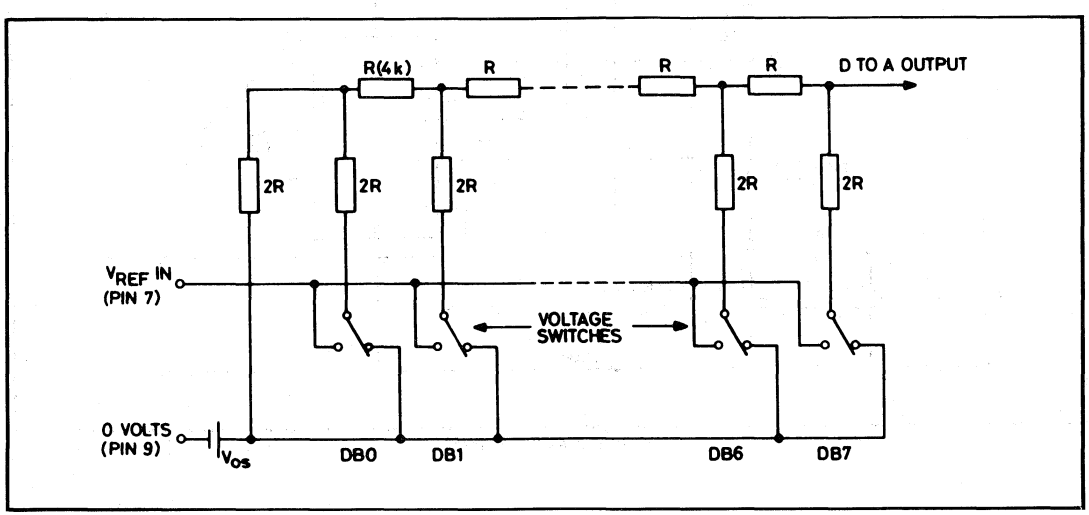



*Fig.6 R-2R ladder network*

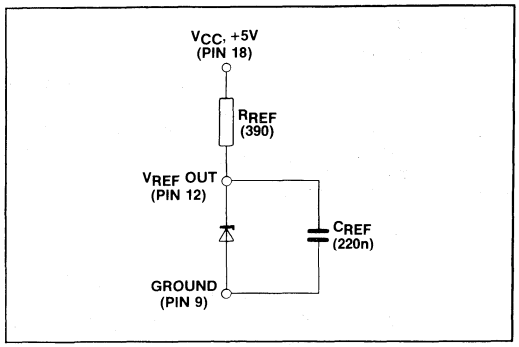



*Fig.7 Internal voltage reference*

## APPLICATIONS

The applications of the ZN525 are too many and varied to detail in this data sheet. However a few basic configurations are illustrated. A feature of the device is that the UP/DOWN control lines can be changed totally asynchronously to the clock. The data presented to these UP/DOWN lines will be latched on the positive edge of clock and the counter will act upon this latched data on the following negative clock edge.

## WAVEFORM GENERATOR

The circuit of a low frequency waveform generator is illustrated in Fig.8. This will produce stable, linear, sawtooth and triangle waveforms.

## RAMP AND COMPARE A TO D CONVERTER

A simple ramp and compare A to D converter can be constructed using the ZN525 as shown in Fig.9.

The counter is set to count up from zero, producing a positive-going ramp at the analog output. When the ramp voltage exceeds the analog input the comparator output will go high, inhibiting the clock and stopping the counter. The converter can be reset and re-started by applying a low-going pulse to the reset input.

The basic analog input range is 0 - $V_{REF}$, but other ranges can be accommodated by adding an attenuator to the comparator unit. The comparator offset adjustment can be used for zero adjustment. Note that in this circuit the mode input is tied low to make the counter stop at full-scale. This prevents the counter cycling in the event of an overrange input.

## TRACKING A TO D CONVERTER

The on-chip up-down counter allows the ZN525 to be configured very simply as a tracking A to D converter using an external comparator, as shown in Fig.10.

In this circuit two ZN424 op amps are used to make a window comparator. This has a deadband equal to one LSB of the DAC output (10mV), which is set by adjusting the offset of A1 until its threshold is 10mV above that of A2.

Whenever the analog voltage is above the threshold of A1 the counter will count up so that the DAC output increases to follow the analog voltage. Whenever the analog voltage is below the threshold of A2 the counter will count down to make the DAC follow the analog voltage. When the analog voltage is between the two thresholds the outputs of A1 and A2 will be high and the counter will be stopped.

The circuit here has an analog input range of ±10V. Other ranges may be accommodated by suitable choice of input resistors.

Note that in this circuit the mode input is tied low. This causes the counter to stop when full-scale or zero is reached, i.e. when the analog input exceeds plus or minus full-scale. Without this feature the counter would simply cycle continuously.

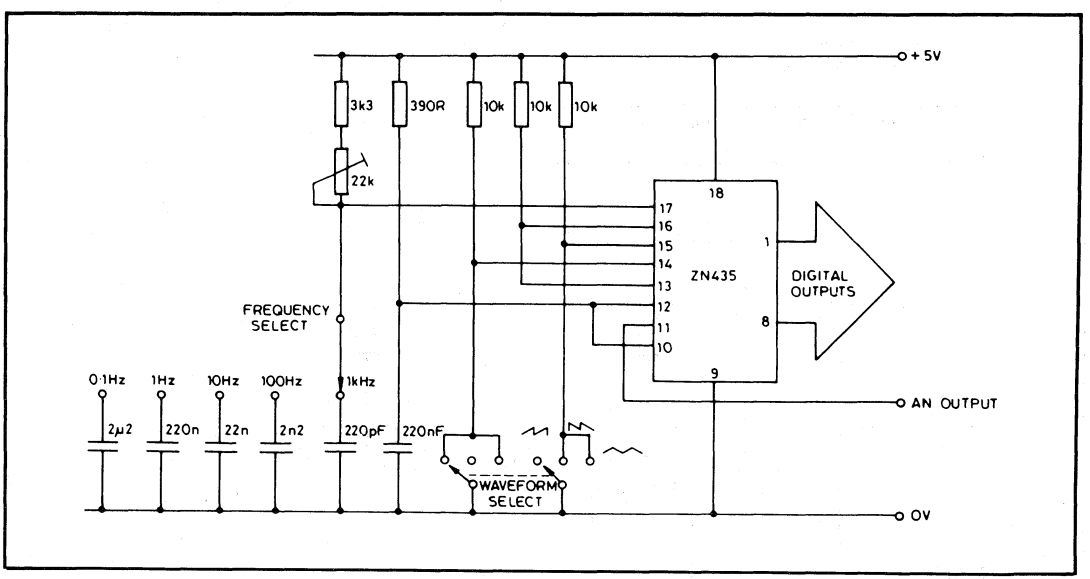



*Fig.8 Waveform generator*

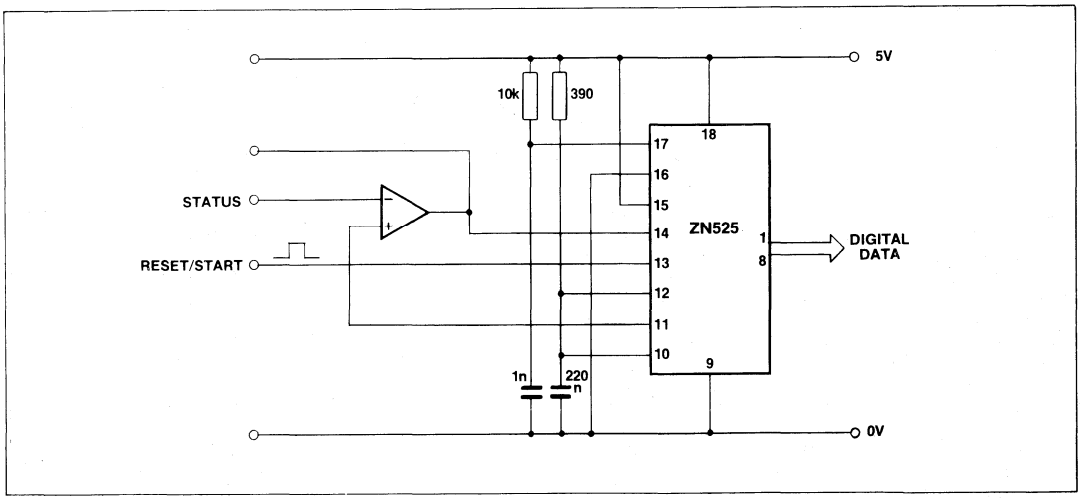



*Fig.9 Ramp and compare ADC*

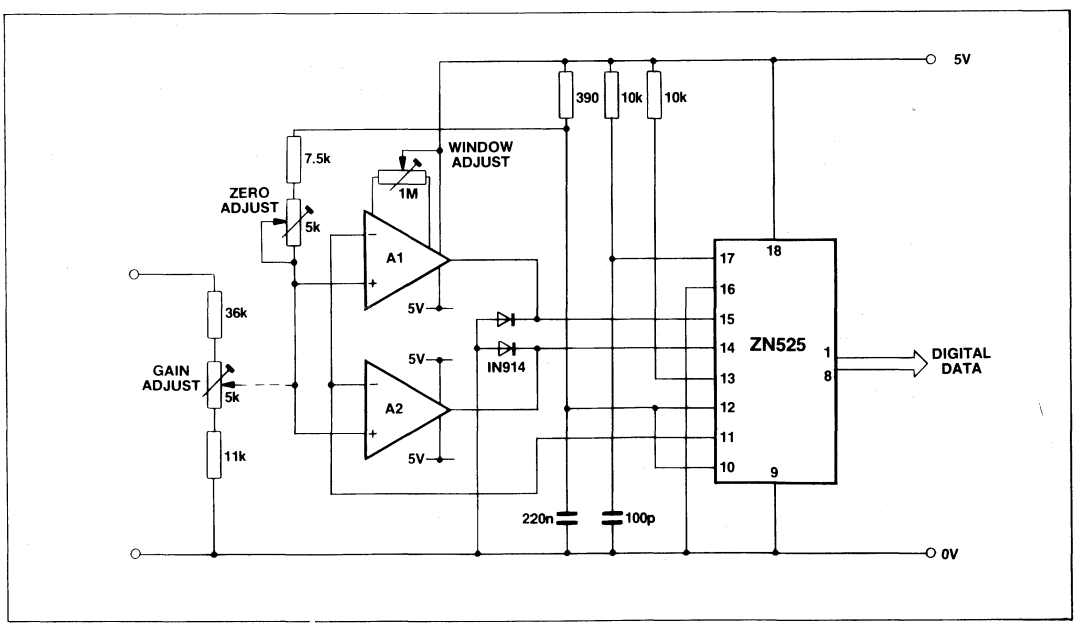



*Fig.10 Tracking ADC*

2375-1.0

# ZN540/ZN541
## 8-BIT ANALOG I/O PORT

The ZN540/1 is a complete analog I/O system contained on one chip. It includes a high speed successive approximation ADC with 5$\mu$s conversion time and double buffered latch outputs (which allow data to be read out regardless of the state of the ADC), two DACs with double latch inputs with 1$\mu$s settling time, and an on-chip (2.5V) temperature compensated bandgap reference. Separate reference input connection for the ADC and a common reference for the DACs allows flexible connection to the on-chip reference or to an external reference source or sources.

The main data interface is a fast 8-bit bi-directional data bus and eight control lines, which allow for complete and flexible management of the system.

A programmable clock prescaler allows input clock speeds of up to 12.8MHz to be used to drive the ADC.

The device is packaged in a 28-pin plastic DIL (DP28) or a 28-pin Plastic Leaded Chip Carrier (HP28).

### FEATURES

- 5$\mu$s ADC/Two 1$\mu$s DACs
- On-Chip Bandgap Reference
- On-Chip Clock Prescaler
- Double Buffered ADC Output
- Fast Microprocessor Interface
- TTL and CMOS Compatible
- Single Supply Operation

### ORDERING INFORMATION

| Device Type | Linearity Error (LSB) | Operating Temperature | Package |
|---|---|---|---|
| **ZN540E** | ±0.5 | -40°C to +85°C | DP28 |
| **ZN540Q** | ±0.5 | -40°C to +85°C | HP28 |
| **ZN541E** | ±1.0 | -40°C to +85°C | DP28 |
| **ZN541Q** | ±1.0 | -40°C to +85°C | HP28 |

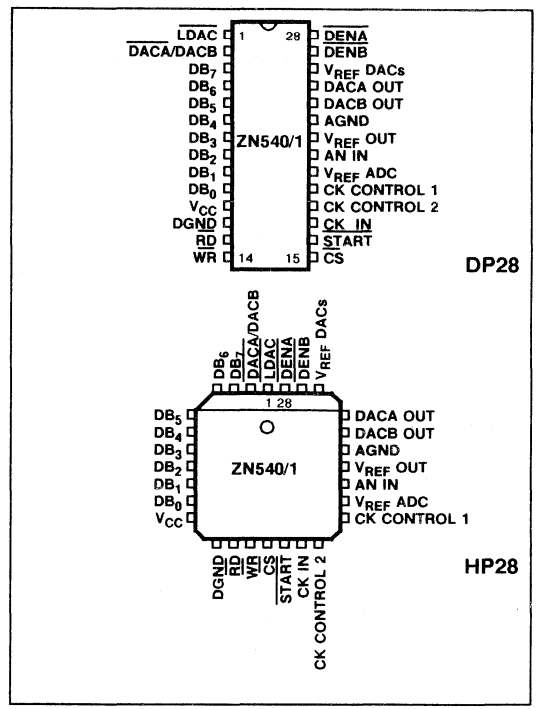



*Fig.1 Pin connections (top view)*

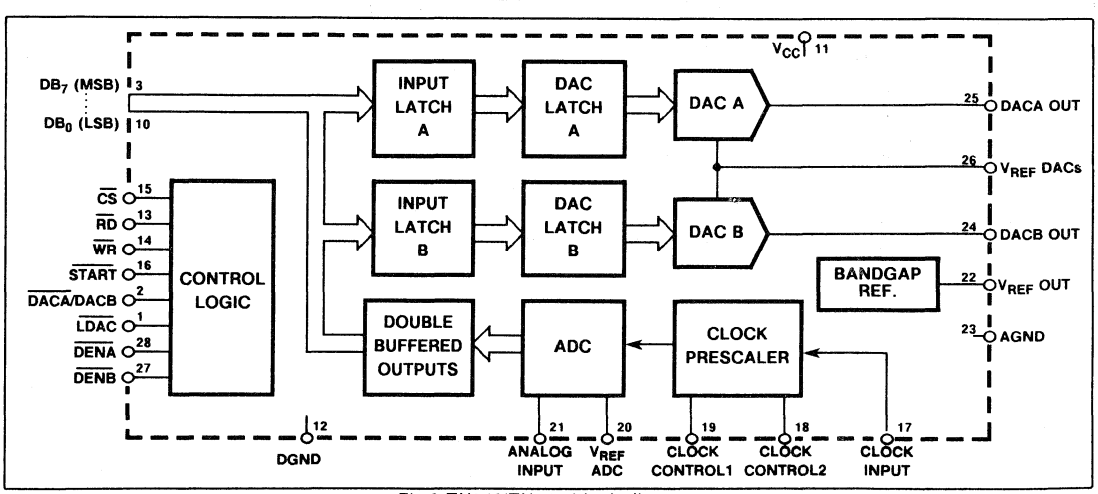



*Fig.2 ZN540/ZN541 block diagram*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | +7V |
| Voltage, logic and $V_{REF}$ inputs | $V_{CC}$ |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -55°C to +125°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_{CC}$ = 5V, $V_{REF}$ = 2.56V, $f_{CLK}$ = 1.6MHz after prescaling

| Characteristic | Value | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | $T_{amb}$ = +25°C | | | Over specified temp. range | | | |
| | Min. | Typ. | Max. | Min. | Max. | | |
| **ADC** | | | | | | | |
| **ZN540** | | | | | | | |
| Linearity error | | | ±0.5 | | ±0.5 | LSB | |
| Differential linearity error | | | ±0.75 | | ±0.75 | LSB | |
| **ZN541** | | | | | | | |
| Linearity error | | | ±1 | | ±1 | LSB | } Note 1 |
| Differential linearity error | | | ±1 | | ±1 | LSB | |
| **All Types** | | | | | | | |
| Zero transition (00000000 → 00000001) | | 10 | | | | mV | |
| Full-scale transition (11111110 → 11111111) | | 2.5 | | | | V | |
| Resolution | 8 | | | 8 | | Bits | |
| Conversion time | 5 | | | | | µs | |
| **DACs** | | | | | | | |
| **ZN540** | | | | | | | |
| Linearity error | | | ±0.5 | | ±0.5 | LSB | |
| Differential linearity error | | | ±0.75 | | ±0.75 | LSB | |
| **ZN541** | | | | | | | |
| Linearity error | | | ±1 | | ±1 | LSB | |
| Differential linearity error | | | ±1 | | ±1 | LSB | |
| **All Types** | | | | | | | |
| Offset voltage | | 3 | | | | mV | I/P = 00000000 |
| Full scale output | | 2.5 | | | | V | I/P = 11111111 |
| Settling time to ½LSB | | 0.7 | | | 1.2 | µs | I/P = 127 to 128 |
| | | 1 | | | 1.7 | µs | I/P = 0 to 255 |
| Analog output resistance | | 3.5 | | | 6 | kΩ | |
| **WHOLE SYSTEM** | | | | | | | |
| Reference input range | 2.0 | | 3.0 | 2.0 | 3.0 | V | |
| Supply voltage | 4.5 | 5.0 | 5.5 | 4.5 | 5.5 | V | |
| Supply current | 75 | 100 | 130 | | 170 | mA | |
| Power consumption | 375 | 500 | 650 | | 850 | mW | |
| **Analog Input** | | | | | | | |
| Analog input current | | -180 | | -110 | -310 | µA | |
| Analog input resistance | | 14 | | | | kΩ | |
| Analog input voltage | -0.5 | | 3.5 | -0.5 | 3.5 | V | |
| **Internal $V_{REF}$** | | | | | | | |
| Output voltage | | 2.5 | | | | V | |
| Output voltage tolerance | | | ±3 | | | % | |
| Output voltage TC | | 70 | | | | ppm/°C | at 5mA |
| Slope impedance | | 0.5 | 2.5 | | 2.5 | Ω | |
| Reference current | 4.0 | | 15.0 | 4.0 | 15.0 | mA | |
| Current drawn by 2 DACs + ADC | | 1 | | | 1.7 | mA | |

## ELECTRICAL CHARACTERISTICS (continued)

| Characteristic | Value | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | $T_{amb}$ = +25°C | | | Over specified temp. range | | | |
| | Min. | Typ. | Max. | Min. | Max. | | |
| **Data Inputs/Outputs** | | | | | | | |
| High level I/P voltage, $V_{IH}$ | 2.0 | | | 2.0 | | V | |
| Low level I/P voltage, $V_{IL}$ | | | 0.8 | | 0.8 | V | |
| High level I/P current, $I_{IH}$ | | 125 | | 75 | 215 | μA | $V_{IN} = V_{CC}$ |
| | | 30 | | 15 | 55 | μA | $V_{IN}$ = 2.4V |
| Low level I/P current, $I_{IL}$ | | -30 | | -15 | -55 | μA | $V_{IN}$ = 0.4V |
| High level O/P voltage, $V_{OH}$ | 2.4 | | | 2.4 | | V | $I_{OH}$ max. |
| Low level O/P voltage, $V_{OL}$ | | | 0.4 | | 0.4 | V | $I_{OL}$ max. |
| High level O/P current, $I_{OH}$ | | | -4 | | -4 | mA | |
| Low level O/P current, $I_{OL}$ | | | 8 | | 8 | mA | |
| **Clock and Control Inputs** | | | | | | | |
| High level I/P voltage, $V_{IH}$ | 2.0 | | | 2.0 | | V | |
| Low level I/Pvoltage, $V_{IL}$ | | | 0.8 | | 0.8 | V | |
| High level I/P current, $I_{IH}$ | | 275 | | 160 | 465 | μA | $V_{IN} = V_{CC}$ |
| | | 70 | | 40 | 120 | μA | $V_{IN}$ = 2.4V |
| Low level I/P current, $I_{IL}$ | | -60 | | -35 | -110 | μA | $V_{IN}$ = 0.4V |
| Clock input frequency | | | 12.8 | | 12.8 | MHz | |
| **TIMING** | | | | | | | |
| **ADC** | | | | | | | |
| $\overline{START}$ pulse width | 62.5 | | | 62.5 | | ns | |
| $\overline{CS}$ to $\overline{RD}$ set-up time | 0 | | | 0 | | ns | |
| $\overline{CS}$ to $\overline{RD}$ hold time | 0 | | | 0 | | ns | |
| $\overline{RD}$ low to data valid delay $t_{E1}$ | | 80 | | | 105 | ns | Using standard 3-state load circuit, Fig.18 |
| $t_{E0}$ | | 40 | | | 45 | ns | |
| $\overline{RD}$ high to bus relinquish delay $t_{D1}$ | | 40 | | | 45 | ns | |
| $t_{D0}$ | | 105 | | | 140 | ns | |
| **DACs** | | | | | | | |
| $\overline{CS}$ to $\overline{WR}$ set-up time | 0 | | | 0 | | ns | |
| $\overline{CS}$ to $\overline{WR}$ hold time | 0 | | | 0 | | ns | |
| $\overline{DACA}$/DACB to $\overline{WR}$ set-up time | 0 | | | 0 | | ns | |
| $\overline{DACA}$/DACB to $\overline{WR}$ hold time | 0 | | | 0 | | ns | |
| Input data valid to $\overline{WR}$ set-up time | 0 | | | 0 | | ns | |
| Input data valid to $\overline{WR}$ hold time | 0 | | | 0 | | ns | |
| $\overline{WR}$ pulse width | 62.5 | | | 62.5 | | ns | Input data valid |
| $\overline{WR}$ to input latch output data valid (internal bus) $t_{DL1}$ | | | 35 | | 35 | ns | |
| $t_{DL0}$ | | | 35 | | 35 | ns | |
| $\overline{LDAC}$ pulse width | 62.5 | | | 62.5 | | ns | $\overline{WR}$ high or input data stable |
| $\overline{DENA}$ pulse width | 62.5 | | | 62.5 | | ns | |
| $\overline{DENB}$ pulse width | 62.5 | | | 62.5 | | ns | |
| $\overline{LDAC}$ to DAC latch output data valid (internal bus) $t_{DT1}$ | | | 35 | | 35 | ns | $\overline{DENA}$/$\overline{DENB}$ low |
| $t_{DT0}$ | | | 35 | | 35 | ns | |

NOTE 1.Guaranteed no missing codes

## PIN DESIGNATIONS

| Pin | Function | Description |
|---|---|---|
| 1 | $\overline{\text{LDAC}}$ | Load DAC (active low). Allows data transfers between the input latches and the DAC latches to take place. |
| 2 | $\overline{\text{DACA/DACB}}$ | Selects whether external data is loaded into input latches A or input latches B in a write operation. If low, latch A is loaded, if high latch B is loaded. |
| 3 | $DB_7$ | Most Significant Bit (data bit 7). |
| 4-9 | $DB_6$-$DB_1$ | Data bits 6 to 1. |
| 10 | $DB_0$ | Least Significant Bit (data bit 0). |
| 11 | VCC | Supply voltage (+5V). |
| 12 | DGND | Digital Ground. |
| 13 | $\overline{\text{RD}}$ | Read input (active low). This allows data to be read from the double buffered output latches of the ADC; it also inhibits the input latches from accepting data. |
| 14 | $\overline{\text{WR}}$ | Write input (active low). This allows data to be written to the input latches of either DAC. |
| 15 | $\overline{\text{CS}}$ | Chip select input (active low). When active this input allows data read and write operations to be performed. |
| 16 | $\overline{\text{START}}$ | Start A-D conversion input (active low). A short pulse on this input causes the system to perform a single A-D conversion. If this input is held low continuous A-D conversions are performed. |
| 17 | CLK IN | Clock input. The rate of the input clock signal determines the rate of A-D conversion. See also CLOCK CONTROL 1 and CLOCK CONTROL 2. |
| 18<br>19 | CLOCK CONTROL 2<br>CLOCK CONTROL 1 | These two control inputs determine the division ratio of the clock prescaler which is selectable for divide by 1, divide by 2, divide by 4, and divide by 8. Using this facility allows clock input frequencies of up to 12.8MHz to be used to drive the ADC (the maximum clock frequency after prescaling is 1.6 MHz, which corresponds to a 5$\mu$s conversion time). |
| 20 | $V_{REF}$ ADC | ADC reference voltage input. |
| 21 | AN IN | Analog voltage input. |
| 22 | VREF OUT | Reference voltage output. A completely separate reference is provided on-chip so either this reference or an external reference may be used for the ADC and/or DACs. |
| 23 | AGND | Analog ground ; this serves the analog sections of both the ADC and the DAC |
| 24 | DACB OUT | DAC B output voltage. |
| 25 | DACA OUT | DAC A output voltage. |
| 26 | $V_{REF}$ DACs | Reference voltage input for both DACs. |
| 27 | $\overline{\text{DENB}}$ | Data transfer enabled in B (active low). Permits data to be transferred between input latches B and DAC B latches when LDAC is low. |
| 28 | $\overline{\text{DENA}}$ | Data transfer enabled in A (active low). Permits data to be transferred between input latches A and DAC A latches when LDAC is low. |

## CIRCUIT DESCRIPTION

### D-A Converters

The two DACs are of the voltage switching type, and use an R-2R ladder network as shown in Fig.3. Each 2R element is connected to either 0V or $V_{REF}$DACs by transistor voltage switches specially designed for low offset voltage (< 1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

$$V_{OUT} = V_{REF}DACs\text{-}V_{OS} \times n/256 + V_{OS},$$

where n is the digital input to the DAC from the DAC latch. VOS is a small offset voltage produced by the DAC switch currents flowing through the package lead resistance. This offset will normally be removed in the setting-up and because the offset temperature coefficient is low ($\pm 6\mu V/°C$), the effect on accuracy is negligible.

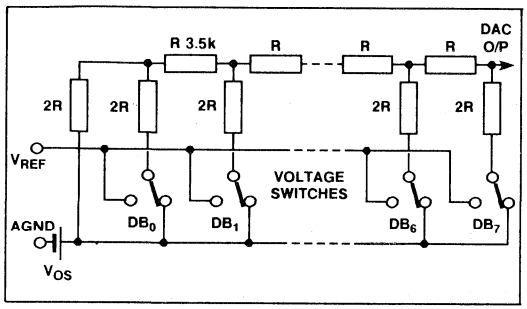



*Fig.3 R-2R ladder network*

Fig.4 shows the analog output equivalent circuit (ignoring $V_{OS}$). The output resistance R has a temperature coefficient of approximately +0.2%/°C. $R_L$ should be chosen to be as large as possible to make the gain drift small. For example, if $R_L = 350k\Omega$ then the gain drift due to the TC of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively each DAC could be buffered by an amplifier.

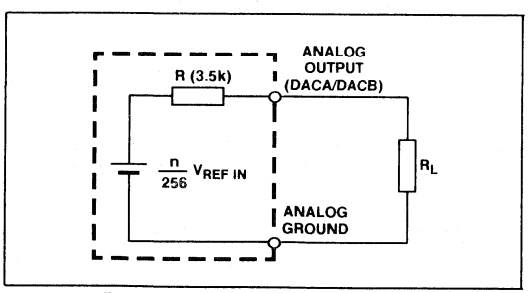



*Fig.4 Analog output equivalent circuit*

### A-D Converter

The analog-to-digital converter on the ZN540/1 uses the successive approximation technique to achieve an 8-bit parallel digital output after 5$\mu$s. The ADC reference input may be connected either to the on-chip 2.5V bandgap reference or to an external voltage reference.

A-D conversion is triggered by the negative edge of the $\overline{START}$ pulse which can be as short as 62.5ns. However, the MSB must be allowed to settle for at least 625ns before the MSB decision is made. To ensure that this criterion is met even with short write pulses, the A-D converter waits for a falling clock edge (from the output of the clock prescaler) before commencing with the conversion. Therefore, a complete conversion takes between 8 and 9 clock cycles dependent on the relative timing of $\overline{START}$ to the clock. If $\overline{START}$ is pulsed low at any time, the conversion will restart.

Internal logic monitors the $\overline{START}$ signal and if at the end of a conversion the $\overline{START}$ input is high the clock signal will be locked out of the converter, leaving it set up and waiting for its next $\overline{START}$ pulse. If the $\overline{START}$ pulse remains low the clock signal will not be inhibited, allowing another conversion to proceed. The double buffering on the A-D data outputs gives extra flexibility, allowing the $\overline{RD}$ (ADC data read) input to operate completely asynchrously with respect to the $\overline{START}$ pulse and the clock input. Note that the $\overline{RD}$ input should not be tied low as this would prevent the ADC updating at the end of a conversion.

The equivalent analog input is shown in Fig.5.

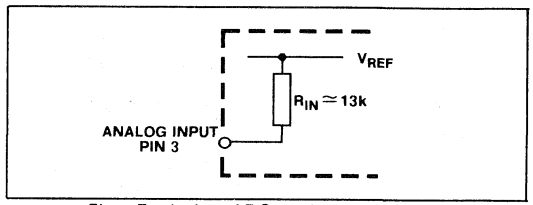



*Fig.5 Equivalent ADC analog input circuit*

### I/O Data Ports

The ZN540 has eight data ports. These are bi-directional input/output ports. The data outputs are provided with 3-state outputs to allow connection to a common data bus (see Figs. 6 and 7). Whilst the output enable signal is high, both output transistors are off and the output buffer presents a high impedance load to the data bus. When this signal is low the data outputs assume the logic states present on the outputs of the double buffered registers.

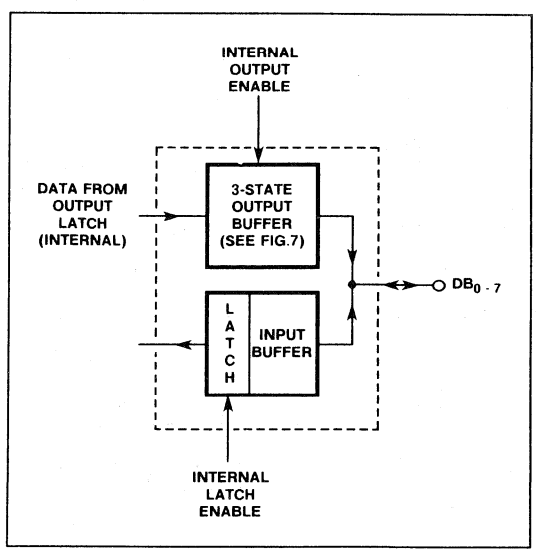



*Fig. 6 ZN540/1 data port*

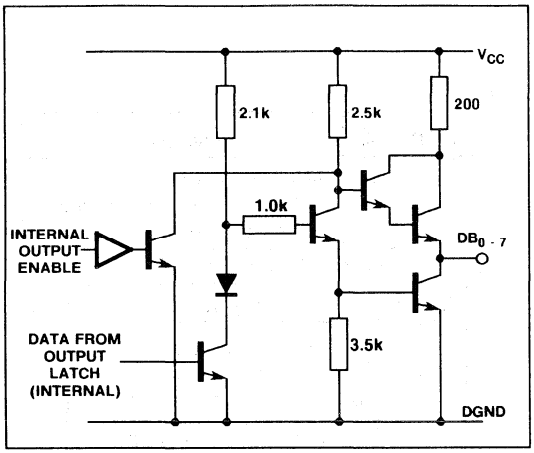



*Fig. 7 Data outputs*

## Clock Input and Clock Prescaler

The external clock determines the rate of the A-D conversion. The ADC requires 8 internal clock periods to perform a single conversion. The minimum conversion time is 5$\mu$s, which corresponds to a maximum ADC clock rate of 1.6MHz. However, by setting the clock prescaler to the appropriate division ratio, external clock signals of up to 12.8MHz may be used.

The inputs CLOCK CONTROL1 and CLOCK CONTROL2 determine the division ratio of the clock prescaler which is selectable to divide by 1, 2, 4 or 8 – see Table 5.

## Internal Voltage Reference

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (see Fig.8). A resistor ($R_{REF}$) should be connected between $V_{CC}$ and $V_{REF}$OUT and a decoupling capacitor ($C_{REF}$, 22$\mu$F, electrolytic) is required between $V_{REF}$OUT and AGND. For internal reference operation with the ADC, $V_{REF}$ADC must be connected to $V_{REF}$OUT; with the DACs, $V_{REF}$DACs must be connected to $V_{REF}$OUT (see Fig.9). A suitable reference current to drive both the ADC and the DACs in one ZN540 is nominally 5mA; this will be supplied by an $R_{REF}$ of 510Ω: (5-2.5)/510 = 4.9mA

## External Voltage Reference

An external reference may also be used; this can be in the range 2V to 3V for both the ADC and the DACs.

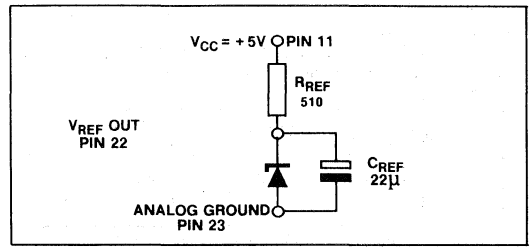



*Fig.8 Internal voltage reference*

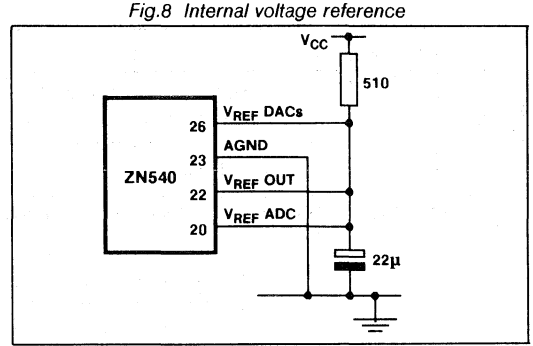



*Fig.9 External components required for on-chip reference operation*

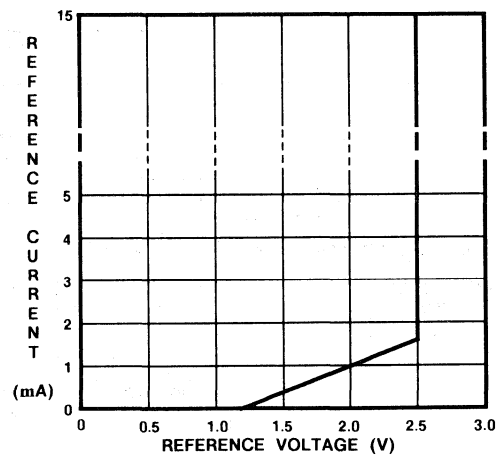



*Fig.10 Typical reference characteristic*

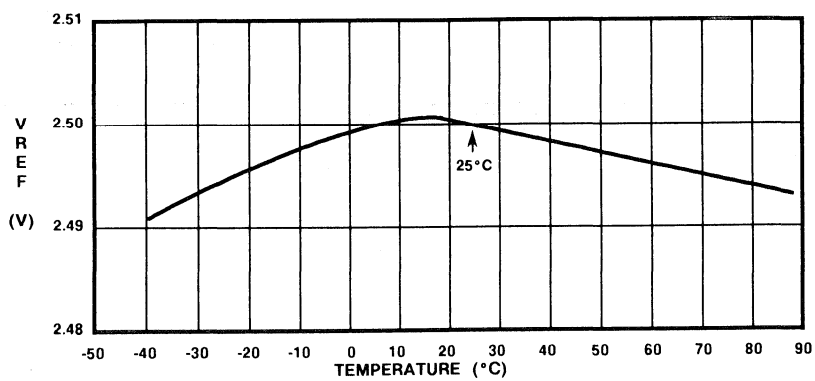



*Fig.11 Typical temperature characteristic*

## TIMING AND CONTROL

### Logic Interface

Tables 1 through 5 and Fig.12 show the control input requirements for the various system functions.

**DACs**

| $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | $\overline{DACA}$/DACB | Function |
|---|---|---|---|---|
| 1 | 0 | 0 | 0 | Load I/P Latch A |
| 1 | 0 | 0 | 1 | Load I/P Latch B |

*Table 1 Loading input latches with data*

| $\overline{LDAC}$ | $\overline{DENA}$ | $\overline{DENB}$ | Function |
|---|---|---|---|
| 0 | 0 | 1 | Transfer Latch A to DACA |
| 0 | 1 | 0 | Transfer Latch B to DACB |
| 0 | 0 | 0 | Transfer Latch A to DACA and Latch B to DACB |

*Table 2 Transferring data from input latches to DAC latches*

**ADC**

| $\overline{RD}$ | $\overline{WR}$ | $\overline{CS}$ | Function |
|---|---|---|---|
| 0 | 1 | 0 | Read ADC data from buffered latches (independent of state of current conversion) |

*Table 3 Reading ADC data*

| $\overline{START}$ | Function |
|---|---|
| 1 | No conversion started |
| ⊓ | Single A-D conversion then stop |
| 0 | Continuous A-D conversions |

*Table 4 Starting A-D conversion*

| CLK CNTRL 1 | CLK CNTRL 2 | Clock division ratio |
|---|---|---|
| 0 | 0 | ÷8 |
| 1 | 0 | ÷4 |
| 0 | 1 | ÷2 |
| 1 | 1 | ÷1 |

*Table 5 Clock prescaler*

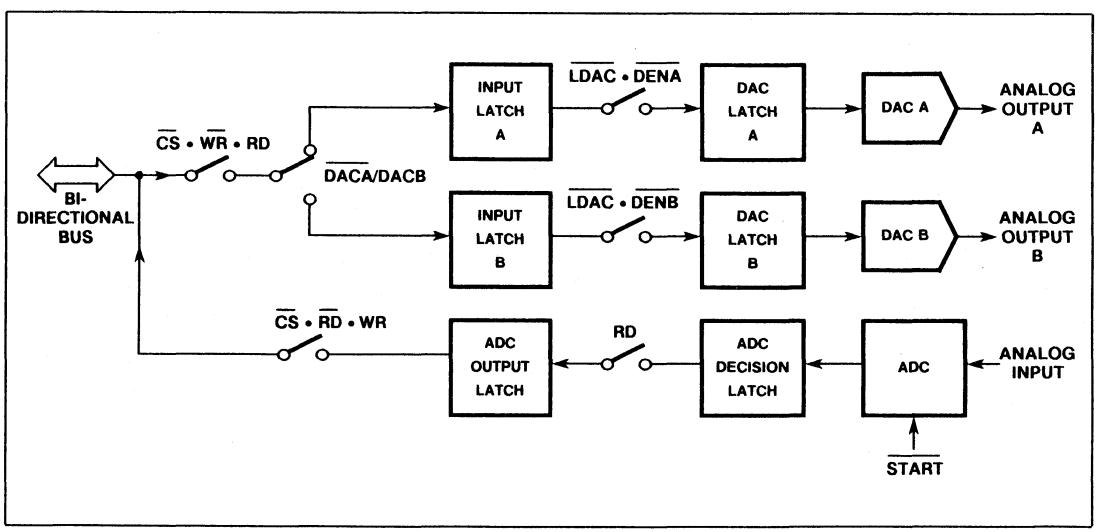



*Fig.12 ZN540/1 logic diagram*

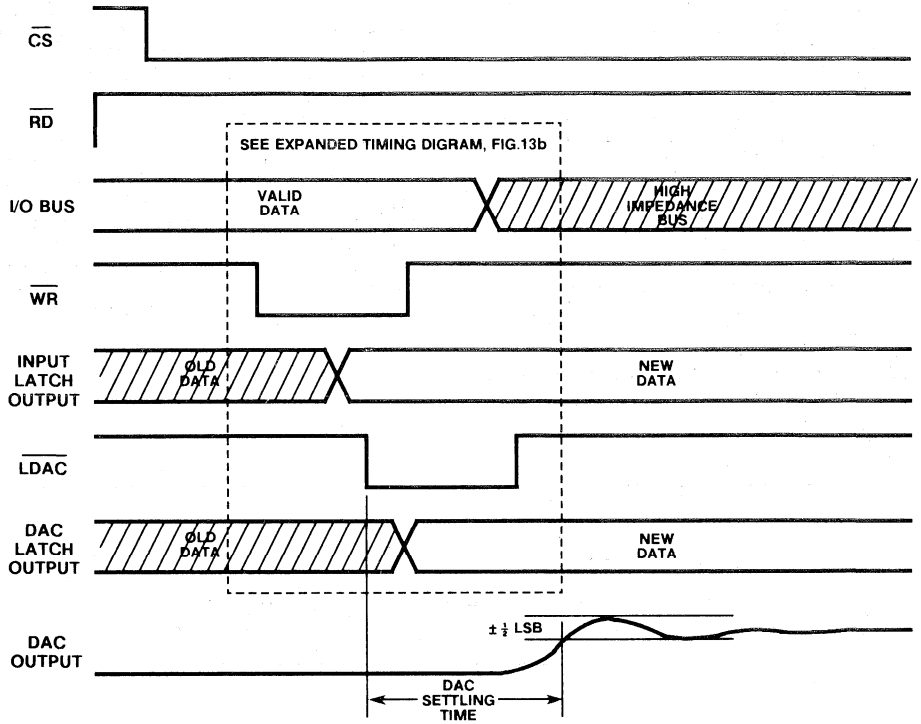



*Fig.13a DAC timings*

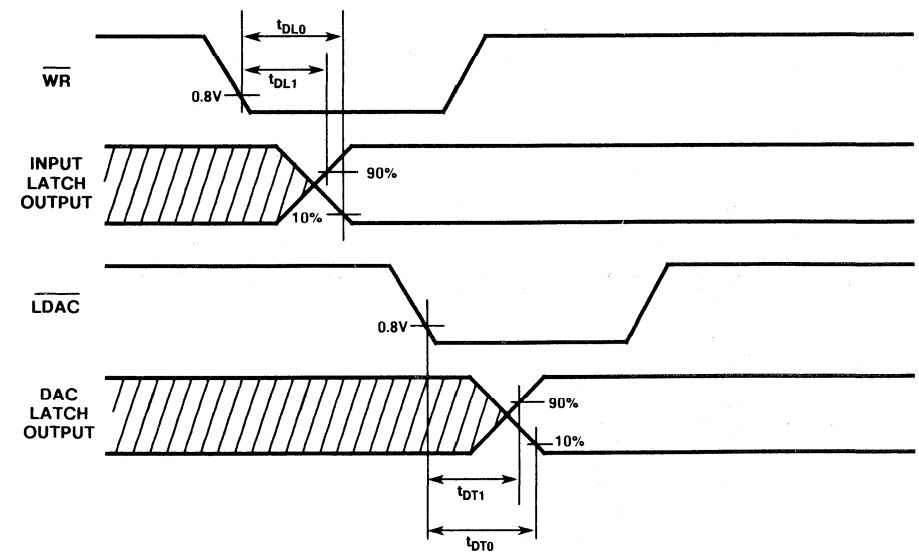



*Fig.13b Expanded DAC timings*

*Fig.13*

## DAC Timing and Control

Each DAC has two sets of eight latches: the input latches store data ready to be transferred to the DAC latches; the DAC latches hold the data which is being used in the current D-A conversion.

All the DAC control lines are level sensitive. To load data into one of the sets of input latches, $\overline{CS}$ must be low and $\overline{RD}$ high. The input latches to be updated are selected using the $\overline{DACA}$/DACB input. If $\overline{WR}$ is taken low the selected input latches will be updated with the data present on the I/O port (see Table 1). Independent of the input latches' write operation, is the transfer data operation. Data may be transferred from latches A to DAC latches A, from latches B to DAC latches B, or both operations at the same time. $\overline{DENA}$ and $\overline{DENB}$ determine which operation. $\overline{LDAC}$ low allows the transfer operation(s) to take place. Combining the load data operations and the transfer data operations, it is possible to have a direct path between the I/O port and DACA or DACB, the intervening latches being transparent. In this case new data on the I/O port will immediately start updating the DAC.

The timing diagram for DAC operations is shown in Fig,13.

## ADC Timing and Control

To perform an A-D conversion the $\overline{START}$ signal must either be held low or pulsed low for greater than 62.5ns. This may be done at any time independent of the other operations being performed by the system. The results of the most recent conversion will be held in a set of latches (the 'decision latches') and will only be transferred to the output latches ready for reading when an ADC read operation is not being performed. A subsequent read operation will bring this new data out to the I/O port. To perform an ADC read operation $\overline{CS}$ must be low and $\overline{WR}$ must be high, then, taking $\overline{RD}$ low will disable the DAC input buffers and allow data to be read from the I/O port. The read operation has no effect on the current conversion in progress.

The timing diagrams for ADC operation are shown in Fig.s 14, 15 and 16.

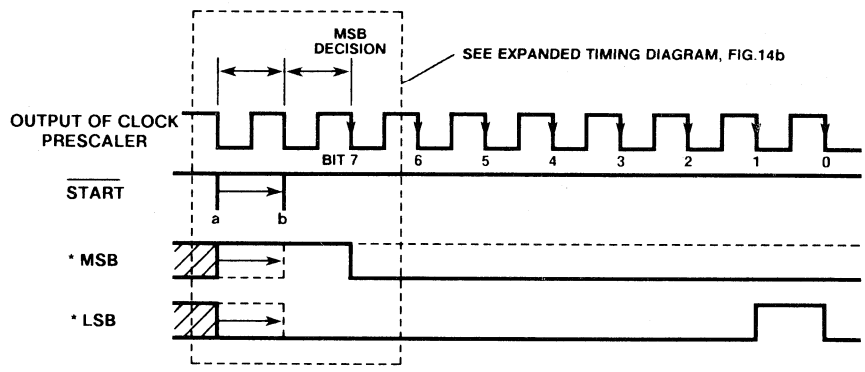



*Fig.14a ADC timing*

* NOTE. THESE SIGNALS ARE THE INTERNAL MSB AND LSB OF THE SUCCESSIVE APPROXIMATION REGISTER

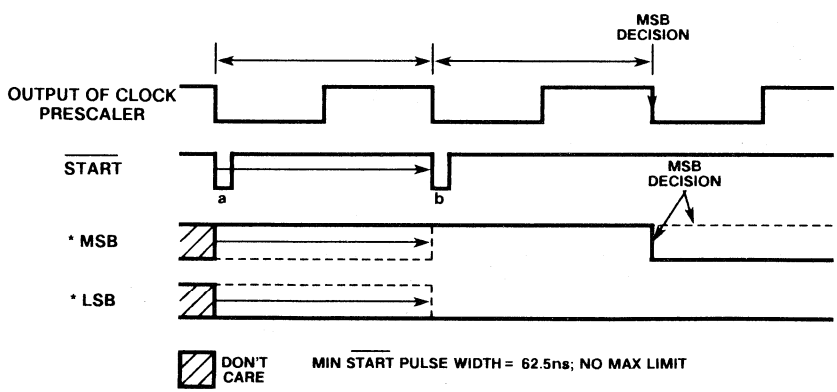



*Fig.14b ADC timing (expanded)*

*Fig.14 ZN540/1 ADC timing diagram*

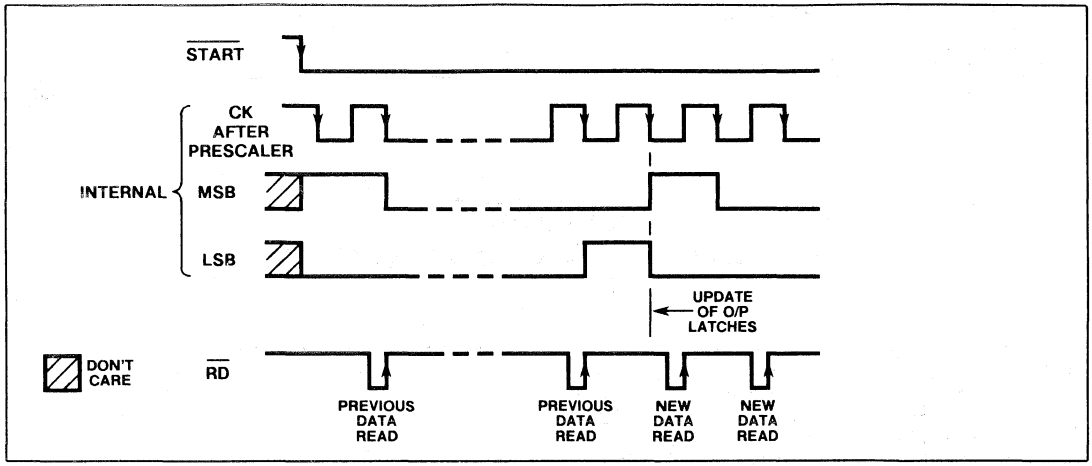



*Fig.15 ADC timing for continuous conversion*

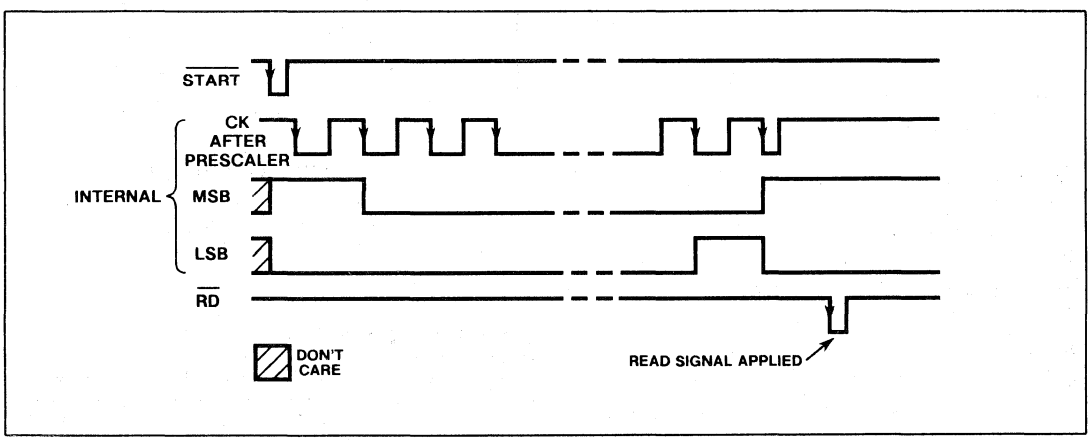



*Fig.16 ADC timing for single conversion*

## Data Outputs

A timing diagram and test circuit for the bus access/relinquish delays are shown in Figs.17 and 18.

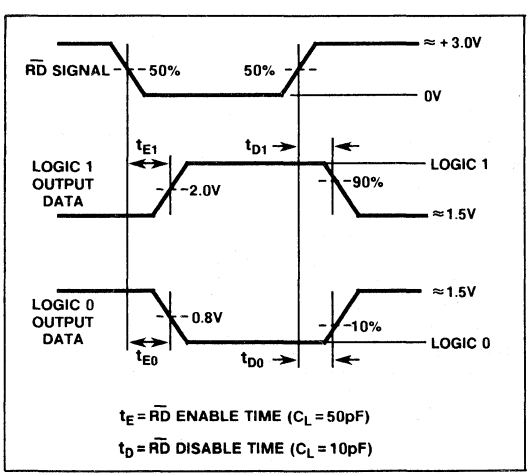



*Fig.17 Output enable/disable delays*

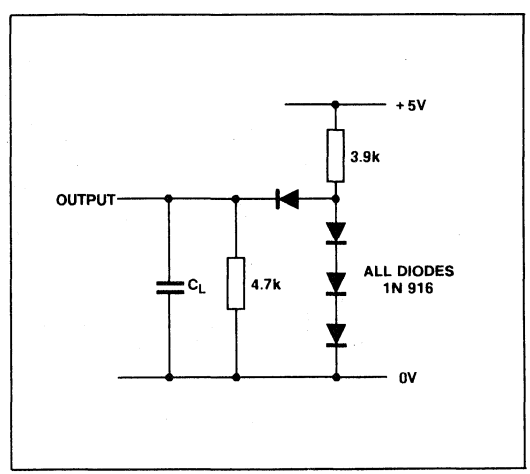
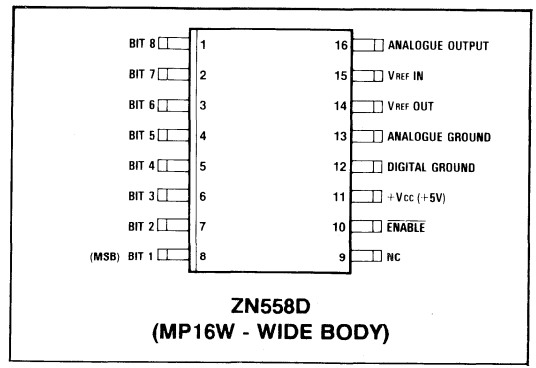



*Fig.18 Output load test circuit*

# ZN558D
## 8-BIT LATCHED INPUT D-A CONVERTER

The ZN558 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when enable is LOW and the data is held when enable is taken HIGH. The ZN558 also contains a 2.5V reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.




**ZN558D**
**(MP16W - WIDE BODY)**

**Pin connections - top view**

### FEATURES

- Contains DAC with Data Latch and On-Chip Reference
- Guaranteed Monotonic over the Full Operating Temperature Range
- Single +5V Supply
- Microprocessor Compatible
- TTL and 5V CMOS Compatible
- 800ns Settling Time
- Complementary to ZN447 A-D Series
- Commercial and Military Temperature Ranges
- Available in Miniature Plastic Surface Mount Package (MP16)

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| ZN558D | 0°C to +70°C | MP16W |

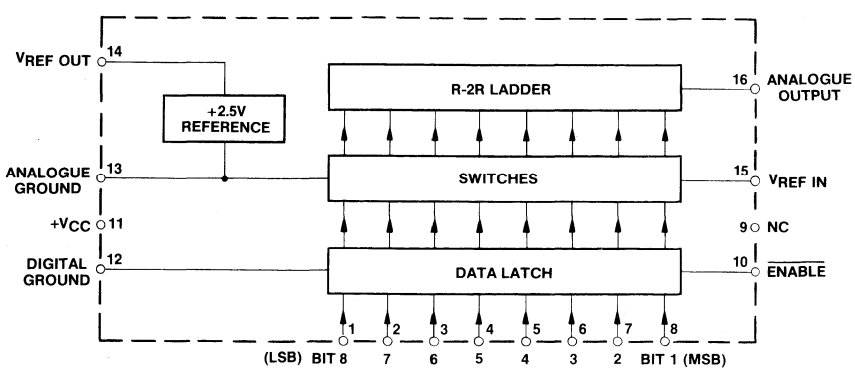



**Fig.1 System diagram**

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | +7.0V |
| Max. voltage, logic and $V_{REF}$ input | $+V_{CC}$ |
| Operating temperature range | 0°C to +70°C |
| Storage temperature range | -55°C to +125°C |
| Analogue ground to digital ground | ±200mV |

**ELECTRICAL CHARACTERISTICS** ($V_{CC}$ = +5V, $T_{amb}$ = 25°C unless otherwise specified).

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| **Internal voltage reference** | | | | | |
| Output voltage | 2.475 | 2.550 | 2.625 | V | $R_{REF}$ = 390Ω, $C_{REF}$ = 1μF |
| Slope resistance | | 0.5 | 2 | Ω | |
| $V_{REF\ OUT}$ T.C. | | 50 | | ppm/°C | |
| Reference current | 4 | | 15 | mA | Note 1 |
| **D-A converter** | | | | | |
| Linearity error | | | ±0.5 | LSB | 2.0V ≤ $V_{REF\ IN}$ ≤ 3.0V |
| Differential non-linearity | | ±0.5 | | LSB | |
| Linearity error T.C. | | ±3 | | ppm/°C | |
| Differential non-linearity T.C. | | ±6 | | ppm/°C | |
| Offset voltage | | 2 | 5 | mV | All bits OFF |
| Offset voltage | | ±6 | | μV/°C | |
| Full scale output | 2.545 | 2.550 | 2.555 | | External reference $V_{REF\ IN}$ = 2.560V, all bits ON |
| Full scale output T.C. | | 2 | | ppm/°C | |
| Analogue output resistance | | 4 | | kΩ | |
| External reference voltage | 0 | | 3.0 | V | |
| Settling time to 0.5 LSB | | 800 | | ns | 1 LSB major transition (note 2) |
| | | 1.25 | | μs | All bits ON to OFF or OFF to ON (note 2) |
| Operating temperature range: ZN558D | 0 | | 70 | C | |
| Supply voltage ($V_{CC}$) | 4.5 | 5.0 | 5.5 | V | |

Note 1 See REFERENCE.
Note 2 $R_L$ = 10MΩ, $C_L$ = 10pF.

**ELECTRICAL CHARACTERISTICS** (Cont.)

| Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|
| Supply current | | 20 | 30 | mA | Note 3 |
| Power consumption | | 100 | | mW | |
| **Logic** (over specified operating temperature range) | | | | | |
| High level input voltage | 2.0 | | | V | |
| Low level input voltage | | | 0.8 | V | |
| High level input current | | | 60 | $\mu$A | $V_{IN}=5.5V$, $V_{CC}=$Max. |
| | | | 20 | $\mu$A | $V_{IN}=2.4V$, $V_{CC}=$Max. |
| Low level input current | | | −5 | $\mu$A | $V_{IN}=0.4V$, $V_{CC}=$Max. |
| Input clamp diode voltage | | −1.5 | | V | $I_{IN}=-8mA$ |
| Enable pulse width | 100 | | | ns | |
| Data set-up time | 150 | | | ns | Note 4 |
| Data hold time | 10 | | | ns | Note 5 |

Note 3 All inputs HIGH ($V_{IH}=3.5V$).
Note 4 Set up time before $\overline{\text{enable}}$ goes high.
Note 5 Hold time after $\overline{\text{enable}}$ goes high.

## D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig. 2. Each 2R element is connected to 0V or $V_{REF\,IN}$ by transistor voltage switches specially designed for low offset voltage (<1mV). A binary weighted voltage is produced at the output of the R-2R ladder.

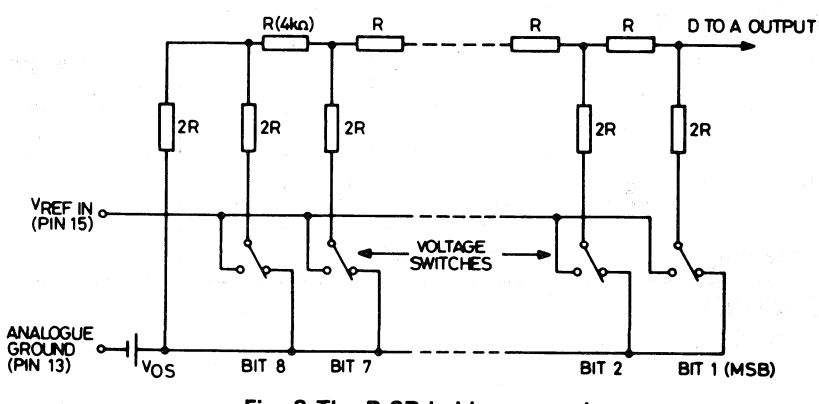



**Fig. 2 The R-2R ladder network**

Analog output $= \frac{n}{256}(V_{REF\ IN} - V_{OS}) + V_{OS}$

where n is the digital input to the D-A from the data latch.

$V_{OS}$ is a small offset voltage produced by the D-A switch currents flowing through the package lead resistance. The value of $V_{OS}$ is typically 1mV. This offset will normally be removed by the setting up procedure (see APPLICATIONS section) and because the offset temperature coefficient is low ($\pm 6\mu V/°C$) the effect on accuracy is negligible.

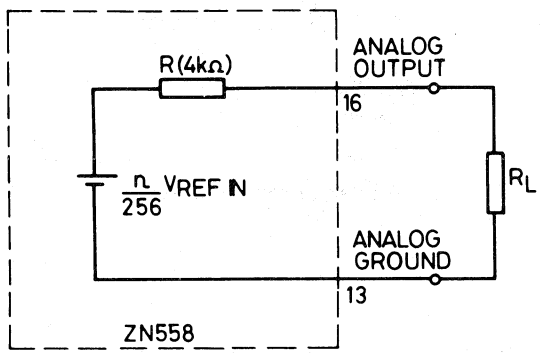



**Fig. 3 Analogue output equivalent circuit**

Fig. 3 shows an equivalent circuit of the output (ignoring $V_{OS}$). The output resistance R has a temperature coefficient of +0.2% per °C.

The gain drift due to this is $\frac{0.2R}{R+R_L}$ % per °C

$R_L$ should be chosen to be as large as possible to make the gain drift small. As an example if $R_L$ = 400kΩ then the gain drift due to the T.C. of R for a 100°C change in ambient temperature will be less than 0.2%. Alternatively the ZN558 can be buffered by an amplifier (see Operating Notes).

## REFERENCE

### (a) Internal reference

The internal reference is an active band gap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig. 4). A resistor ($R_{REF}$), should be connected between $+V_{CC}$ (pin 11) and pin 14. The recommended value of 390Ω will supply a nominal reference current of (5.0-2.5)/0.39 = 6.4mA. A stabilising/decoupling capacitor $C_{REF} = 1\mu F$ is required between pins 14 and 13 for internal reference option, $V_{REF\ OUT}$ (pin 14) being connected to $V_{REF\ IN}$ (pin 15).

Up to five ZN558's may be driven from one internal reference (there is no need to reduce $R_{REF}$). This useful feature saves power and gives excellent gain tracking between the converters.

### (b) External reference

If required an external reference voltage may be connected to $V_{REF\ IN}$. The slope resistance of such a reference source should be less than $\frac{2.5\Omega}{n}$, where n is the number of converters supplied.

$V_{REF\ IN}$ can be varied from 0 to +3V for ratiometric operation. The ZN558 is guaranteed monotonic for $V_{REF\ IN}$ above 2V.

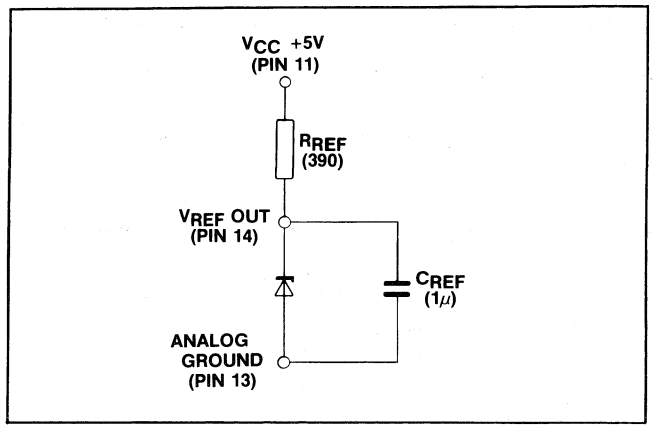



**Fig.4 Internal voltage reference**

## LOGIC

Input coding is binary for unipolar operation and offset binary for bipolar operation. When the enable input is low the data inputs drive the D-A directly. When enable goes high the input data word is held in the data latch.

The equivalent circuit for the data and clock inputs is shown in Fig.5.

The ZN558 is provided with seperate analogue and digital ground connections. The circuit will operate correctly with as much as ±200mV between the two grounds.

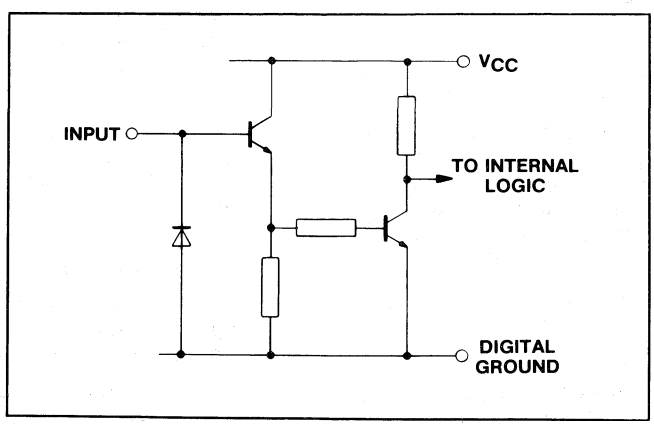



**Fig. 5 Equivalent circuit of all inputs**

## OPERATING NOTES

### (1) Unipolar D-A converter

The nominal output range of the ZN558 is 0 to $V_{REF\ IN}$ through a 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

The general scheme (Fig. 6) is suitable for amplifiers with input bias currents less than 1.5μA.

The resulting full scale range is given by

$$V_{OUT}\ FS = \left(1 + \frac{R1}{R2}\right) V_{REF\ IN} = G.V_{REF\ IN}$$

The impedance at the inverting input is R1//R2 and for low drift with temperature this parallel combination should be equal to the ladder resistance (4kΩ). The required nominal values of R1 and R2 are given by $R1 = 4GkΩ$ and $R_2 = 4G/(G-1)kΩ$.

Using these relationships a table of nominal resistance values for $R_1$ and $R_2$ can be constructed for $V_{REF\ IN} = 2.5V$.

| Output range | G | $R_1$ | $R_2$ |
|---|---|---|---|
| +5V | 2 | 8kΩ | 8kΩ |
| +10V | 4 | 16kΩ | 5.33kΩ |

For gain setting $R_1$ is adjusted about its nominal value. Practical circuit realisations (including amplifier stabilising components) for +5 and +10V output ranges are given in Fig. 7. Settling time for a major transistion is 1.5μs typical.

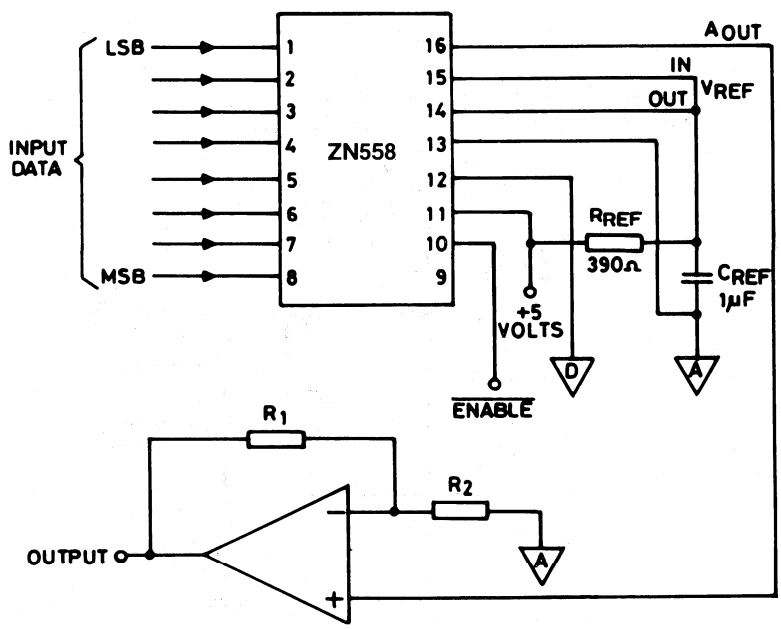
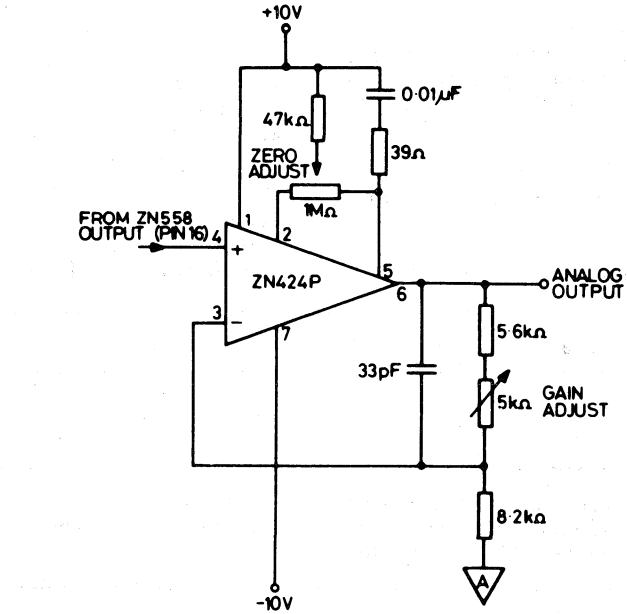



Fig. 6 Unipolar operation - basic circuit



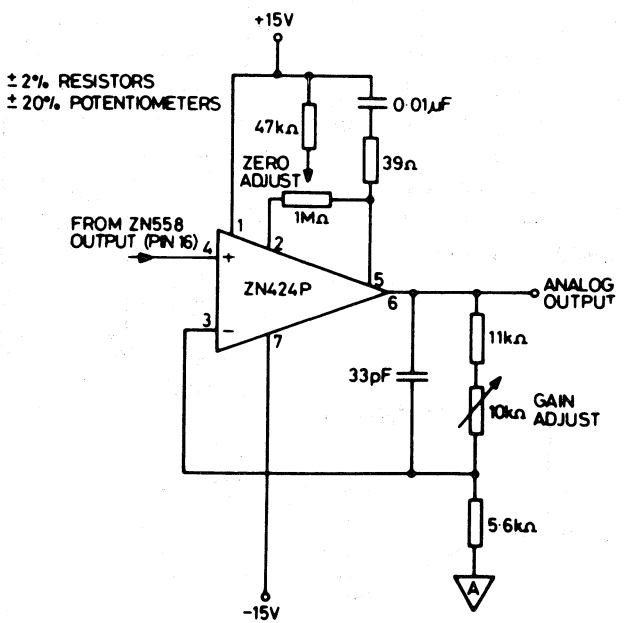




**Fig. 7 Unipolar operation - component values**

## UNIPOLAR ADJUSTMENT PROCEDURE

(i) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust zero until $V_{OUT} = 0.0000V$.
(ii) Set all bits ON (high) and adjust gain until $V_{OUT} = FS - 1LSB$.

### UNIPOLAR SETTING UP POINTS

| Output range, +FS | LSB | FS - 1LSB |
|---|---|---|
| +5V | 19.5mV | 4.9805V |
| +10V | 39.1mV | 9.9609V |

$$1LSB = \frac{FS}{256}$$

### UNIPOLAR LOGIC CODING

| Input code (Binary) | Analog output (Nominal value) |
|---|---|
| 11111111 | FS - 1LSB |
| 11111110 | FS - 2LSB |
| 11000000 | ¾ FS |
| 10000001 | ½FS + 1LSB |
| 10000000 | ½FS |
| 01111111 | ½FS - 1LSB |
| 01000000 | ¼FS |
| 00000001 | 1LSB |
| 00000000 | 0 |

### (2) Bipolar D-A converter

For bipolar operation the output from the ZN558 is offset by half full scale by connecting a resistor $R_3$ between $V_{REF\ IN}$ and the inverting input of the buffer amplifier (Fig. 8).

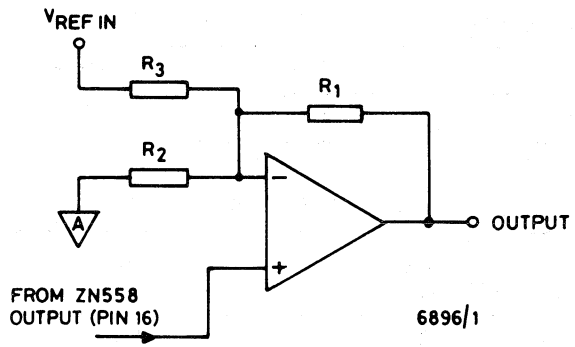



**Fig. 8 Bipolar operation - basic circuit**

When the digital input to the ZN558 is zero the analogue output is zero and the amplifier output should be – full scale. An input of all ones to the D-A will give a ZN558 output of $V_{REF\ IN}$ and the amplifier output required is + full scale. Also, to match the ladder resistance the parallel combination of $R_1$, $R_2$ and $R_3$ should be 4kΩ.

The nominal values of $R_1$, $R_2$ and $R_3$ which meet these conditions are given by

$R_1 = 8Gk\Omega$, $R_2 = 8G/(G-1)k\Omega$ and $R_3 = 8k\Omega$

where the resultant output range is $\pm G\ V_{REF\ IN}$.

A bipolar output range of $\pm V_{REF\ IN}$ (which corresponds to the basic unipolar range 0 to $V_{REF\ IN}$) is obtained if $R_1 = R_3 = 8k\Omega$ and $R_2 = \infty$.

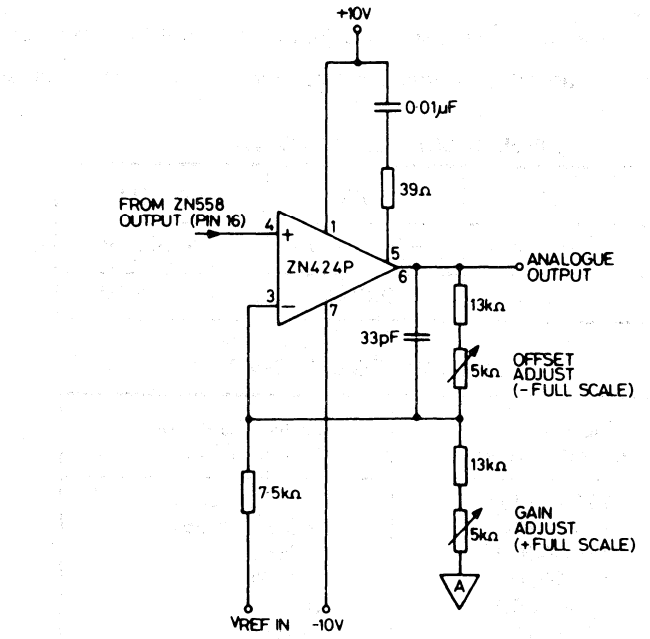
Assuming that $V_{REF\ IN} = 2.5V$ the nominal values of resistors for ±5 and ±10V output ranges are given in the following table:

| Output range | G | $R_1$ | $R_2$ | $R_3$ |
|---|---|---|---|---|
| ±5V | 2 | 16kΩ | 16kΩ | 8kΩ |
| ±10V | 4 | 32kΩ | 10.66kΩ | 8kΩ |

Minus full scale (offset) is set by adjusting $R_1$ about its nominal value relative to $R_3$. Plus full scale (gain) is set by adjusting $R_2$ relative to $R_1$.

Practical circuit realisations are given in Fig. 9.

Note that in the ±5V case $R_3$ has been chosen as 7.5kΩ (instead of 8.2kΩ) to get a more symmetrical range of adjustment using standard potentiometers. Settling time for a major transition is 1.5μs typical.



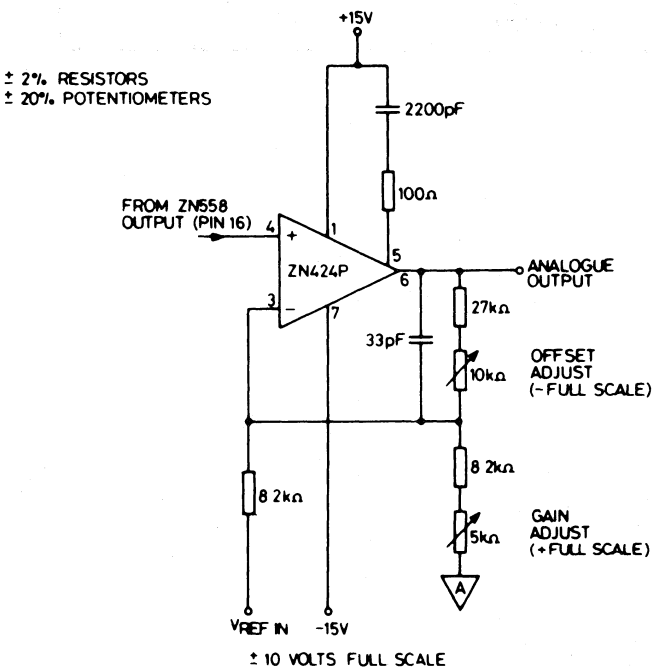




Fig. 9 Bipolar operation - component values

**Bipolar Adjustment Procedure**

(1) Set all bits to OFF (low) with $\overline{\text{enable}}$ low and adjust offset until the amplifier output reads −full scale.

(2) Set all bits ON (high) and adjust gain until the amplifier output reads +(full scale - 1LSB).

**BIPOLAR SETTING UP POINTS**

| Input range, ±FS | LSB | −FS | +(FS - 1LSB) |
|---|---|---|---|
| ±5V | 39.1mV | −5.0000V | +4.9609V |
| ±10V | 78.1mV | −10.0000V | +9.9219V |

$$1LSB = \frac{2FS}{256}$$

**BIPOLAR LOGIC CODING**

| Input code (Offset binary) | Analogue output (Nominal value) |
|---|---|
| 11111111 | +(FS - 1LSB) |
| 11111110 | +(FS - 2LSB) |
| 11000000 | +½FS |
| 10000001 | +1LSB |
| 10000000 | 0 |
| 01111111 | −1LSB |
| 01000000 | −½FS |
| 00000001 | −(FS - 1LSB) |
| 00000000 | −FS |

2354-1.0

# ZN682/3, ZN684/5, ZN688/9

## 2/4/8-CHANNEL 8-BIT MICROPROCESSOR COMPATIBLE ADCs

*(ZN688/9 supersede ZN538/9 designs)*

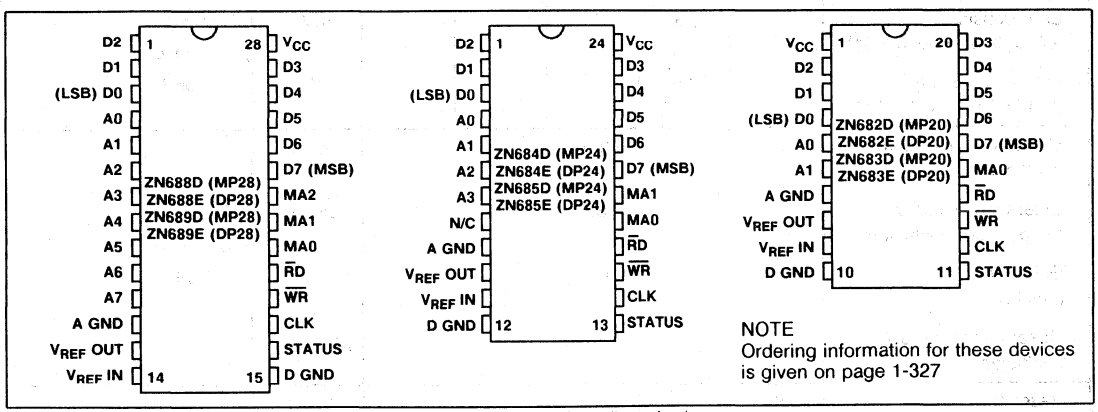
These integrated circuits are a set of 2, 4 and 8-channel, 8-bit analog to digital converters, designed to interface easily to most popular microprocessors.

Each consists of an 8-bit successive approximation A-D converter, a 2, 4 or 8-channel multiplexer, clock generator, 2.5V bandgap reference, control logic and double buffered latches with 3-state outputs. The address bus ($MA_0 \rightarrow MA_n$) is used to select the channel on which the next conversion is to be performed.

The devices are offered in two linearity options: ±0.5LSB (ZN682/4/8) or ±1.0 LSB (ZN683/5/9). All operate over the temperature range -40°C to +85°C from a single +5V supply and are available in a choice of surface mount or plastic DIL packages

### FEATURES

- Choice of Linearity: ±0.5LSB or ±1LSB
- 8 µs Conversion Time
- Choice of 2,4 or 8 Analog Inputs
- Continuous Conversion on Specified Channel
- Sub-100ns Access Time
- Operates from Single +5V Supply
- On-Chip Bandgap Reference
- On-Chip Overdrivable Clock Oscillator
- Microprocessor/TTL/CMOS Compatible
- ROM Type Operation




NOTE
Ordering information for these devices is given on page 1-327

*Fig.1 Pin connections (top view)*

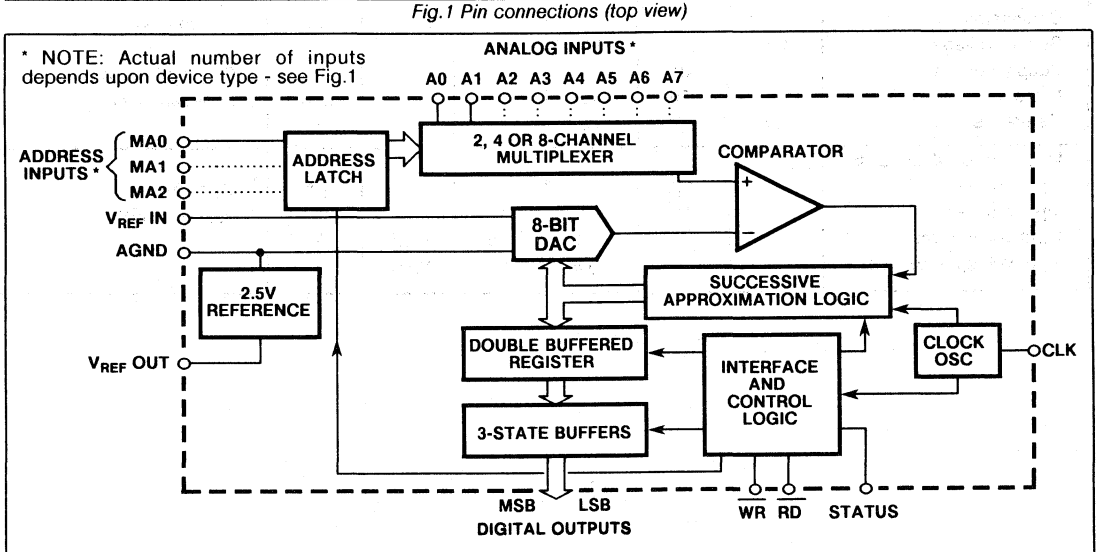



*Fig.2 System diagram*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage, $V_{CC}$ | +7V |
| Voltage, logic and $V_{REF}$ inputs | $V_{CC}$ |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -55°C to +125°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$V_{CC}$ = 5V, $T_{amb}$ = +25°C, $f_{CLK}$ = 1.0MHz

| Characteristic | Value | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | $T_{amb}$ = +25°C | | | Over specified temp. range | | | |
| | Min. | Typ. | Max. | Min. | Max. | | |
| **ZN688/4/2** | | | | | | | |
| Linearity error | | | ±0.5 | | ±0.5 | LSB | |
| Differential linearity error | | | ±0.75 | | ±0.75 | LSB | |
| **ZN689/5/3** | | | | | | | |
| Linearity error | | | ±1 | | ±1 | LSB | |
| Differential linearity error | | | ±1 | | ±1 | LSB | |
| **ALL TYPES** | | | | | | | |
| Zero transition (00000000 → 00000001) | | 13 | | | | mV | External reference |
| Full-scale transition (11111110 → 11111111) | | 2.540 | | | | V | = 2.56V |
| Linearity temperature coefficient | | | ±3 typ | | | ppm/°C | External reference = 2.56V |
| Differential linearity temperature coefficient | | | ±6 typ | | | ppm/°C | |
| Gain temperature coefficient | | | ±10 typ | | | ppm/°C | |
| Offset temperature coefficient | | | ±7 typ | | | ppm/°C | |
| Resolution | 8 | | | | | bits | |
| Conversion time | 8 | | | | | µs | Per channel |
| Supply voltage | 4.5 | 5.0 | 5.5 | 4.5 | 5.5 | V | |
| Supply current | | 40 | 55 | | | mA | Outputs in high impedance state |
| Power consumption | | 200 | 275 | | | mW | |
| Reference input range | 2.0 | 2.0 | 3.0 | | | V | |
| **MULTIPLEXED INPUTS** | | | | | | | |
| Input current | | -106 | | | | µA | $V_{IN}$ = 0V |
| Input resistance | | 24 | | | | kΩ | $V_{REF}$ = 2.56V |
| Input voltage (Max.) | -0.5 | | +3.5 | -0.5 | +3.5 | V | |
| Input voltage (operational) | 0 | | $V_{REF}$ | 0 | $V_{REF}$ | V | |

## ELECTRICAL CHARACTERISTICS (continued)

| Characteristic | Value | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | $T_{amb}$ = +25°C | | | Over specified temp. range | | | |
| | Min. | Typ. | Max. | Min. | Max. | | |
| **INTERNAL VOLTAGE REFERENCE** | | | | | | | |
| Output voltage | | 2.58 | | | | V | |
| Output voltage tolerance | | | ±3 | | | % | |
| Slope impedance | | 0.5 | 2 | | | Ω | |
| Reference current | 0.75 | | 5.2 | 0.75 | 5.2 | mA | |
| Output voltage temperature coefficient | | 70 | | | | ppm/°C | |
| **CLOCK** | | | | | | | |
| Maximum on-chip clock frequency | | 1.0 | | | | MHz | $C_{CK}$ = 220pF typ. (Fig.7) |
| Clock frequency temperature coefficient | | -0.125 | | | | %/°C | |
| Maximum external clock frequency | 1.0 | | | 1.0 | | MHz | |
| Clock pulse width | 250 | | | | | ns | |
| High level I/P voltage $V_{IH}$ | 3.5 | | | 3.5 | | V | |
| Low level I/P voltage $V_{IL}$ | | | 0.8 | | 0.8 | V | |
| High level I/P current $I_{IH}$ | | 750 | | | | μA | $V_{CC}$ = +5.5V, $V_{IN}$ = +3.5V |
| Low level I/P current $I_{IL}$ | | -880 | | | | μA | $V_{CC}$ = +5.5V, $V_{IN}$ = 0.8V |
| Supply rejection | | 3.0 | | | | %/V | |
| **LOGIC $\overline{RD}$ INPUT** | | | | | | | |
| High level I/P voltage $V_{IH}$ | 2.4 | | | 2.4 | | V | |
| Low level I/P voltage $V_{IL}$ | | | 0.8 | | 0.8 | V | |
| High level I/P current $I_{IH}$ | | 350 | | | | μA | $V_{CC}$ = +5.5V, $V_{IN}$ = +5.5V |
| | | 90 | | | | μA | $V_{CC}$ = +5.5V, $V_{IN}$ = +2.4V |
| Low level I/P current $I_{IL}$ | | -80 | | | | μA | $V_{CC}$ = +5.5V, $V_{IN}$ = +0.4V |
| **LOGIC $\overline{WR}$ INPUT** | | | | | | | |
| High level I/P voltage $V_{IH}$ | 2.4 | | | 2.4 | | V | |
| Low level I/P voltage $V_{IL}$ | | | 0.8 | | 0.8 | V | |
| High level I/P current $I_{IH}$ | | 160 | | | | μA | $V_{CC}$ = +5.5V, $V_{IN}$ = +5.5V |
| | | 40 | | | | μA | $V_{CC}$ = +5.5V, $V_{IN}$ = +2.4V |
| Low level I/P current $I_{IL}$ | | -25 | | | | μA | $V_{CC}$ = +5.5V, $V_{IN}$ = +0.4V |

## ORDERING INFORMATION

Operating temperature, all variants = –40°C to +85°C

| Device type | Number of analog inputs | Linearity error (LSB) | Package |
|---|---|---|---|
| **ZN682D** | 2 | ±0.5 | MP20 |
| **ZN682E** | 2 | ±0.5 | DP20 |
| **ZN683D** | 2 | ±1.0 | MP20 |
| **ZN683E** | 2 | ±1.0 | DP20 |
| **ZN684D** | 4 | ±0.5 | MP24 |
| **ZN684E** | 4 | ±0.5 | DP24 |
| **ZN685D** | 4 | ±1.0 | MP24 |
| **ZN685E** | 4 | ±1.0 | DP24 |
| **ZN688D** | 8 | ±0.5 | MP28 |
| **ZN688E** | 8 | ±0.5 | DP28 |
| **ZN689D** | 8 | ±1.0 | MP28 |
| **ZN689E** | 8 | ±1.0 | DP28 |

## ELECTRICAL CHARACTERISTICS (continued)

| Characteristic | Value | | | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | $T_{amb}$ = +25°C | | | Over specified temp. range | | | |
| | Min. | Typ. | Max. | Min. | Max. | | |
| **LOGIC ADDRESS INPUT MA0, MA1, MA2** | | | | | | | |
| High level I/P voltage $V_{IH}$ | 2.0 | | | 2.0 | | V | |
| Low level I/P voltage $V_{IL}$ | | | 0.8 | | 0.8 | V | |
| High level I/P current $I_{IH}$ | | 170 | | | | $\mu$A | $V_{CC}$ = +5.5V, $V_{IN}$ = +5.5V |
| | | 45 | | | | $\mu$A | $V_{CC}$ = +5.5V, $V_{IN}$ = +2.4V |
| Low level I/Pcurrent $I_{IL}$ | | -20 | | | | $\mu$A | $V_{CC}$ = +5.5V, $V_{IN}$ = +0.4V |
| **DATA AND STATUS OUTPUTS** | | | | | | | |
| High level O/P voltage $V_{OH}$ | 2.4 | | | 2.4 | | V | $I_{OH\ MAX}$ |
| Low level O/P voltage $V_{OL}$ | | | 0.4 | | 0.4 | V | $I_{OL\ MAX}$ |
| High level O/P current $I_{OH}$ | | | -1.2 | | | mA | |
| Low level O/Pcurrent $I_{OL}$ | | | 4.0 | | | mA | |
| Three-state disable O/P leakage current | | | 2.0 | | | $\mu$A | $V_{OUT}$ = 0.4V |
| (Data O/P only) | | | 2.0 | | | $\mu$A | $V_{OUT}$ = 2.4V |
| **TIMING INFORMATION** | | | | | | | |
| 3-state enable/disable delay times: | | | | | | | |
| $t_{E1}$ | | 65 | 80 | | 95 | ns | |
| $t_{E0}$ | | 40 | 55 | | 70 | ns | |
| $t_{D1}$ | | 50 | 65 | | 80 | ns | |
| $t_{D0}$ | | 65 | 80 | | 95 | ns | |
| Write pulse width | 50 | | | | | ns | |
| $\overline{WR}$ I/P low to Status O/P high | | 105 | 140 | | | ns | |
| Read pulse width | 80 | | | | | ns | |
| $\overline{RD}$ I/P high to Status O/P high | | 90 | 105 | | 125 | ns | |
| Address set-up time | 10 | | | | | ns | To $\overline{WR}$ high |
| Address hold time | 10 | | | | | ns | After $\overline{WR}$ high |

## GENERAL CIRCUIT DESCRIPTION

The ZN682/4/8 accepts 2/4/8 analog inputs and by using a 1/2/3 bit address can be programmed to convert on the required channel. Each channel can be converted to an 8-bit binary word using the successive approximation technique, with the word being loaded into the Result Latch. Pulsing WR low loads the address into the Address Latch and selects the appropriate channel, the Status output goes high to indicate the start of the conversion and the DAC input MSB is set.

The output of the DAC is compared to the unknown analog signal by means of the comparator. If the analog input is larger, the MSB is left set and if not the MSB is cleared. On the second clock pulse the sequence is repeated for the next most significant bit and so on until all eight bits have been compared. On the 8th negative clock edge Status goes low, indicating that the conversion is complete, and the Result Latch is updated.

Taking $\overline{RD}$ low enables the 3-state outputs, allowing the data to be read. Double buffered latches on chip allow the outputs to be enabled at any time, irrespective of the conversion status and so valid data will always be presented to the data bus. This data will be the result of the most recent conversion, therefore $\overline{RD}$ can be completely asynchronous with respect to Status.

## CONVERSION TIMING

The device will accept a low-going convert pulse ($\overline{WR}$) which can be completely asynchronous with respect to the clock and will produce valid data 8 or 9 clock pulses later, depending on the relative timing of the clock and $\overline{WR}$. Timing diagrams for a typical conversion sequence are shown in Fig.3.

The converter is cleared by taking $\overline{WR}$ low, which sets the MSB of the DAC, sets Status and resets all other bits. While $\overline{WR}$ is low, the address latches are transparent and converter operation is inhibited. The $\overline{WR}$ pulse can be as short as 50ns; however the MSB must be allowed to settle for at least 1.0$\mu$s before the MSB decision is made. To ensure the this criterion is met even with short write pulses, the conversion starts at the next negative clock edge after the positive edge of $\overline{WR}$. This ensures that the MSB is allowed to settle for at least a full clock period or 1$\mu$s at the maximum clock frequency.

The Status output goes low at the end of the conversion, indicating that new data is available. Having completed the first conversion the device will immediately begin another and will continue to convert on the channel in the address latch until a new channel is selected and conversion re-started by pulsing $\overline{WR}$ low. Note that conversion can only be inhibited by holding $\overline{WR}$ low.

The double buffering on the 3-state data outputs gives extra flexibility, allowing the $\overline{RD}$ input to operate asynchronously with repect to Status and always produce valid data. Note that $\overline{RD}$ cannot be tied low as it would prevent the Result Latches from updating at the end of the conversion.

## INTERRUPT DRIVEN MODE

The device can also be used in an interrupt driven mode by using the Status output. A $\overline{WR}$ pulse initiates a conversion, sending Status high. The high to low transition of Status, indicating the end of conversion, can be used as an interrupt signal by the microprocessor, i.e.,to inform the microprocessor that a conversion has been completed. On receiving the interrupt, the microprocessor sends an $\overline{RD}$ pulse to take in the new data. On the rising edge of the $\overline{RD}$ pulse internal logic sets the Status output high, hence removing the interrupt signal. This can be seen in Fig.3a by refering to the 'Status (with $\overline{RD}$)' waveform.

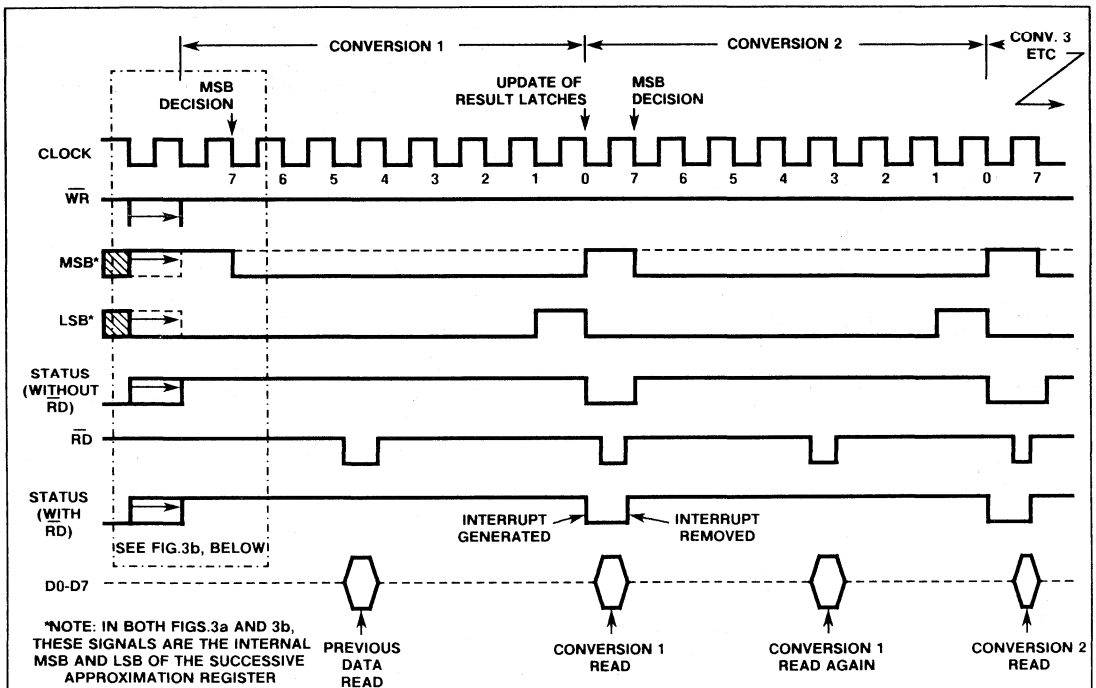



*Fig.3a Main timing diagram*

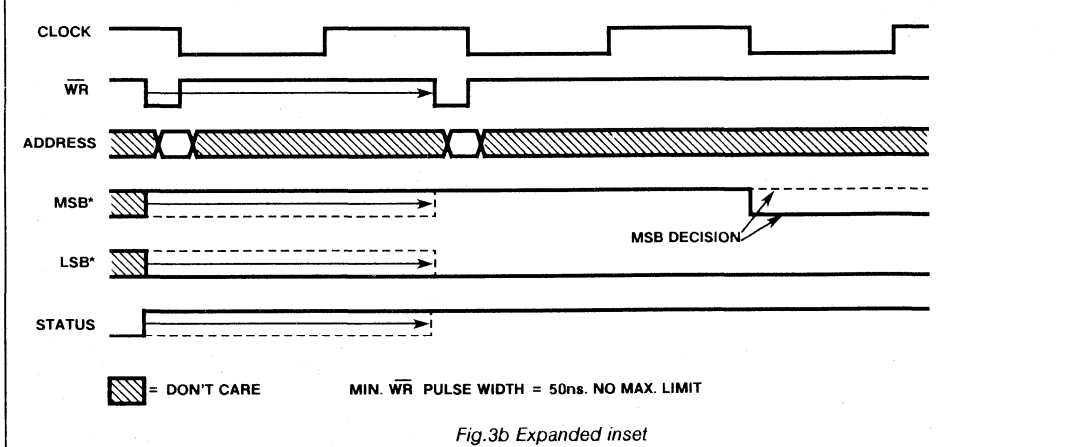



*Fig.3b Expanded inset*

*Fig.3 Timing digram*

## DATA OUTPUTS

The data outputs are provided with 3-state buffers to allow connection to a common data bus.An equivalent circuit is shown in Fig.4. While the $\overline{RD}$ input is high both output transistors are off and the device presents only a high impedance load to the bus. When $\overline{RD}$ is low the data outputs will assume the logic states present on the outputs of the double buffered register.

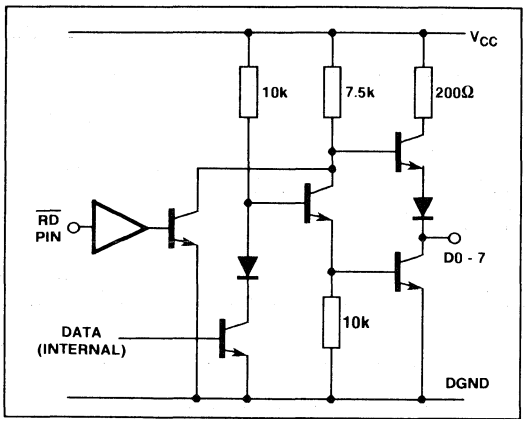



*Fig. 4 Data outputs*

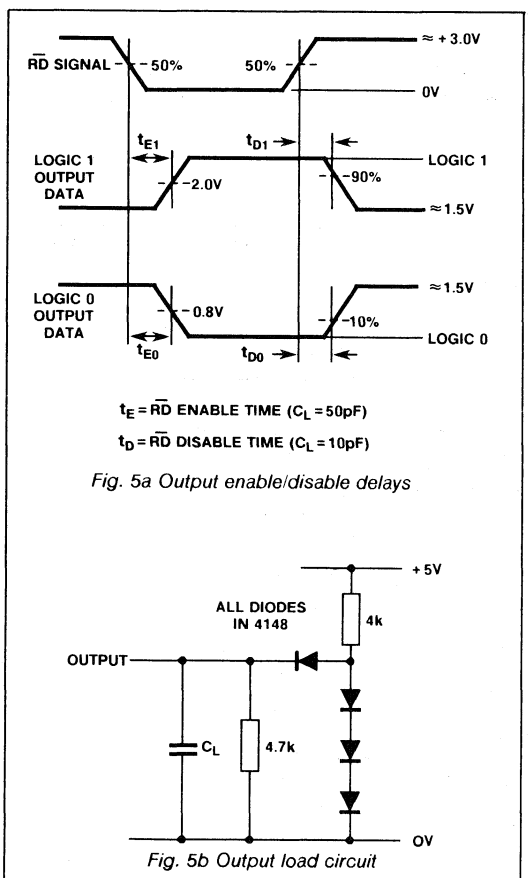



*Fig. 5a Output enable/disable delays*




*Fig. 5b Output load circuit*

A test circuit and timing diagram for the input/output delays are given in Fig.5.

The Status output uses the same active pull-up as the data outputs for CMOS/TTL compatibility.

## ON-CHIP CLOCK

The on-chip clock operates with only a single external capacitor connected between the clock pin and ground as shown in Fig.6a. A graph of typical oscillator frequency versus capacitance is given in Fig.7. The oscillator frequency may be trimmed by means of an external resistor in series with the capacitor as shown in Fig.6b. A graph of typical oscillator frequency versus resistance and capacitance is given in Fig.8. The oscillator may be overdriven with an external clock signal from a TTL or CMOS gate as shown in Fig. 6c.

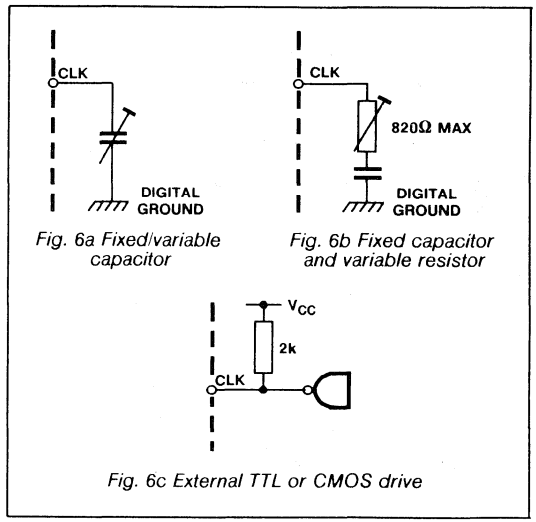



*Fig. 6a Fixed/variable capacitor*

*Fig. 6b Fixed capacitor and variable resistor*

*Fig. 6c External TTL or CMOS drive*

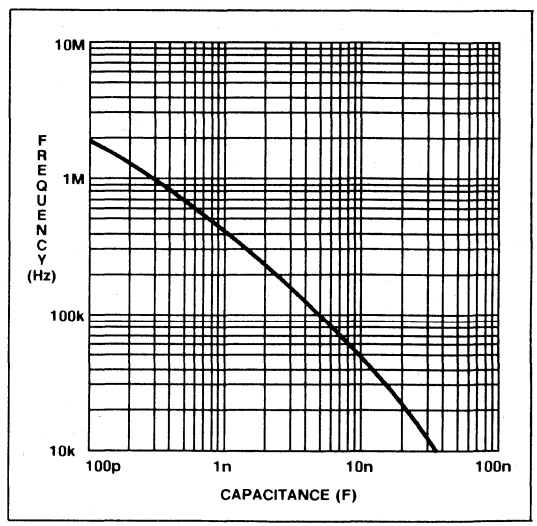



*Fig.7 Clock frequency v. capacitance*

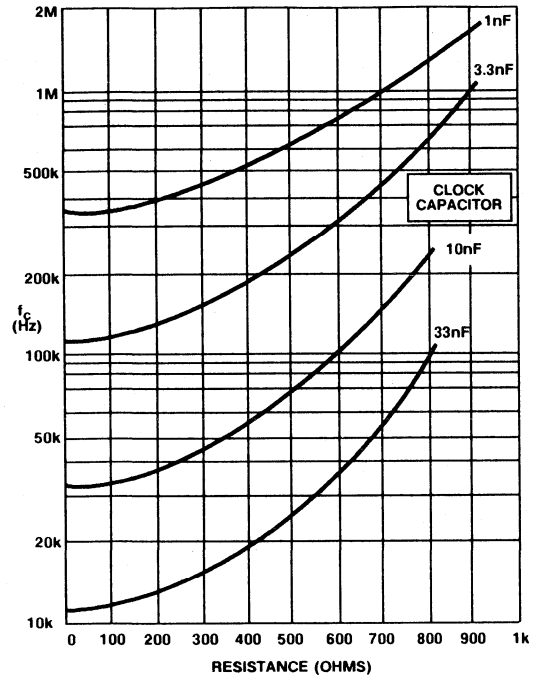



*Fig.8 Clock frequency v. resistance and capacitance*

## ANALOG CIRCUITS

### Reference

**(a) Internal reference**

The internal reference is an active bandgap circuit which is equivalent to a 2.5V Zener diode with a very low slope impedance (Fig.9). A resistor ($R_{REF}$) should be connected between $V_{CC}$ and $V_{REF\ OUT}$ and a decoupling capacitor , $C_{REF}$ (0.47$\mu$F), is required between $V_{REF\ OUT}$ and AGND. For internal reference operation, $V_{REF\ OUT}$ is connected to $V_{REF\ IN}$.

A suitable current to drive one ZN68X is nominally 2mA and will be supplied by an $R_{REF}$ of:

$$(5\text{-}2.56) / 2 \times 10^{-3} = 1.2k\Omega$$

If the reference is required to drive more than one ZN68X then the reference current can be increased e.g., an $R_{REF}$ of 470Ω will supply a nominal reference current of:

$$(5\text{-}2.56) / 470 = 5.2mA$$

and this may be used to drive up to three ZN68Xs from just one internal reference. This useful feature saves power and gives excellent gain tracking between the converters.

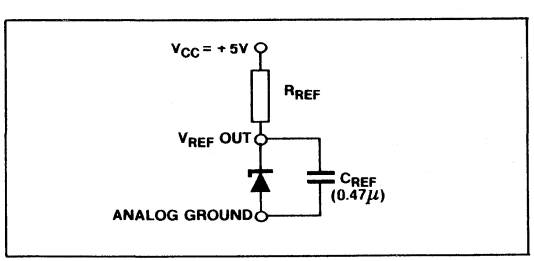



*Fig.9 Internal voltage reference*

Alternatively, with $R_{REF}$ = 680Ω the internal reference can be used as the reference voltage for other external circuits and can source or sink up to 1.5mA.

**(b) External reference**

If required, an external reference in the range +2.0V to +3.0V may be connected to $V_{REF\ IN}$. The slope resistance of such a reference should be less than 2.5Ω /n, where n is the number of converters supplied.

### Ratiometric Operation

If the output from a transducer varies with its supply then an external reference for the ZN68X should be derived from the same supply. Again, this external reference can vary from +2.0V to +3.0V.

### Analog Inputs

The equivalent circuit for each analog input is shown in Fig.10.

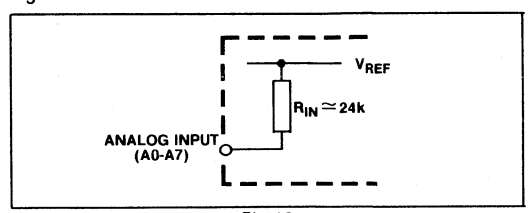



*Fig.10*

## D-A CONVERTER

The converter is of the voltage switching type and uses an R-2R ladder network as shown in Fig.11. Each element is connected to either 0V or $V_{REF\ IN}$ by by transistor voltage switches specially designed for low voltage offset (1mV typ.).

A binary weighted voltage is produced at the output of the R-2R ladder:

$$\text{DAC output} = (n/256) \times (V_{REF\ IN} - V_{OS}) + V_{OS}$$

where n is the digital input to the DAC from the successive approximation register.

$V_{OS}$ is a small offset voltage that is produced by the device supply current flowing in the package lead resistance. This offset will normally be removed by the setting up procedure and since the offset temperature coefficient is low (±7ppm/°C) the effect on accuracy will be negligible.

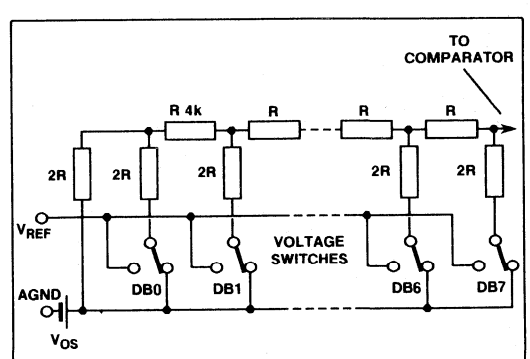



*Fig.11 R-2R ladder network*

# ZN7528

## DUAL 8-BIT MICROPROCESSOR COMPATIBLE D-A CONVERTER

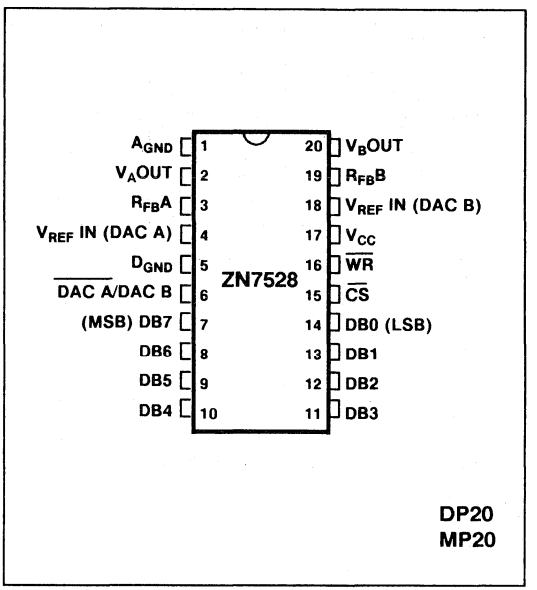
The ZN7528 is a monolithic dual 8-bit DAC designed to be easily interfaced to microprocessors, integrated on-chip are two 8-bit thin film resistor R-2R ladder networks, two data latches, input buffers, and control logic. A consequence of the two DAC's being fabricated on the same chip is excellent, inherent, DAC to DAC matching.
Operation is from 5 volts single supply and dissipates only 50mW (typ).

### FEATURES

- 800ns Voltage Settling Time
- TTL/CMOS Compatible
- Monotonic over Full Temperature Range
- Single +5V Supply
- Excellent DAC to DAC Matching
- Separate $V_{REF\ IN}$ for each DAC
- Commercial and Industrial Temperature Ranges
- Microprocessor Compatible
- Low power Consumption (50mW typ)

### APPLICATIONS

- Digital Gain/Attenuation Control
- Digital Control of Filter Parameters
- Digital Controlled Audio Circuits
- X-Y Graphics
- Robotics




*Pin connection - top view*

### ORDERING INFORMATION

**ZN7528E** (Commercial - plastic DIL package)
**ZN7528D** (Commercial - miniature plastic DIL package)

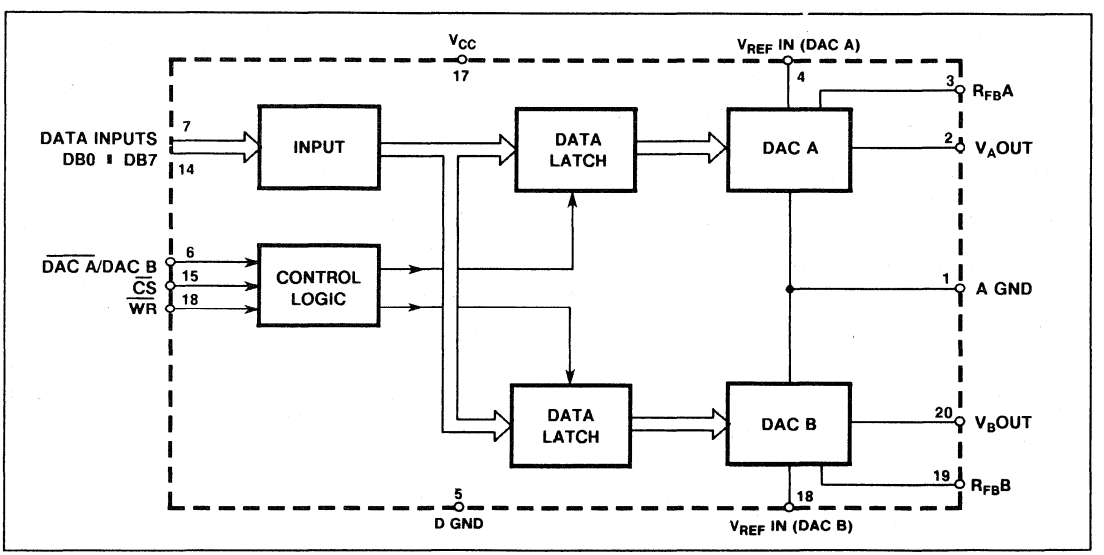



*Fig.1 ZN7528 block diagram*

# Section 2
## Voltage References

2475-1.0

# REF12Z/REF12D

## 1.26V MICROPOWER PRECISION REFERENCE

The REF12Z and REF12D are integrated circuits using the bandgap principle to provide a precise stable reference voltage of 2.5V. There are two package options available: REF12Z in a plastic 3-pin TO-92 and REF12D in a miniature surface mount package (MP8).

These references feature a recommended operating current range of 90$\mu$A to 2.5mA which make them ideal for all low power and battery applications.

### FEATURES

- Low Knee Current - typically 80 microamps
- Ideal for Battery Operation - 113 microwatts
- REF12Z - 3 lead TO-92 Plastic Package
- REF12D - Miniature Plastic Surface Mount Package (MP8)
- Tight Initial $V_{REF}$ Tolerance ± 1%
- Low Temperature Coefficient
- Low Slope Resistance
- Low Cost
- Operation over Industrial Temperature Range

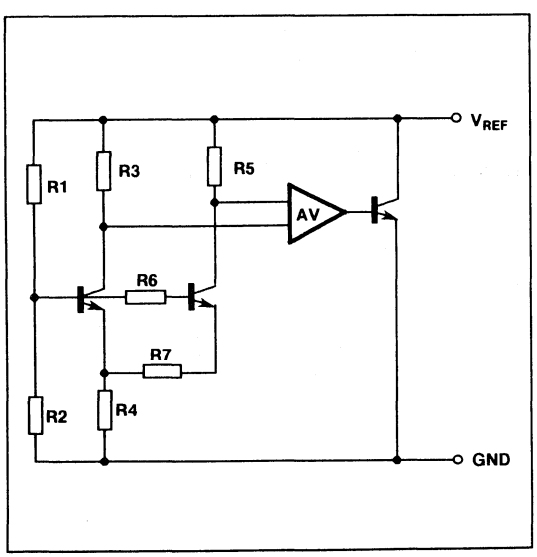



*Fig.2 Internal connections*

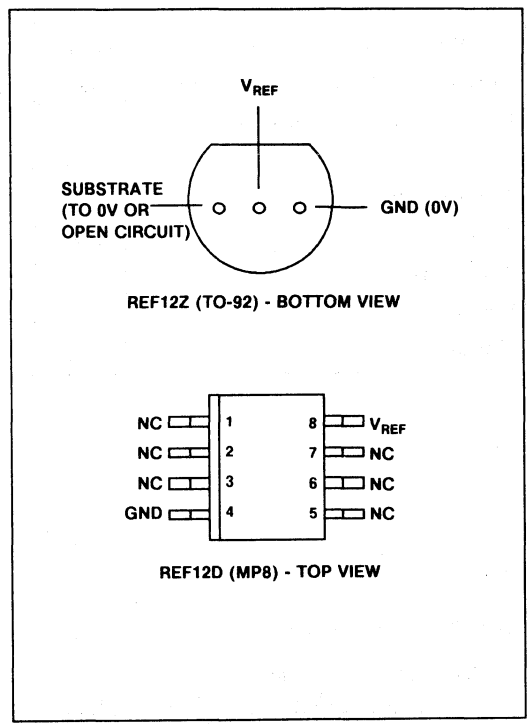



*Fig.1 Pin connections*

### ORDERING INFORMATION

| Device Type | Operating Temperature | Package |
|---|---|---|
| REF12Z | -40°C to +85°C | TO-92 |
| REF12D | -40°C to +85°C | MP8 |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 2.5mA |
| Operating temperature range : | |
| REF12Z | -40 to +85°C |
| REF12D | -40 to +85°C |
| Storage temperature | -55 to +125°C |
| Soldering temperature for a max. time of 10s: | |
| within 1.59mm of the seating plane | 300°C |
| within 0.80mm of the seating plane | 265°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**

$T_{amb}$ = 25°C, $C_S$ = 470nF (see Fig. 3)

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage | $V_{REF}$ | 1.247 | 1.26 | 1.273 | V | |
| Slope resistance (Note 1) | $R_{REF}$ | | 2.5 | 4.0 | Ω | $I_{REF}$ = 100μA to 2.5mA, Note 1 |
| Turn-on (knee) current | $I_{ON}$ | | 80 | 90 | μA | |
| Recommended operating current range | $I_{REF}$ | 0.09 | | 2.5 | mA | |
| Temperature coefficient (note 2) | TC $V_{REF}$ | | 40 | 56 | ppm/°C | REF12Z } Note 2 |
| | | | 30 | 80 | ppm/°C | REF12D } Note 2 |
| RMS noise voltage | $E_N$ | | 1.0 | | μV/√Hz | 0.1Hz to 25kHz |
| Turn-on time | $T_{ON}$ | | 0.4 | | ms | } $I_{REF}$ = 1.5mA |
| Turn-off time | $T_{OFF}$ | | 15 | | ms | } $I_{REF}$ = 1.5mA |
| Turn-on time | $T_{ON}$ | | 5 | | ms | } $I_{REF}$ = 150μA |
| Turn-off time | $T_{OFF}$ | | 110 | | ms | } $I_{REF}$ = 150μA |

NOTES

1. Slope resistance ($R_{REF}$)

   Slope resistance is defined as

   $$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over a specified current range}}{\text{The change in reference current}}$$

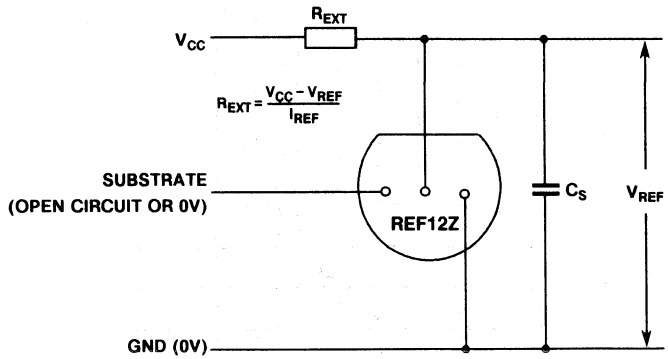
2. Reference voltage temperature coefficient (TC $V_{REF}$)

   This is the normalised reference voltage change over temperature, divided by the change in temperature. It is expressed in ppm/°C

   $$\text{TC } V_{REF} = \frac{\Delta V_{REF} \times 10^6 \text{ ppm/°C}}{V_{REF} \times \Delta T}$$

   $\Delta T$ = temperature change in °C

   $\Delta V_{REF}$ = change in reference voltage over temperature change $\Delta T$




NOTE: In order to achieve optimum operation, a stabilising capacitor ($C_S \geq 470nF$) should be connected between $V_{REF}$ and 0V as shown.

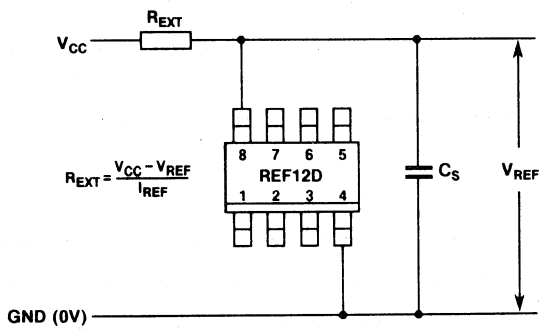
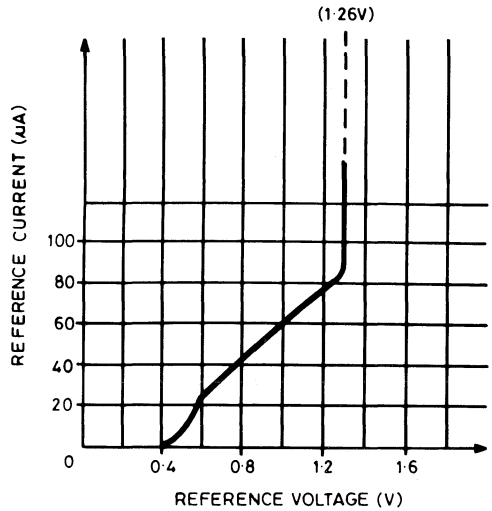
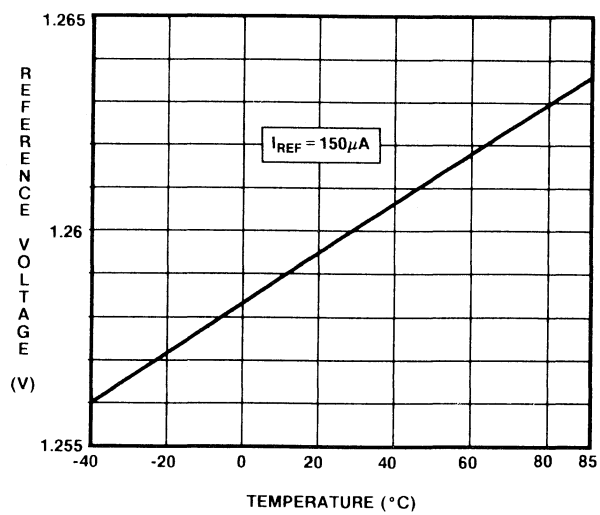


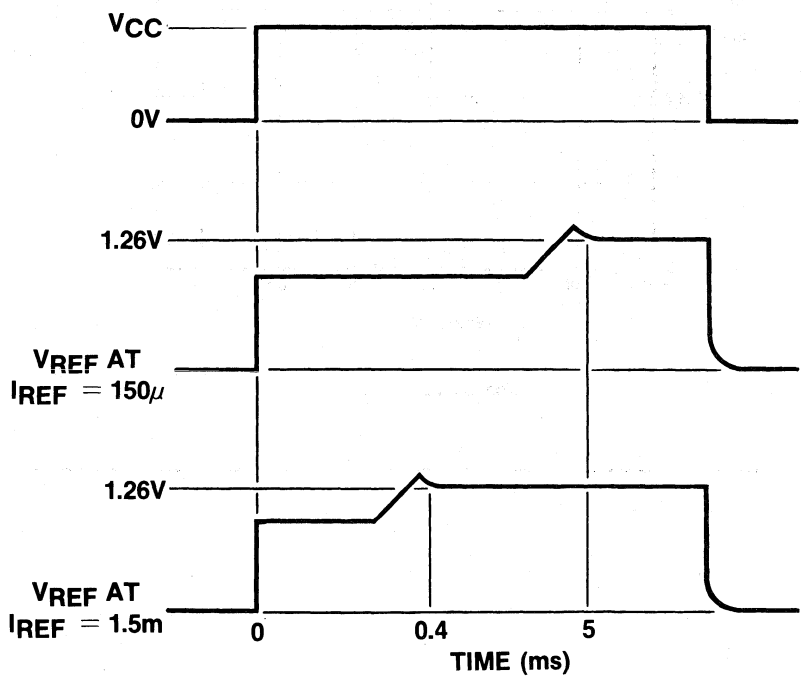

*Fig 3. Connection diagram*



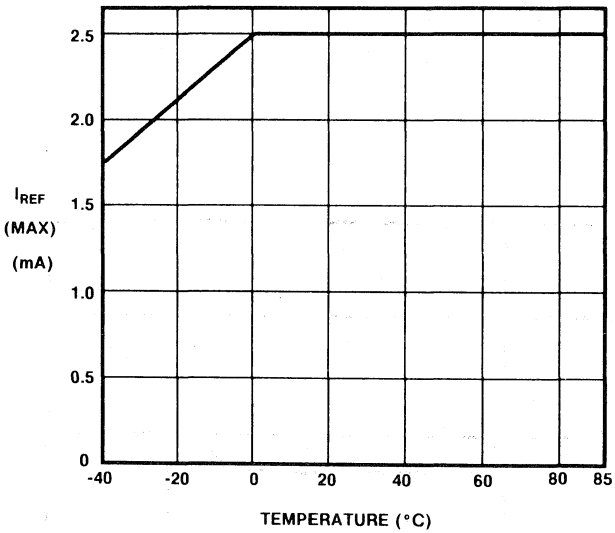

**Typical reference characteristic**




**Typical temperature characteristic**




Typical response time




Typical derating curve

# REF25Z/REF25D

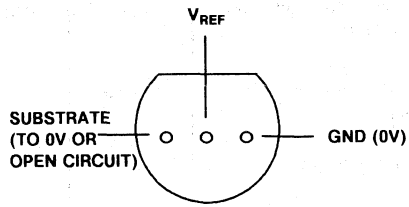
## 2.5V MICROPOWER PRECISION REFERENCE

The REF25Z and REF25D are integrated circuits using the bandgap principle to provide a precise stable reference voltage of 2.5V without the need for an external shaping capacitor. There are two package options available: REF25Z in a plastic 3-pin TO-92 and REF25D in a miniature surface mount package (MP8).

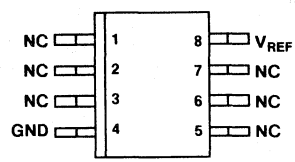
These references feature a recommended operating current range of 60$\mu$A to 5mA which make them ideal for all low power and battery applications.

### FEATURES

- Low Knee Current - typically 40 microamps
- Ideal for Battery Operation - 150 microwatts
- Internally Shaped
- REF25Z - 3 lead TO-92 Plastic Package
- REF25D - Miniature Plastic Surface Mount Package (MP8)
- Tight Initial $V_{REF}$ Tolerance ±1%
- Low Temperature Coefficient
- Low Slope Resistance
- Low Cost
- Operation over Industrial Temperature Range




REF25Z (TO-92) - BOTTOM VIEW




REF25D (MP8) - TOP VIEW

*Fig.1 Pin connections*

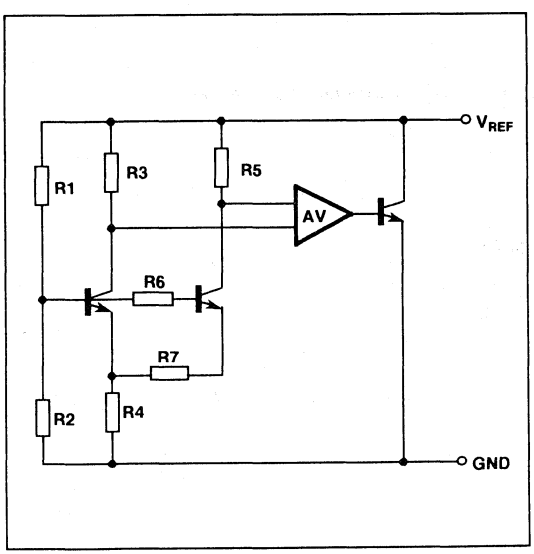



*Fig.2 Internal connections*

### ORDERING INFORMATION

| Device Type | Operating Temperature | Package |
|---|---|---|
| REF25Z | -40°C to +85°C | TO-92 |
| REF25D | -40°C to +85°C | MP8 |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 5mA |
| Operating temperature range : | |
| REF25Z | -40 to +85°C |
| REF25D | -40 to +85°C |
| Storage temperature | -55 to +125°C |
| Soldering temperature for a max. time of 10s: | |
| within 1.59mm of the seating plane | 300°C |
| within 0.80mm of the seating plane | 265°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**

$T_{amb}$ = 25°C, $I_{REF}$ = 150μA

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage | $V_{REF}$ | 2.475 | 2.500 | 2.525 | V | |
| Slope resistance (Note 1) | $R_{REF}$ | | 1.2 | 2.0 | Ω | REF25Z, $I_{REF}$ = 150μA to 5mA |
| | | | 1.2 | 2.0 | Ω | REF25D, $I_{REF}$ = 150μA to 5mA |
| Turn-on (knee) current | $I_{ON}$ | | 40 | | μA | |
| Recommended operating current range | $I_{REF}$ | 0.06 | | 5.0 | mA | |
| Temperature coefficient (Note 2) | TC $V_{REF}$ | | 35 | 110 | ppm/°C | REF25Z, Note 2 |
| | | | 35 | 80 | ppm/°C | REF25D, Note 2 |
| RMS noise voltage | $E_N$ | | 13 | | μV | 1kHz to 10kHz |
| Turn-on time | $T_{ON}$ | | 80 | | μs | |
| Turn-off time | $T_{OFF}$ | | 7 | | μs | |
| Turn-on time | $T_{ON}$ | | 65 | | μs | $I_{REF}$ = 500μA |
| Turn-off time | $T_{OFF}$ | | 2 | | μs | $I_{REF}$ = 500μA |

NOTES

1. Slope resistance ($R_{REF}$)

   Slope resistance is defined as

   $$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over a specified current range}}{\text{The change in reference current}}$$

2. Reference voltage temperature coefficient (TC $V_{REF}$)

   This is the normalised reference voltage change over temperature, divided by the change in temperature. It is expressed in ppm/°C

   $$\text{TC } V_{REF} = \frac{\Delta V_{REF} \times 10^6 \text{ ppm/°C}}{V_{REF} \times \Delta T}$$

   $\Delta T$ = temperature change in °C

   $\Delta V_{REF}$ = change in reference voltage over temperature change $\Delta T$

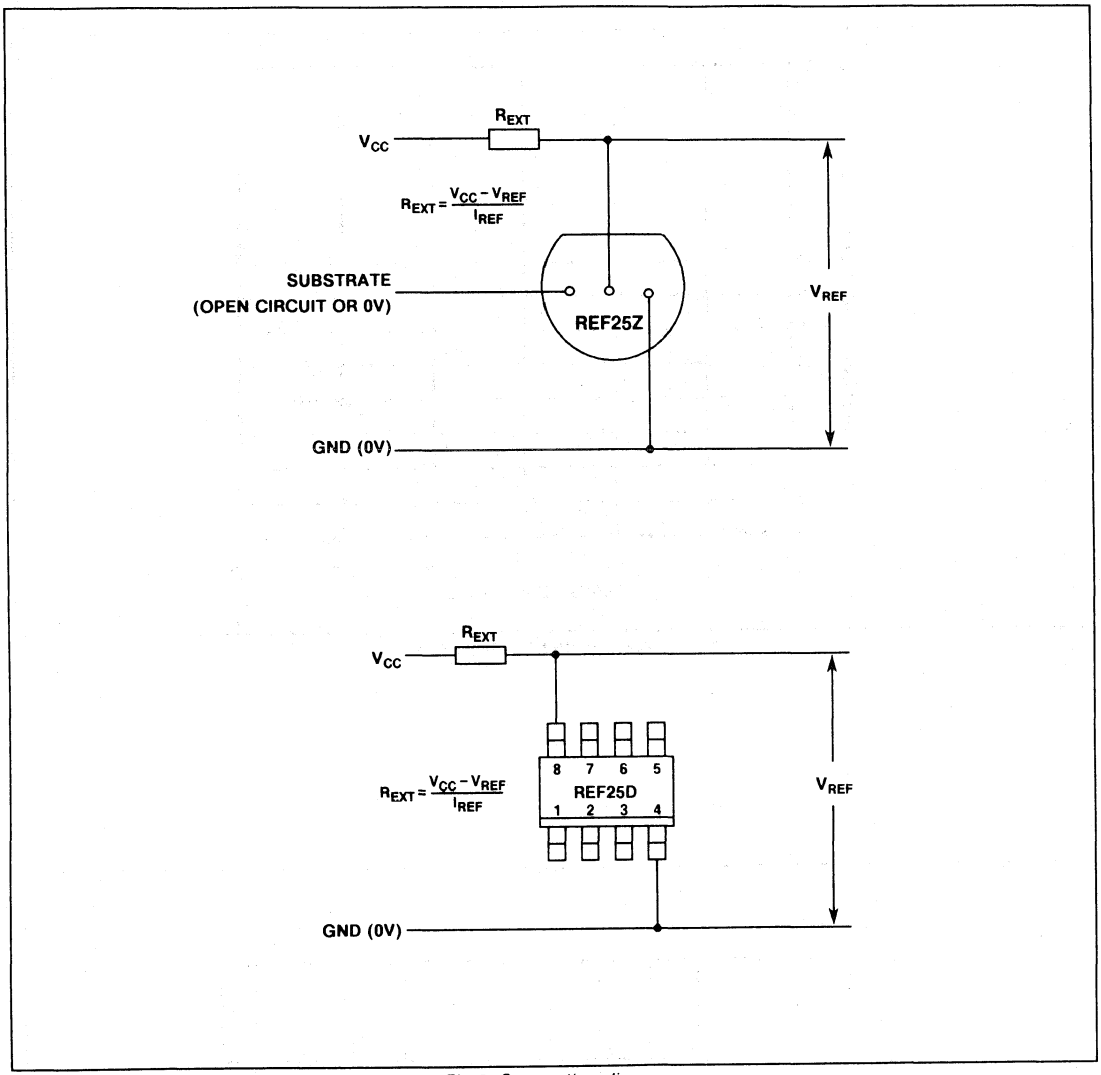



*Fig 3. Connection diagram*

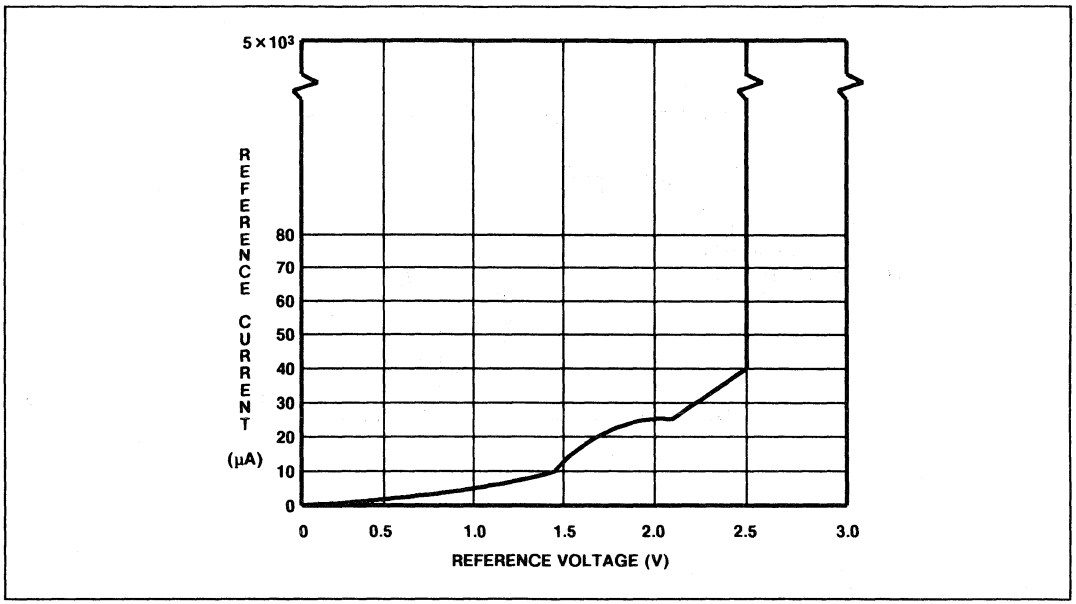



*Fig 4. Typical reference characteristic*

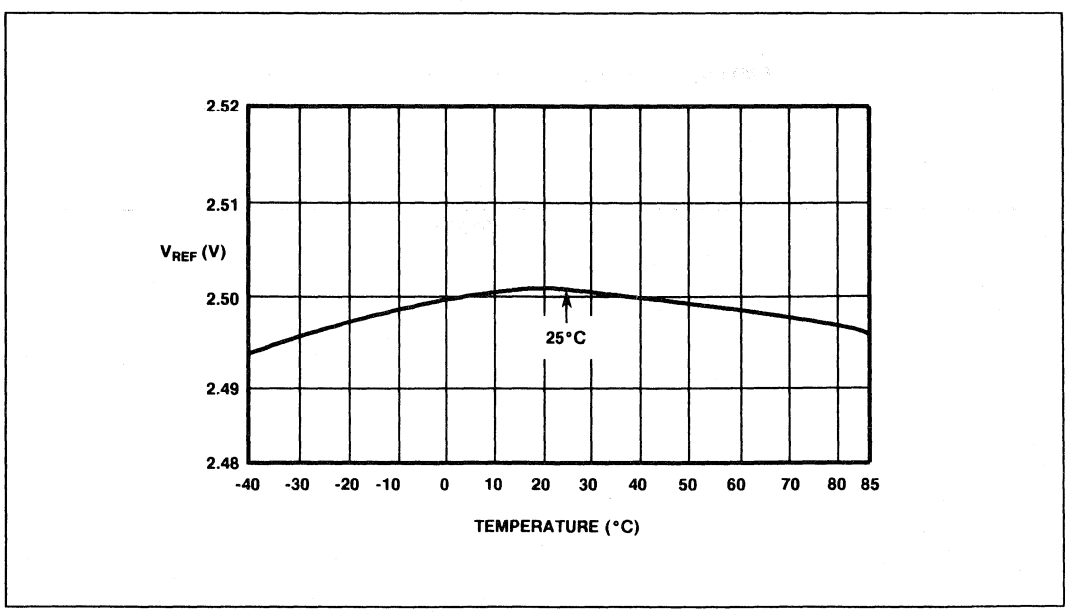



*Fig 5. Typical temperature characteristics at $I_{REF}$ = 150μA*

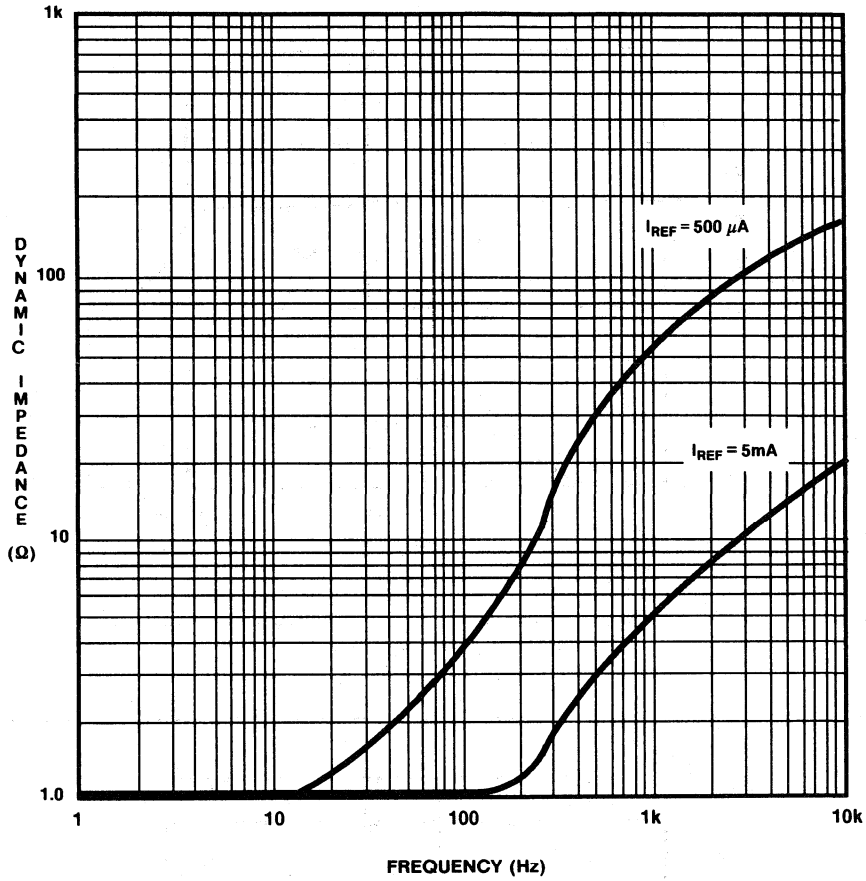



*Fig 6. Typical dynamic impedance*

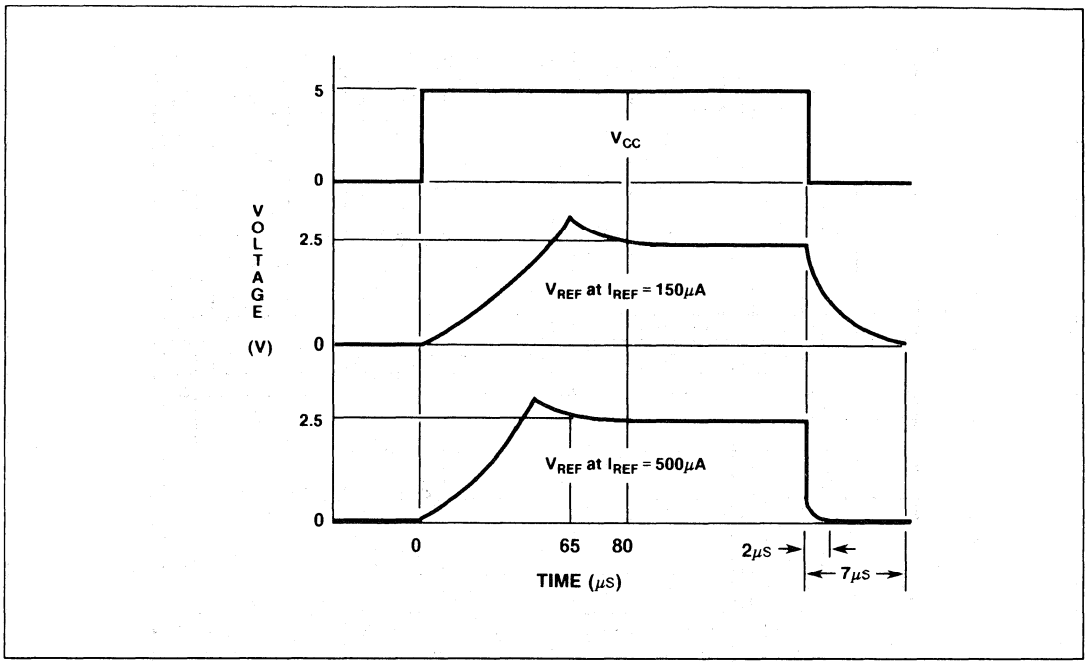



*Fig 7. Typical response time*

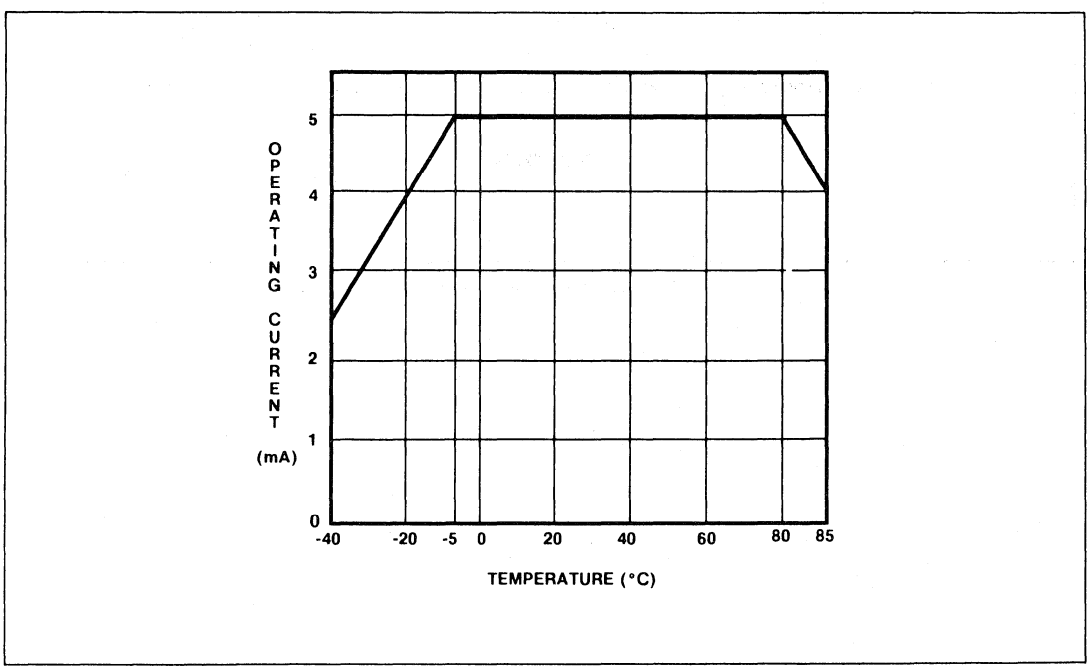



*Fig 8. Derating curve REF25Z/25D*

2383-1.0

# REF2525Z

## LOW TEMPERATURE COEFFICIENT MICROPOWER PRECISION REFERENCE

The REF2525Z is an integrated circuit using the bandgap principle to provide a precise stable reference voltage of 2.5V without the need for an external shaping capacitor. This reference features a recommended operating current range of 60$\mu$A to 5mA which makes it ideal for all low power and battery applications.

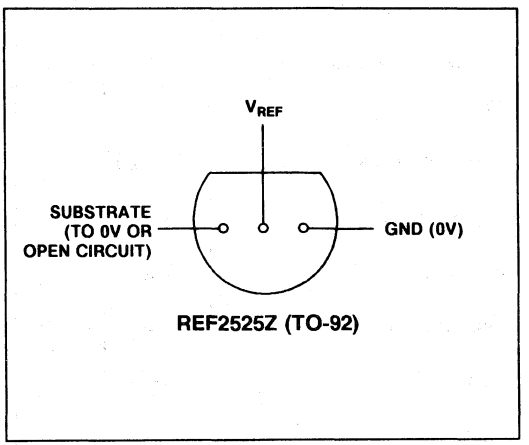



*Fig 1. Pin connections - bottom view*

### FEATURES

- Low knee current - typically 40$\mu$A
- Ideal for battery operation - 150$\mu$W
- Internally shaped
- Low temperature coefficient - 25ppm/°C max.
- Low slope resistance

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 5mA |
| Operating temperature range | -40 to +85°C |
| Storage temperature | -55 to +125°C |
| Soldering temperature for a maximum time of 10s | |
| Within 1.59mm of the seating plane | 300°C |
| Within 0.80mm of the seating plane | 265°C |

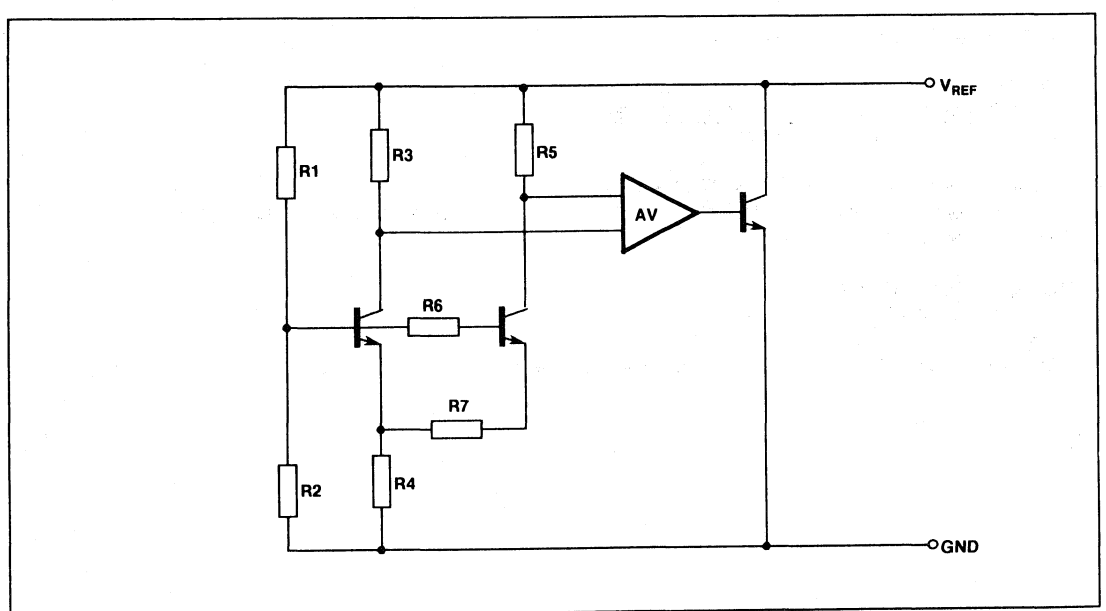



*Fig 2. Internal connections REF2525Z*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**
Temperature $T_{amb}$ = -40°C to +85°C, $I_{REF}$ = 150μA

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Output voltage | $V_{REF}$ | 2.425 | 2.500 | 2.575 | V | |
| Slope resistance (note 1) | $R_{REF}$ | | 1.2 | 2.0 | Ω | $I_{REF}$ = 150μA to 5mA |
| Turn-on (knee) current | $I_{ON}$ | | 40 | 60 | μA | |
| Recommended operating current range | $I_{REF}$ | 0.06 | | 5.0 | mA | -5°C to +80°C (See Fig.8) |
| Temperature coefficent (note 2) | (TC $V_{REF}$) | | | 25 | ppm/°C | -40°C to +85°C |
| RMS noise voltage | $E_N$ | | 13 | | μV | 1Hz to 10kHz |
| Turn-on time | $T_{ON}$ | | 80 | | μs | |
| Turn-off time | $T_{OFF}$ | | 7 | | μs | |
| Turn-on time | $T_{ON}$ | | 65 | | μs | $I_{REF}$ = 500μA |
| Turn-off time | $T_{OFF}$ | | 2 | | μs | $I_{REF}$ = 500μA |

## NOTES

1. Slope resistance ($R_{REF}$)

   Slope resistance is defined as

   $$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over a specified current range}}{\text{The change in reference current}}$$

2. Reference voltage temperature coefficient (TC $V_{REF}$)
   This is the normalised reference voltage change over temperature, divided by the change in temperature.
   It is expressed in ppm/°C

   $$TC\ V_{REF} = \frac{\Delta V_{REF} \times 10^6\ \text{ppm/°C}}{V_{REF} \times \Delta T}$$

   $\Delta T$ = temperature change in °C
   $\Delta V_{REF}$ = change in reference voltage over temperature change $\Delta T$

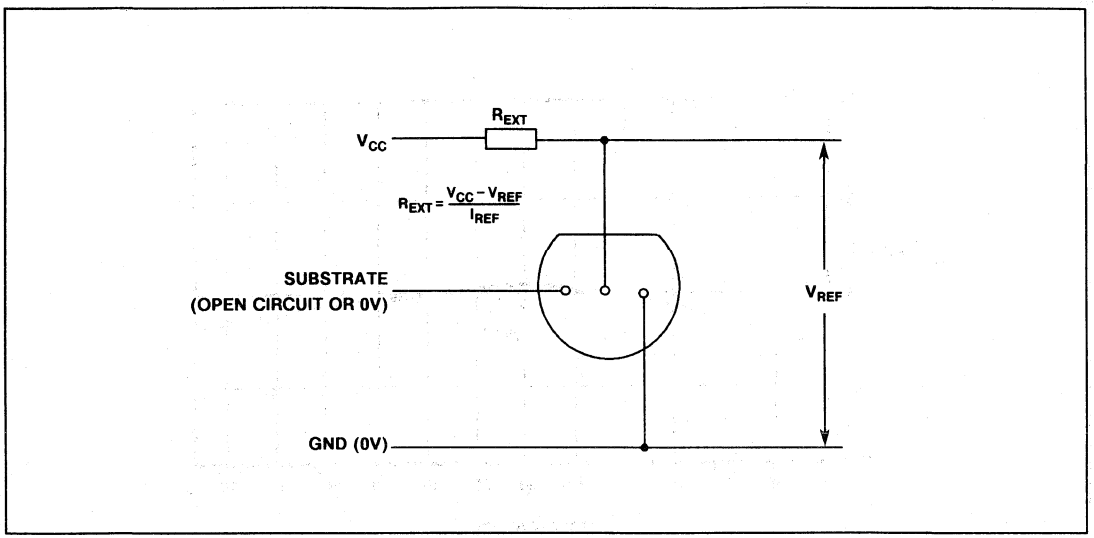



*Fig 3. Connection diagram*

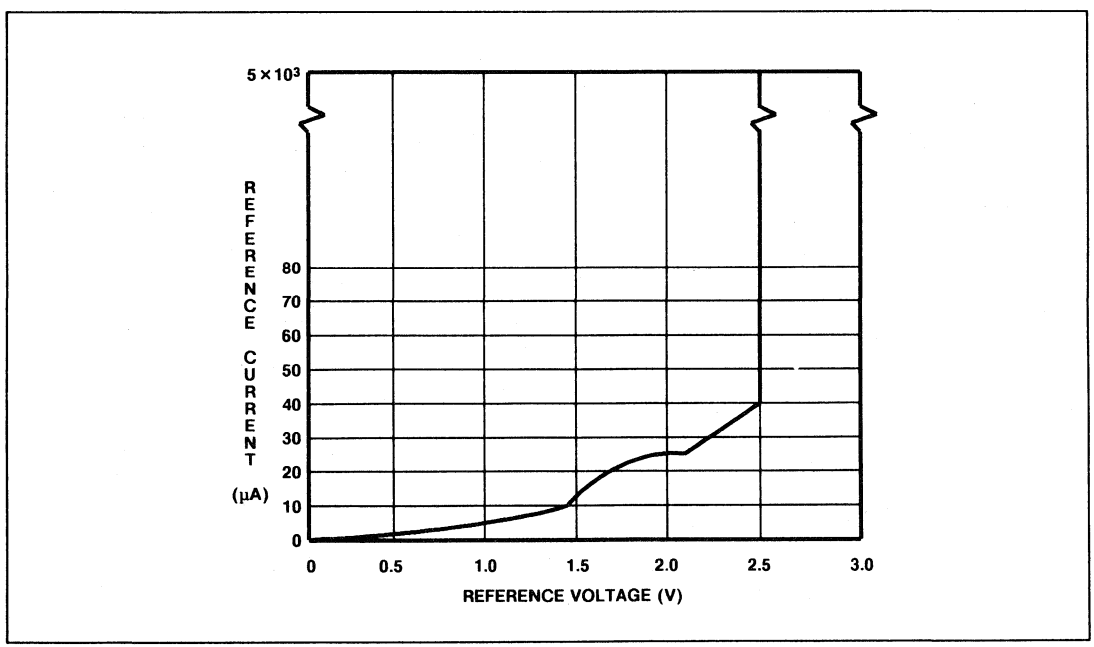



*Fig 4. Typical reference characteristic*

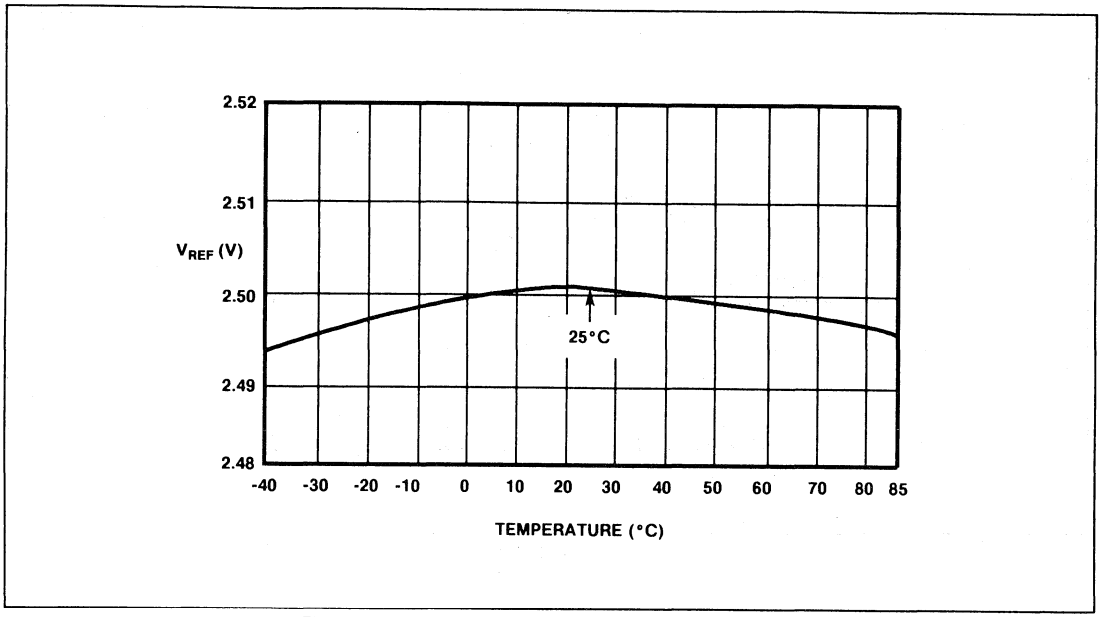



*Fig 5. Typical temperature characteristics at $I_{REF} = 150\mu A$*

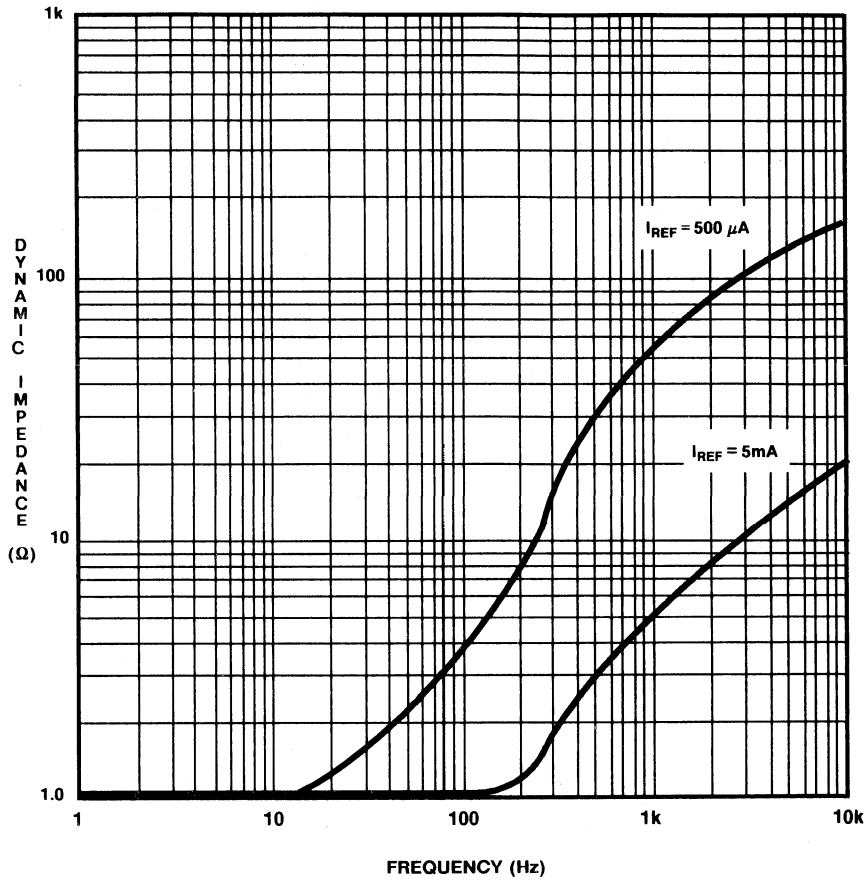



*Fig 6. Typical dynamic impedance*

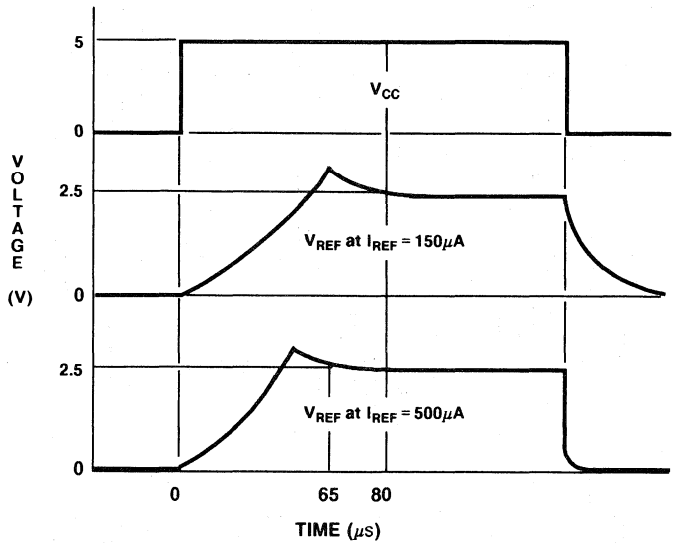



*Fig 7. Typical response time*

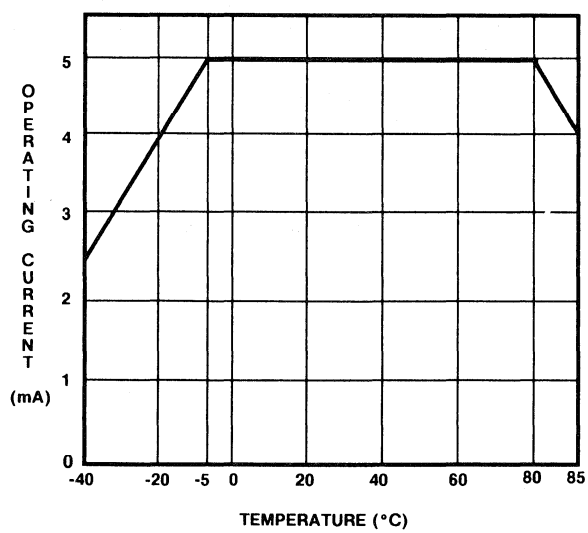



*Fig 8. Derating curve REF2525Z*

2427-1.0

# REF50Z/REF50D

## 5V MICROPOWER PRECISION REFERENCE

The REF50Z and REF50D are integrated circuits using the bandgap principle to provide a precise stable reference voltage of 5V. There are two package options available: REF50Z in a plastic 3-pin TO-92 and REF50D in a miniature surface mount package (MP8).

These references feature a recommended operating current range of 60$\mu$A to 5mA which make them ideal for all low power and battery applications.

### FEATURES

- Low Knee Current - typically 40 microamps
- Ideal for Battery Operation - 300 microwatts
- Internally Shaped
- REF50Z - 3 lead TO-92 Plastic Package
- REF50D - Miniature Plastic Surface Mount Package (MP8)
- Tight Initial $V_{REF}$ Tolerance $\pm$1%
- Low Temperature Coefficient
- Low Slope Resistance
- Low Cost
- Operation over Industrial Temperature Range

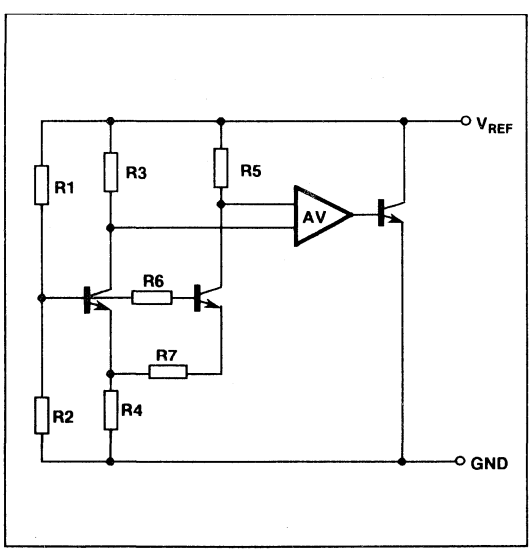



*Fig.2 Internal connections*

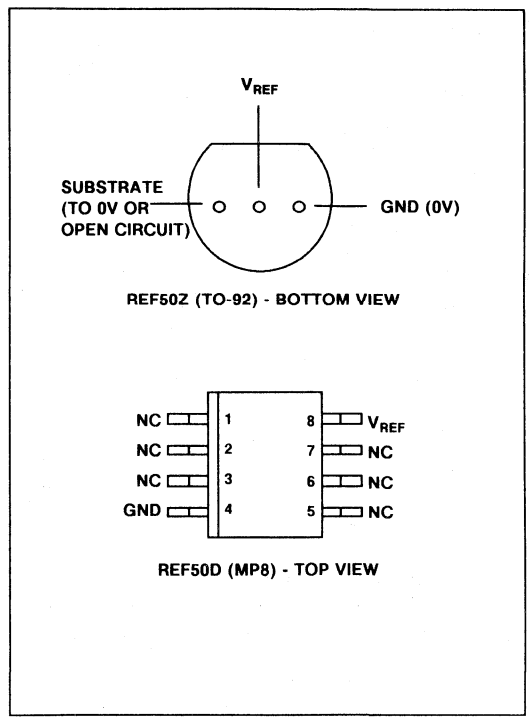



*Fig.1 Pin connections*

### ORDERING INFORMATION

| Device Type | Operating Temperature | Package |
|---|---|---|
| REF50Z | -40°C to +85°C | TO-92 |
| REF50D | -40°C to +85°C | MP8 |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 5mA |
| Operating temperature range : | |
| REF50Z | -40 to +85°C |
| REF50D | -40 to +85°C |
| Storage temperature | -55 to +125°C |
| Soldering temperature for a max. time of 10s: | |
| within 1.59mm of the seating plane | 300°C |
| within 0.80mm of the seating plane | 265°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**

$T_{amb} = 25°C$, $I_{REF} = 150\mu A$

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage | $V_{REF}$ | 4.95 | 5.00 | 5.05 | V | |
| Slope resistance (Note 1) | $R_{REF}$ | | 3.0 | 3.5 | Ω | REF50Z } $I_{REF} = 150\mu A$ to 5mA |
| | | | 3.0 | 3.5 | Ω | REF50D } |
| Turn-on (knee) current | $I_{ON}$ | | 40 | | $\mu A$ | |
| Recommended operating current range | $I_{REF}$ | 0.06 | | 5.0 | mA | |
| Temperature coefficient (Note 2) | TC $V_{REF}$ | | 35 | 110 | ppm/°C | REF25Z } Note 2 |
| | | | 35 | 80 | ppm/°C | REF25D } |
| RMS noise voltage | $E_N$ | | 13 | | $\mu V$ | 1kHz to 10kHz |
| Turn-on time | $T_{ON}$ | | 80 | | $\mu s$ | |
| Turn-off time | $T_{OFF}$ | | 7 | | $\mu s$ | |
| Turn-on time | $T_{ON}$ | | 65 | | $\mu s$ | } $I_{REF} = 500\mu A$ |
| Turn-off time | $T_{OFF}$ | | 2 | | $\mu s$ | } |

NOTES

1. Slope resistance ($R_{REF}$)

   Slope resistance is defined as

   $$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over a specified current range}}{\text{The change in reference current}}$$

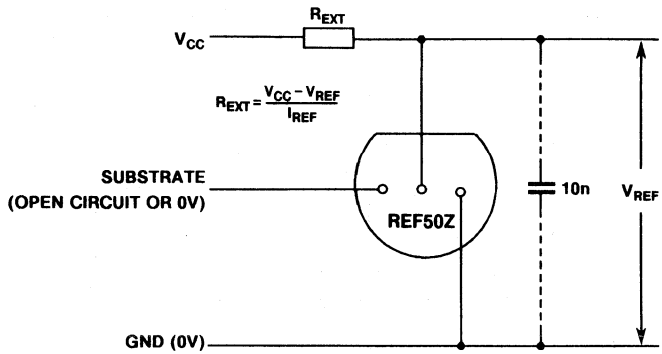
2. Reference voltage temperature coefficient (TC $V_{REF}$)

   This is the normalised reference voltage change over temperature, divided by the change in temperature. It is expressed in ppm/°C

   $$\text{TC } V_{REF} = \frac{\Delta V_{REF} \times 10^6 \text{ ppm/°C}}{V_{REF} \times \Delta T}$$

   $\Delta T$ = temperature change in °C

   $\Delta V_{REF}$ = change in reference voltage over temperature change $\Delta T$




NOTE: In some instances, in order to achieve optimum operation, a 10nF capacitor should be connected between $V_{REF}$ and 0V as shown.

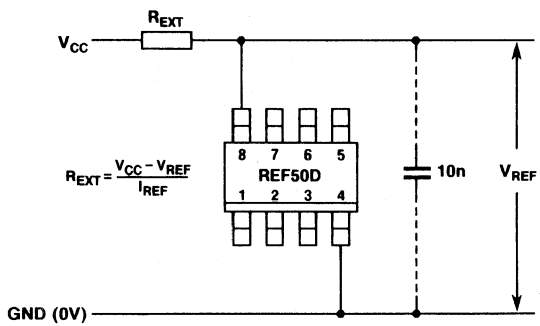



*Fig 3. Connection diagrams*

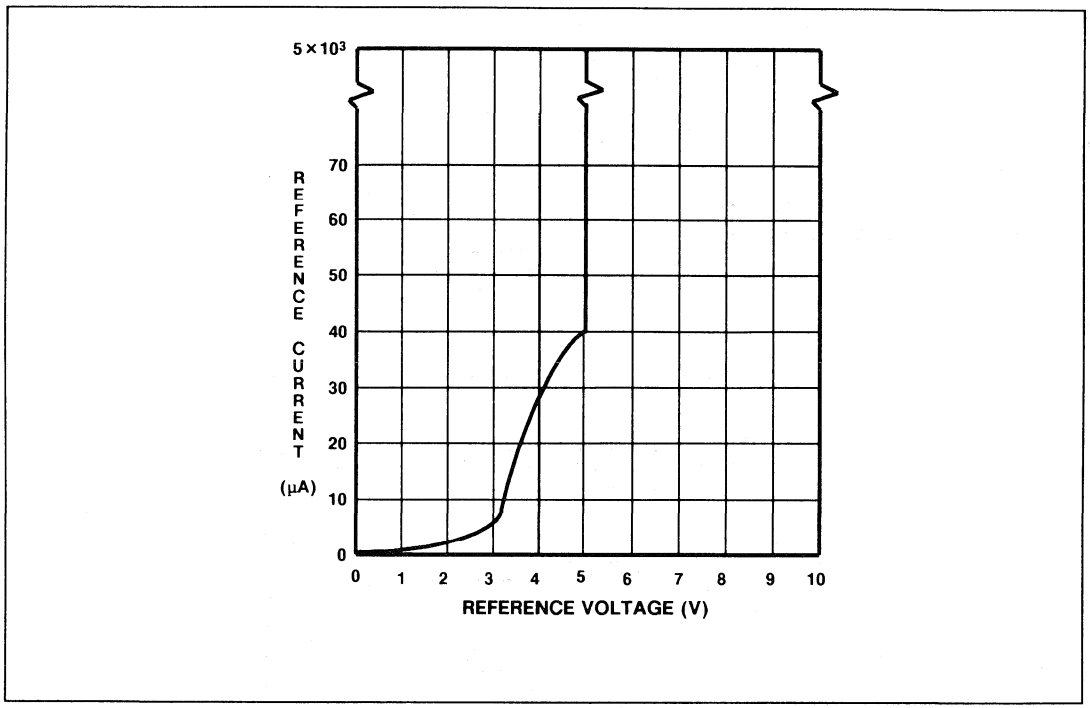



*Fig 4. Typical reference characteristic*

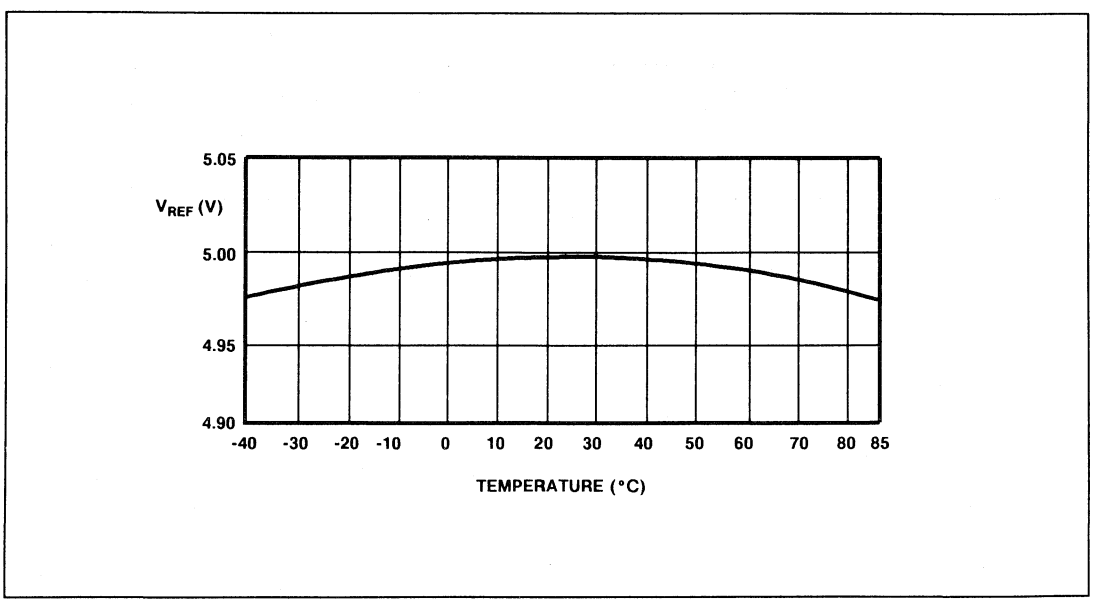



*Fig 5. Typical temperature characteristics at $I_{REF}$ = 150μA*

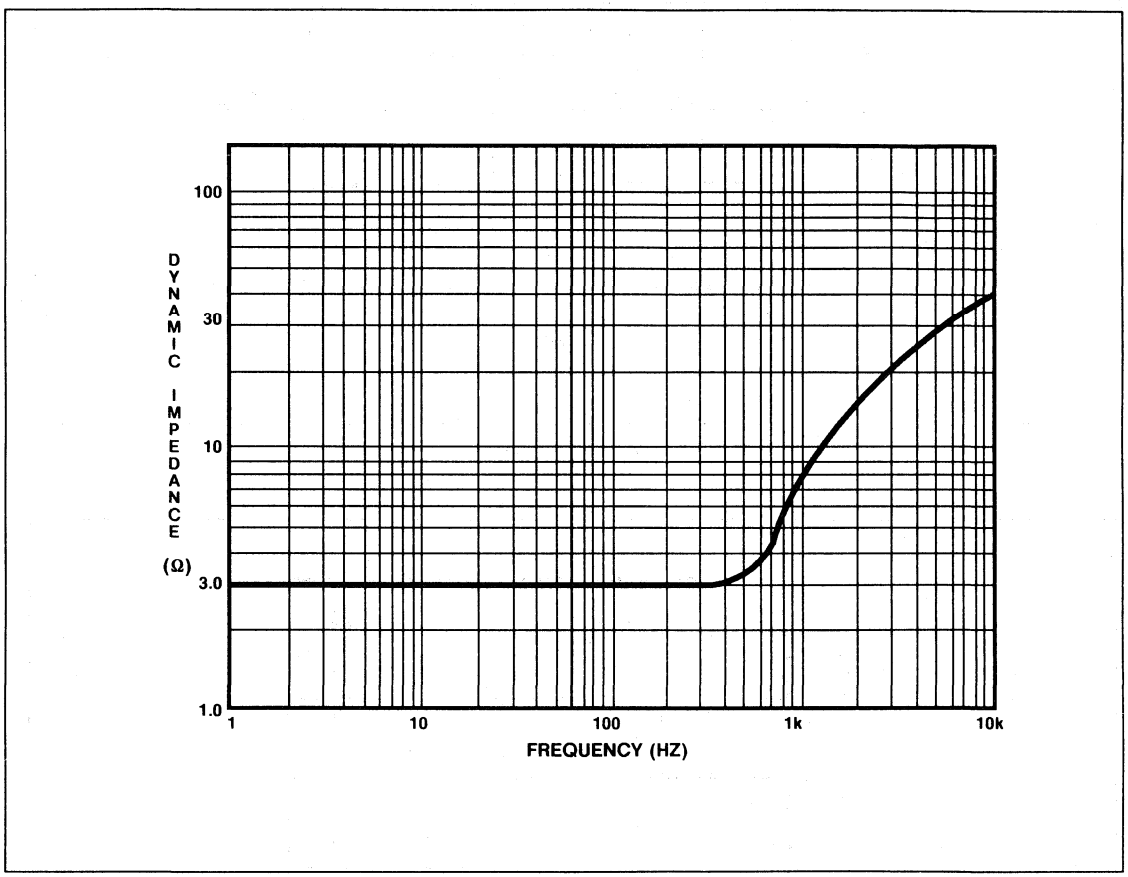



*Fig 6. Typical dynamic impedance at $I_{REF}$ = 5mA*

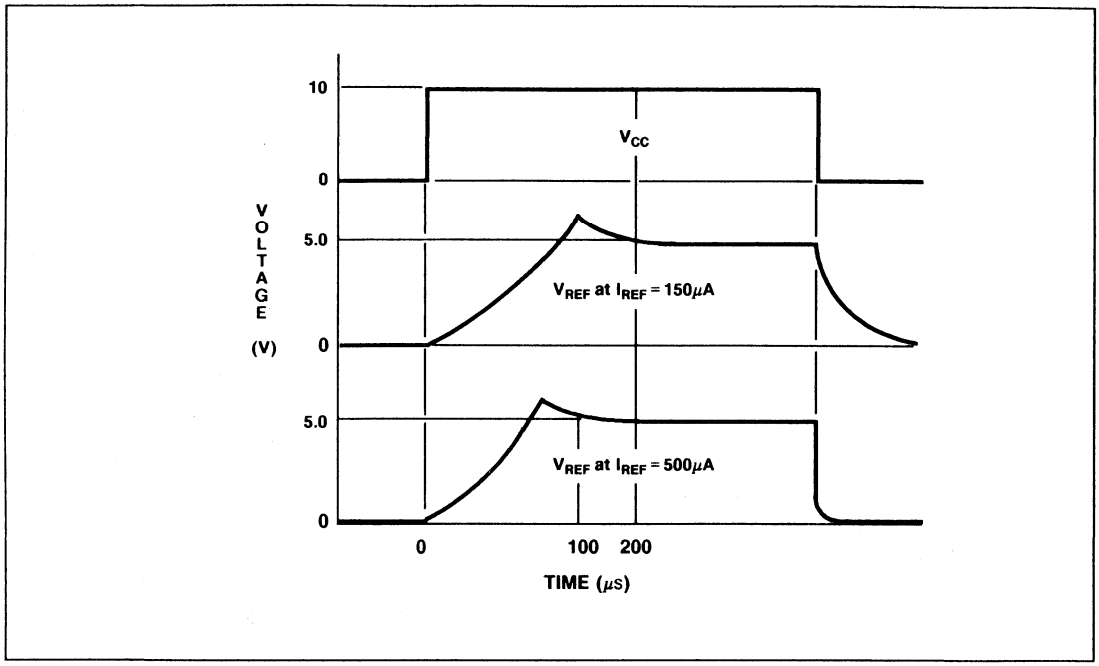



*Fig 7. Typical response time (not to scale)*

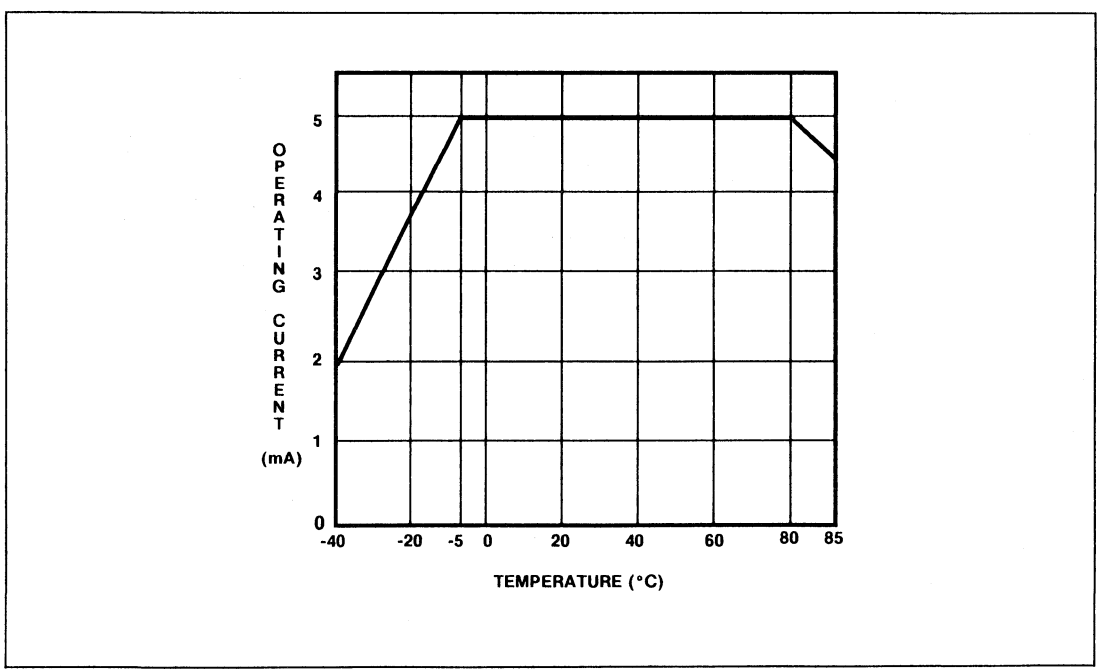



*Fig 8. Derating curve*

2442-1.0

# SR12D

## 1.2V PRECISION VOLTAGE REFERENCE

The SR12D is a monolithic integrated circuit using the bandgap principle to provide a precise reference voltage of 1.23V.

This reference device is packaged in a standard SOT-23 small outline package, making it ideal for all surface mount applications.

### FEATURES

- Standard SOT-23 Surface Mount Package
- Low Knee Current - Typically 80 $\mu$A
- Low Temperature Coefficient

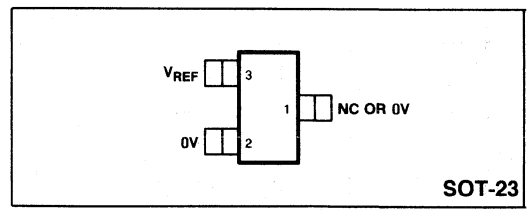



*Fig.1 Pin connections (top view)*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 2.5mA |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -55°C to +125°C |

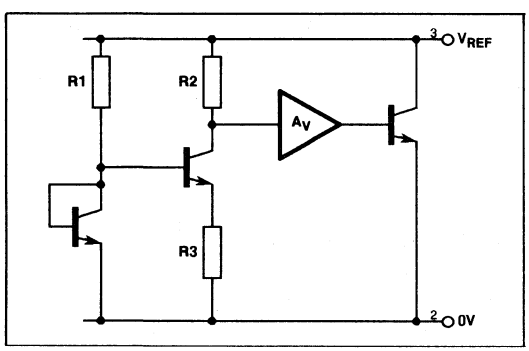



*Fig.2 SR12D circuit diagram*

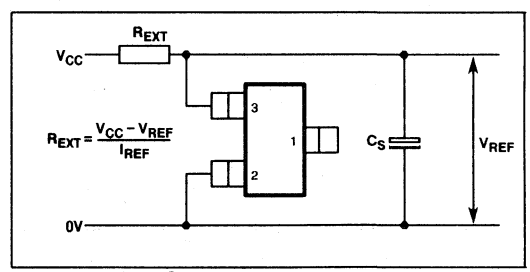



*Fig.3 SR12D external connections.*

NOTE: In order to achieve optimum operation, an electrolytic stabilising capacitor ($C_S \geq 1\mu F$) should be connected between $V_{REF}$ and 0V as shown in Fig. 3.

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = +25°C, $I_{REF}$ = 150$\mu$A, $C_S$ = 1$\mu$F

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage | $V_{REF}$ | 1.193 | 1.230 | 1.267 | V | |
| Slope resistance (see note 1) | $R_{REF}$ | | 1.5 | 2.5 | Ω | $I_{REF}$ = 150$\mu$A to 2.5mA |
| Turn-on (knee) current | $I_{ON}$ | | 80 | 90 | $\mu$A | |
| Recommended operating current range | $I_{REF}$ | 0.09 | | 2.5 | mA | |
| Temperature coefficient (see note 2) | $TCV_{REF}$ | | 40 | 125 | ppm/°C | 0°C to +70°C |
| | | | 40 | 120 | ppm/°C | –40°C to +85°C |
| RMS noise voltage | $E_N$ | | 10 | | $\mu$V | 1Hz to 25kHz |
| Turn on time | $t_{ON}$ | | 7 | | ms | |
| Turn off time | $t_{OFF}$ | | 24 | | ms | |
| Turn on time | $t_{ON}$ | | 0.4 | | ms | } $I_{REF}$ = 5mA |
| Turn off time | $t_{OFF}$ | | 1.8 | | ms | |

## NOTES

### 1. Slope Resistance ($R_{REF}$)

The slope resistance is defined as

$$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over specified current range}}{\text{The change in reference current}}$$

### 2. Reference Voltage Temperature Coefficient ($TCV_{REF}$)

This is the normalised reference voltage change over temperature, divided by the change in temperature. It is expressed in ppm/°C as follows

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

$\Delta T$ = temperature change in °C

$\Delta V_{REF}$ = change in reference voltage over temperature change $\Delta T$.

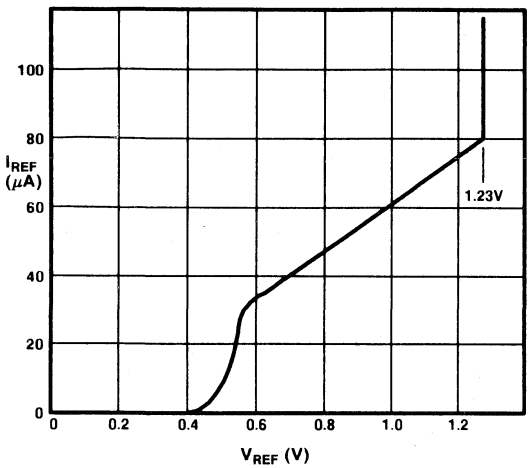



*Fig.4 Typical reference characteristic*

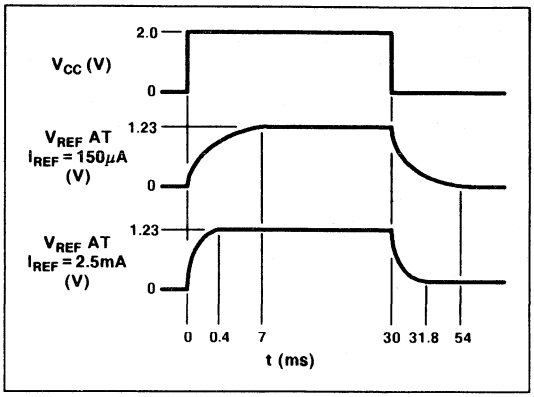



*Fig.5 SR12D typical response time (not to scale)*

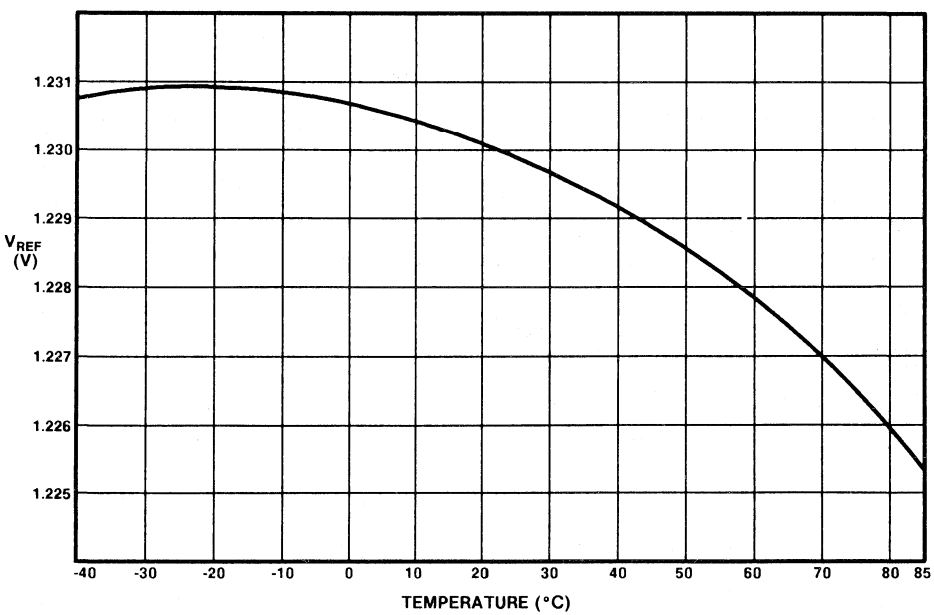



*Fig.6 Typical temperature characteristic of SR12D at $I_{REF}$ = 150$\mu$A*

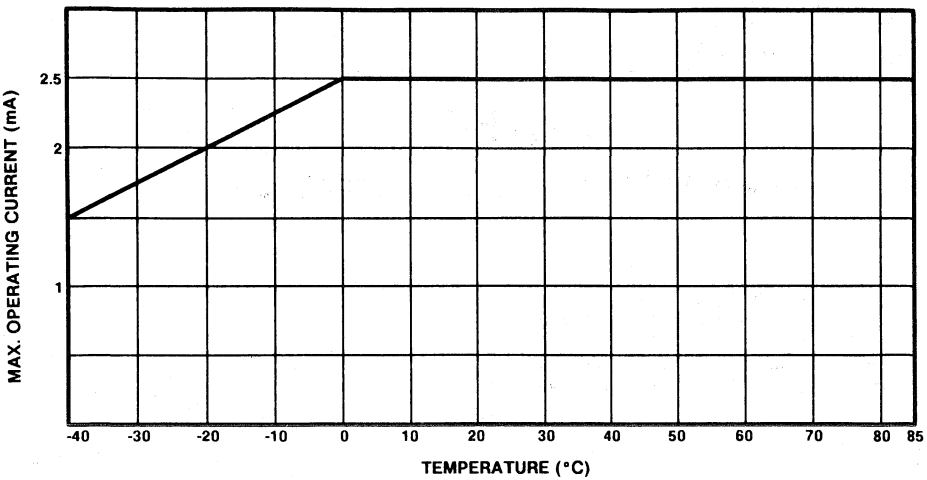



*Fig.7 Derating curve*

2443-1.0

# SR25D

## 2.5V PRECISION VOLTAGE REFERENCE

The SR25D is a monolithic integrated circuit using the bandgap principle to provide a precise reference voltage of 2.5V.

This reference device is packaged in a standard SOT-23 small outline package, making it ideal for all surface mount applications.

### FEATURES

- Standard SOT-23 Surface Mount Package
- Low Knee Current - Typically 60 $\mu$A
- Low Temperature Coefficient

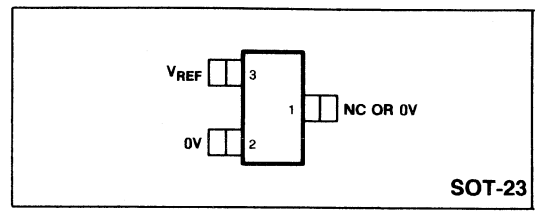



*Fig.1 Pin connections (top view)*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 5mA |
| Operating temperature range | 0°C to +70°C |
| Storage temperature range | -55°C to +125°C |

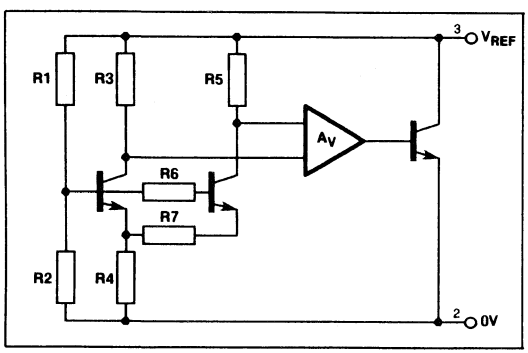



*Fig.2 SR25D circuit diagram*

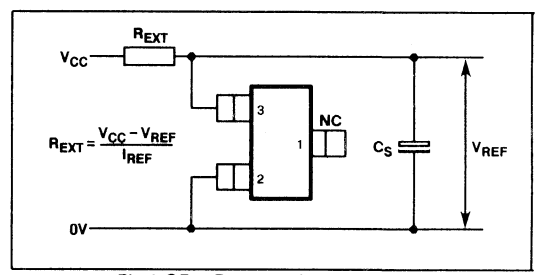



*Fig.3 SR25D external connections.*

NOTE: In order to achieve optimum operation, an electrolytic stabilising capacitor, $C_S$, (see Fig. 9) should be connected between $V_{REF}$ and 0V as shown in Fig. 3.

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{amb}$ = +25°C, $I_{REF}$ = 150$\mu$A, $C_S$ = 1$\mu$F

| Characteristic | Symbol | Value | | | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Output voltage | $V_{REF}$ | 2.425 | 2.50 | 2.575 | V | | |
| Slope resistance | $R_{REF}$ | | 1.2 | 2.0 | Ω | $I_{REF}$ = 150$\mu$A to 5mA | 1 |
| Turn-on (knee) current | $I_{ON}$ | | 60 | 80 | $\mu$A | | 3 |
| Recommended operating current range | $I_{REF}$ | 0.08 | | 5 | mA | | 3 |
| Temperature coefficient | $TCV_{REF}$ | | 40 | 150 | ppm/°C | 0°C to +70°C | 2&3 |
| RMS noise voltage | $E_N$ | | 18 | | $\mu$V | | 3 |
| Turn on time | $t_{ON}$ | | 12.5 | | ms | | 3 |
| Turn off time | $t_{OFF}$ | | 45 | | ms | | 3 |
| Turn on time | $t_{ON}$ | | 0.4 | | ms | } $I_{REF}$ = 5mA | 3 |
| Turn off time | $t_{OFF}$ | | 1.5 | | ms | | 3 |

## NOTES

**1. Slope Resistance ($R_{REF}$)**

The slope resistance is defined as

$$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over specified current range}}{\text{The change in reference current}}$$

**2. Reference Voltage Temperature Coefficient ($TCV_{REF}$)**

This is the normalised reference voltage change over temperature, divided by the change in temperature. It is expressed in ppm/°C as follows

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

$\Delta T$ = temperature change in °C

$\Delta V_{REF}$ = change in reference voltage over temperature change $\Delta T$.

**3. Guaranteed but not tested**

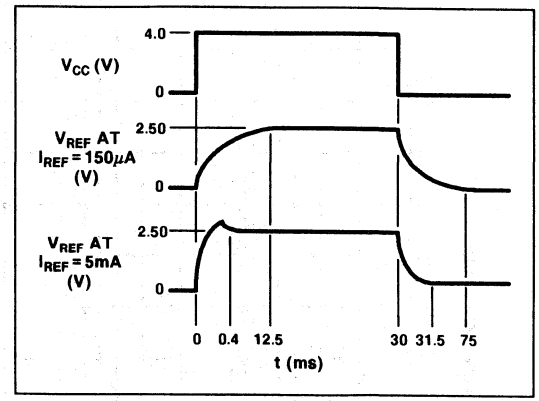



*Fig.5 SR25D typical response time (not to scale)*

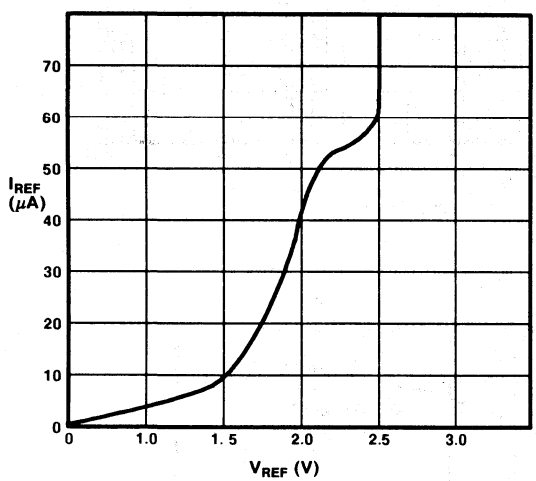



*Fig.4 Typical reference characteristic*

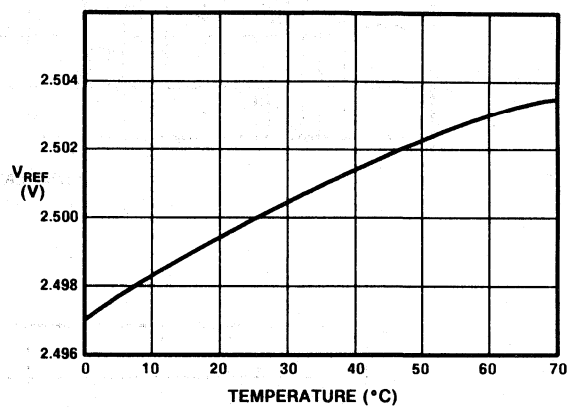



*Fig.6 Typical temperature characteristic of SR25D at $I_{REF}$ = 150μA*

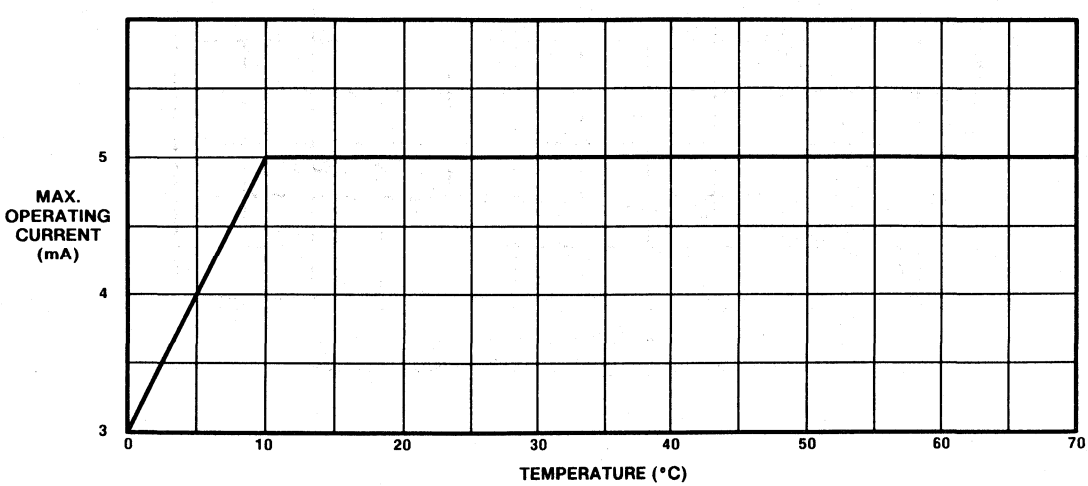



*Fig.7 Derating curve*

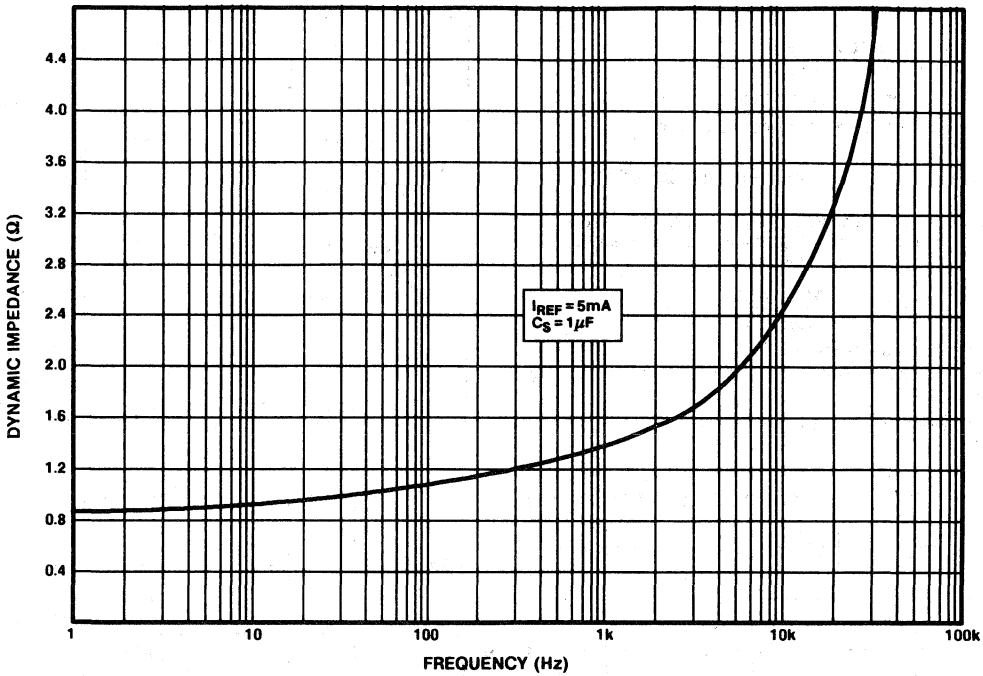



*Fig.8 Typical dynamic impedance of SR25D*

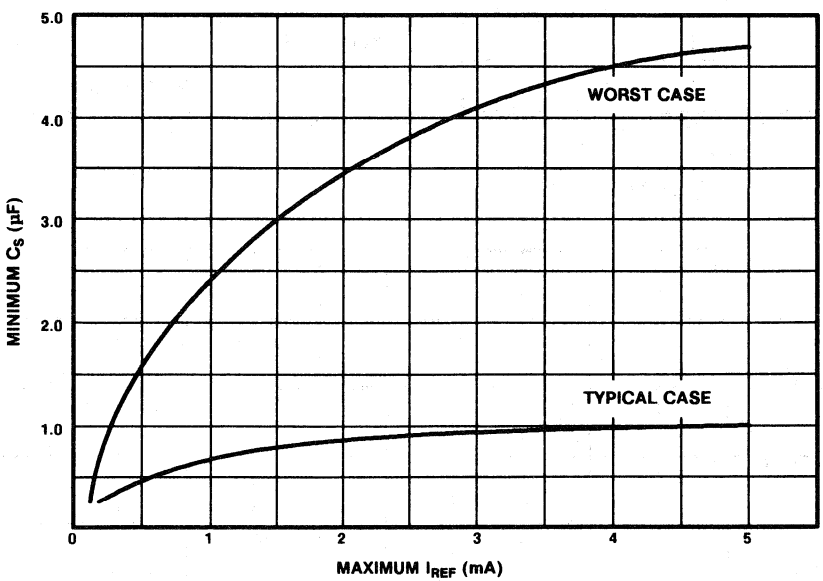



*Fig.9 Stabilising capacitor required for optimum operation*

# SR50D

## 5V PRECISION VOLTAGE REFERENCE

The SR50D is a monolithic integrated circuit using the bandgap principle to provide a precise reference voltage of 5V.

This reference device is packaged in a standard SOT-23 small outline package, making it ideal for all surface mount applications.

### FEATURES

- Standard SOT-23 Surface Mount Package
- Low Knee Current - Typically 75 $\mu$A
- Low Temperature Coefficient

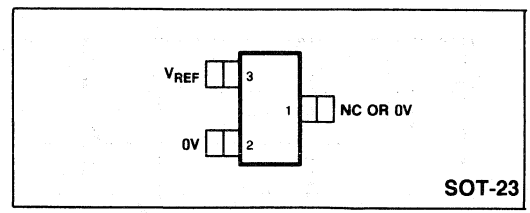



*Fig.1 Pin connections (top view)*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 5mA |
| Operating temperature range | -40°C to +85°C |
| Storage temperature range | -55°C to +125°C |

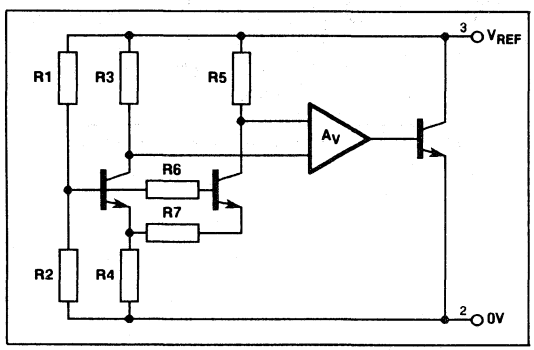



*Fig.2 SR50D circuit diagram*

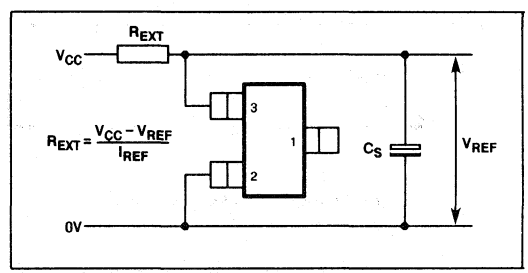



*Fig.3 SR50D external connections.*

NOTE: In order to achieve optimum operation, an electrolytic capacitor, $C_S$, (see Fig. 9) should be connected between $V_{REF}$ and 0V as shown in Fig. 3.

### ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
$T_{amb}$ = +25°C, $I_{REF}$ = 150$\mu$A, $C_S$ = 1$\mu$F

| Characteristic | Symbol | Value | | | Units | Conditions | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Output voltage | $V_{REF}$ | 4.850 | 5.000 | 5.150 | V | | |
| Slope resistance | $R_{REF}$ | | 0.9 | 2.0 | Ω | $I_{REF}$ = 150$\mu$A to 5mA | 1 |
| Turn-on (knee) current | $I_{ON}$ | | 75 | 80 | $\mu$A | | 3 |
| Recommended operating current range | $I_{REF}$ | 0.080 | | 5 | mA | | 3 |
| Temperature coefficient | $TCV_{REF}$ | | 79 | 220 | ppm/°C | 0°C to +70°C | 2&3 |
| | | | 89 | 220 | ppm/°C | -40°C to +85°C | |
| RMS noise voltage | $E_N$ | | 25 | | $\mu$V | 1Hz to 25kHz | 3 |
| Turn on time | $t_{ON}$ | | 34 | | ms | | 3 |
| Turn off time | $t_{OFF}$ | | 120 | | ms | | 3 |
| Turn on time | $t_{ON}$ | | 0.8 | | ms | } $I_{REF}$ = 5mA | 3 |
| Turn off time | $t_{OFF}$ | | 8.4 | | ms | | 3 |

## NOTES

### 1. Slope Resistance ($R_{REF}$)

The slope resistance is defined as

$$R_{REF} = \frac{\text{Change in } V_{REF} \text{ over specified current range}}{\text{The change in reference current}}$$

### 2. Reference Voltage Temperature Coefficient ($TCV_{REF}$)

This is the normalised reference voltage change over temperature, divided by the change in temperature. It is expressed in ppm/°C as follows

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

$\Delta T$ = temperature change in °C

$\Delta V_{REF}$ = change in reference voltage over temperature change $\Delta T$.

### 3. Guaranteed but not tested

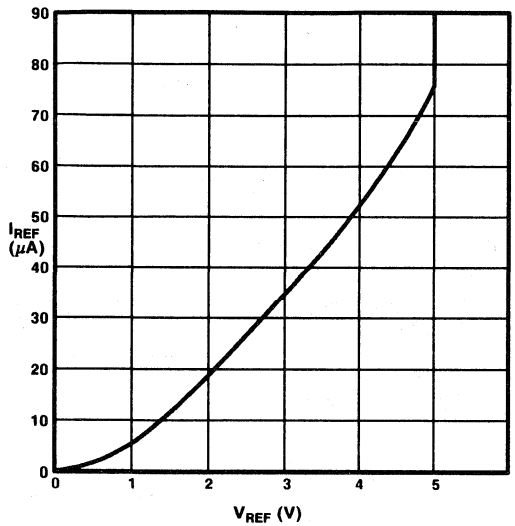



*Fig.4 Typical turn-on characteristic*

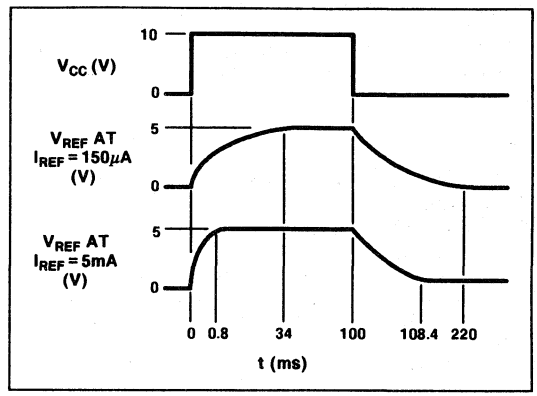



*Fig.5 SR50D typical response time (not to scale)*

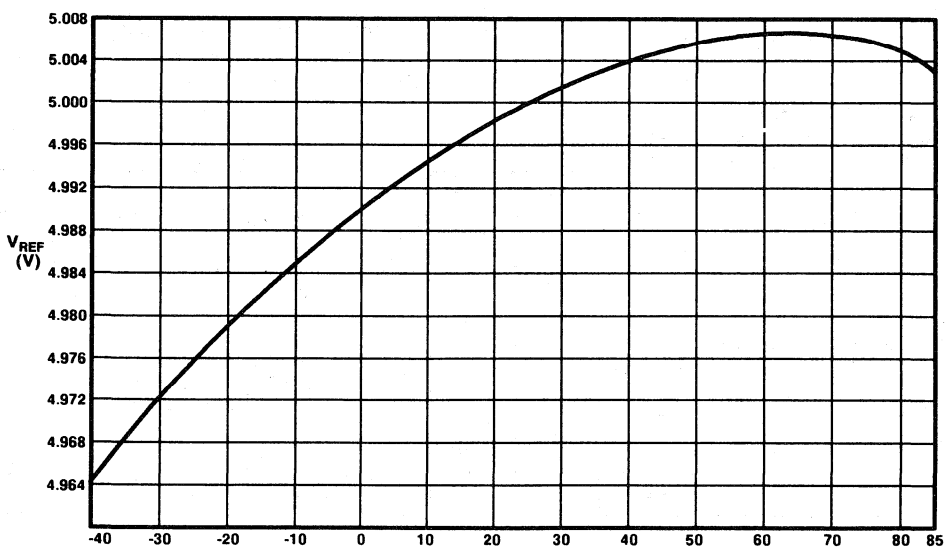



*Fig.6 Typical temperature characteristic of SR50D at $I_{REF}$ = 150μA*

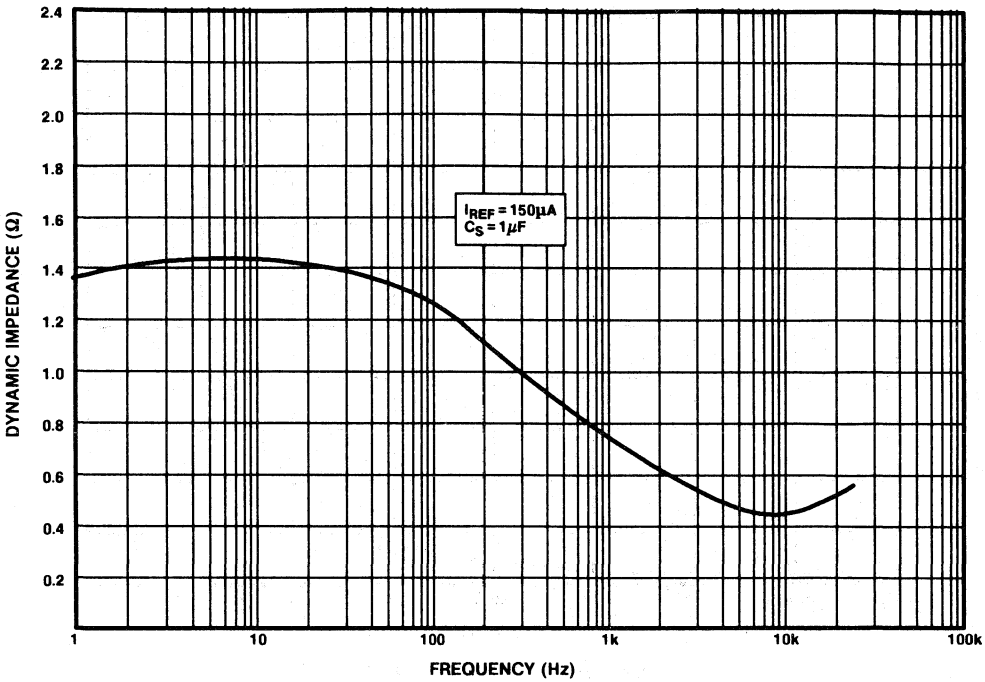



*Fig.7 Typical dynamic impedance of SR50D*

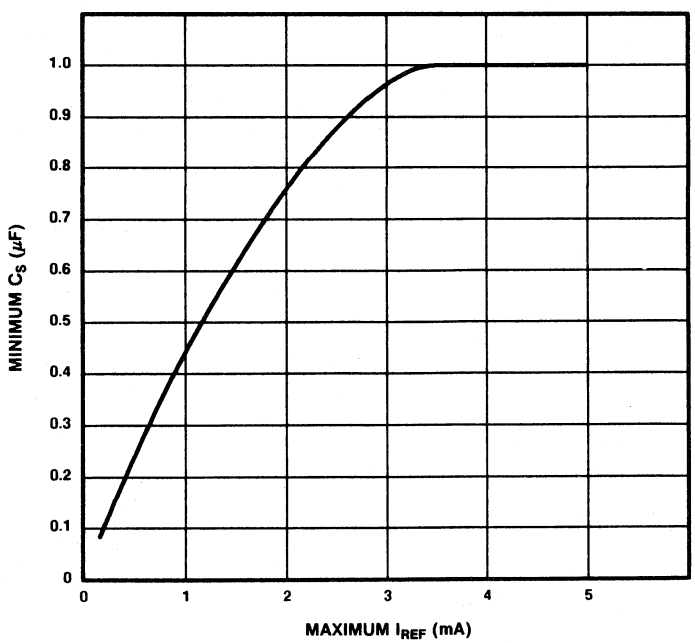



*Fig.8 Stabilising capacitor ($C_S$) required for optimum operation*

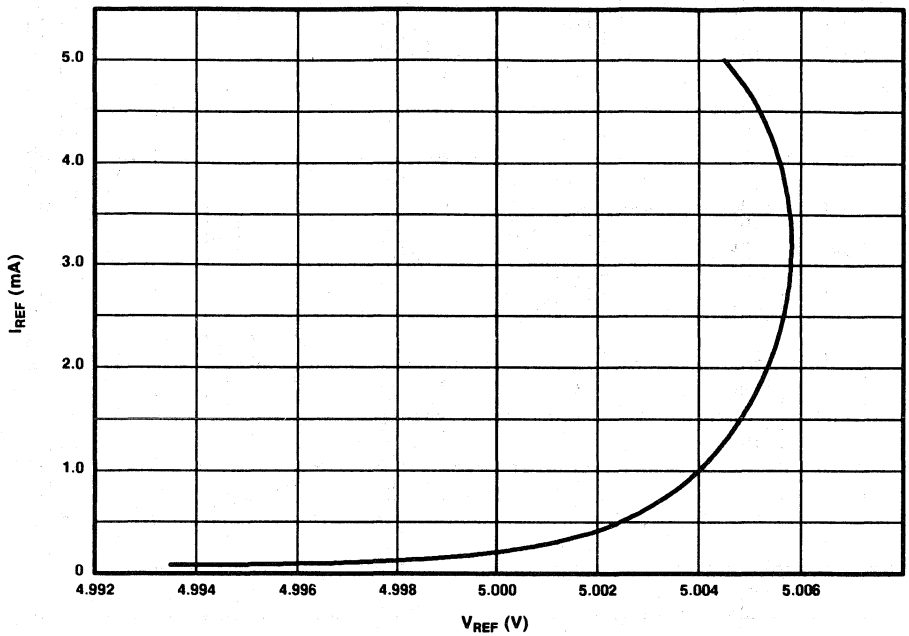



*Fig.9 Typical reference characteristic*

# ZN404 / ZN404D

## 2.45V PRECISION REFERENCE REGULATOR

The ZN404 is a monolithic integrated circuit providing a precise stable regulator source of 2.45V without the need for an external shaping capacitor

### FEATURES

- Low Temperature Coefficient
- Low Slope Resistance
- Very Good Long Term Stability
- Low Noise
- Internally Shaped
- Tight Tolerance
- ZN404 - 2-Lead TO-18 Metal Can Package
- ZN404D - 8-Lead Miniature Plastic Surface Mount Package

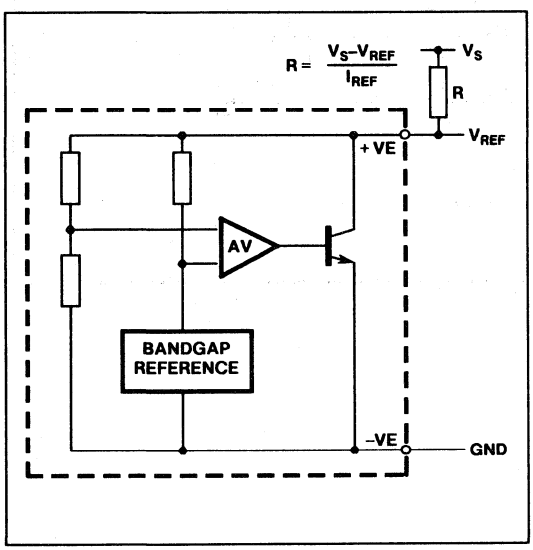



*Fig.2 Circuit diagram*

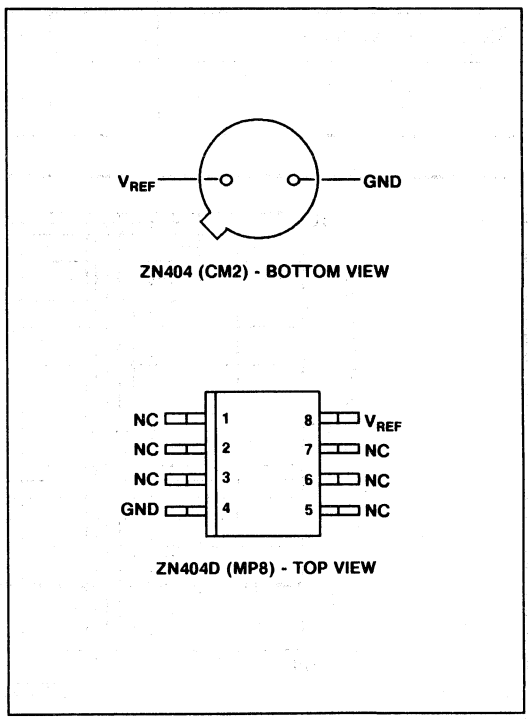



*Fig.1 Pin connections*

### ORDERING INFORMATION

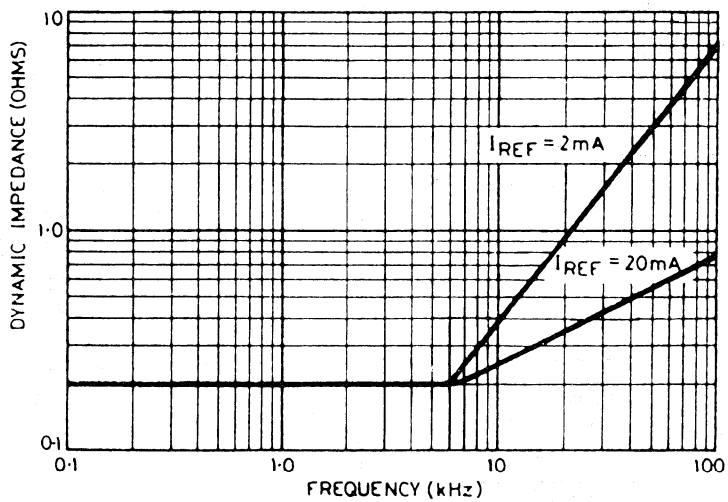
| Device Type | Operating Temperature | Package |
|---|---|---|
| ZN404 | 0°C to +70°C | CM2 |
| ZN404D | -20°C to +70°C | MP8 |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Dissipation | 300mW |
| Operating temperature range : | |
| ZN404 | 0°C to +70°C |
| ZN404D | -20°C to +70°C |
| Storage temperature | -55°C to +125°C |

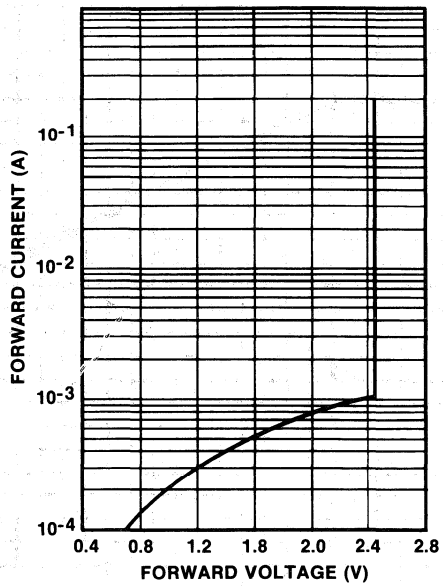
**ELECTRICAL CHARACTERISTICS** (at $T_{amb} = 25°C$ unless otherwise specified).

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Output voltage | $V_{REF}$ | 2.38 | 2.45 | 2.52 | V | Measured at 2mA |
| Slope resistance | $R_{REF}$ | – | 0.2 | 0.4 | Ω | |
| Reference current | $I_{REF}$ | 2 | – | 120 | mA | |
| Maximum change in $V_{REF}$ | $\Delta V_{REF}$ | | 6 | 25 | mV | |
| RMS noise voltage | | – | 10 | – | μV | 1Hz-10kHz |
| $V_{REF}$ drift at 70°C | | – | ±10 | – | ppm/1000 hours | CM2 package |

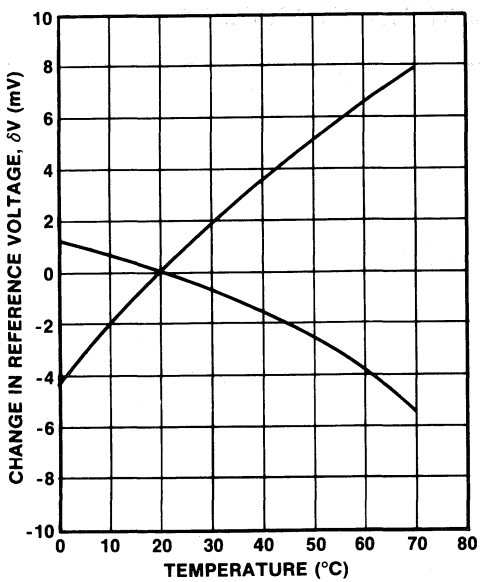


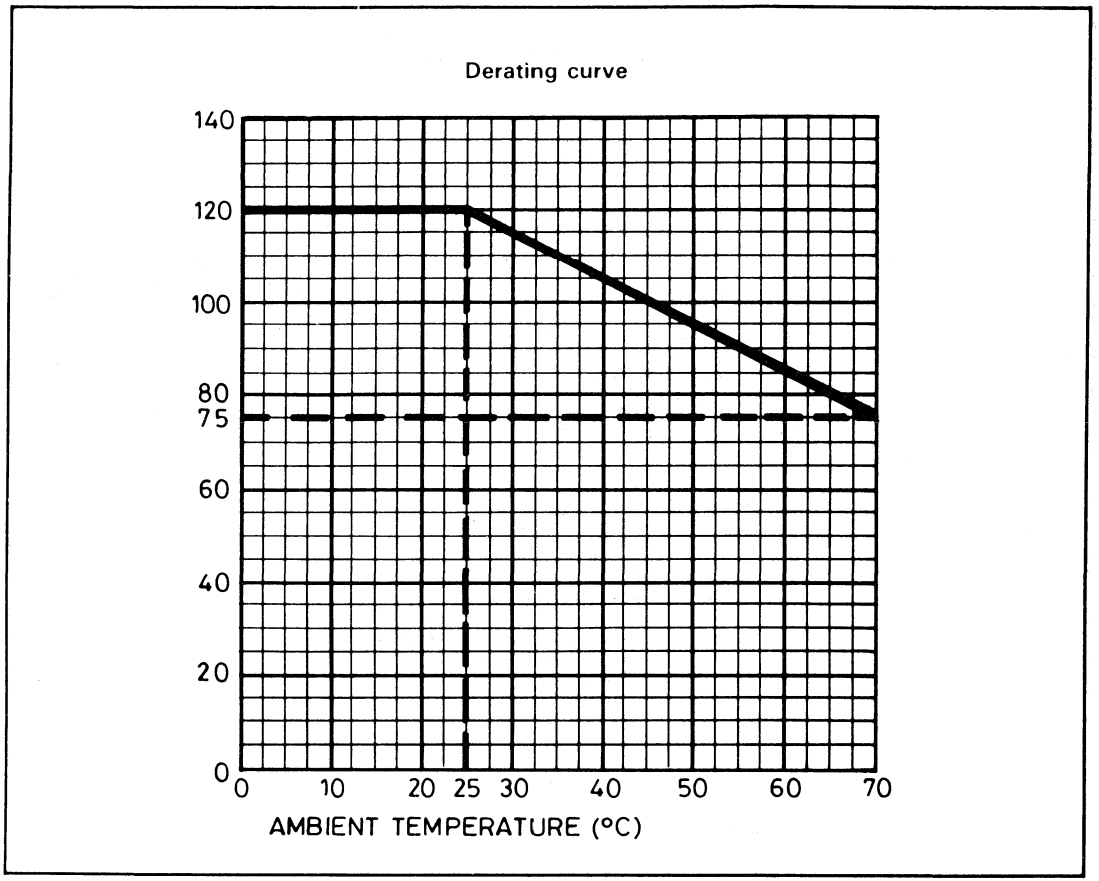

Dynamic impedance

**Forward characteristic (typical)**




**Temperature characteristic (typical)**




Derating curve
140
120
100
80
75
60
40
20
0
0
10
20
25
30
40
50
60
70
AMBIENT TEMPERATURE (°C)

# ZN423 / ZN423Z

## PRECISION VOLTAGE REFERENCE SOURCE

The ZN423/Z is a monolithic integrated circuit using the energy bandgap voltage of a base-emitter junction to produce a precise, stable, reference source of 1.26V. This is derived via an external dropping resistor for supply voltages of 1.5V upwards. The temperature coefficient of the ZN423/Z, unlike conventional Zener diodes, remains constant with reference current. The noise figure associated with breakdown mechanisms is also considerably reduced.

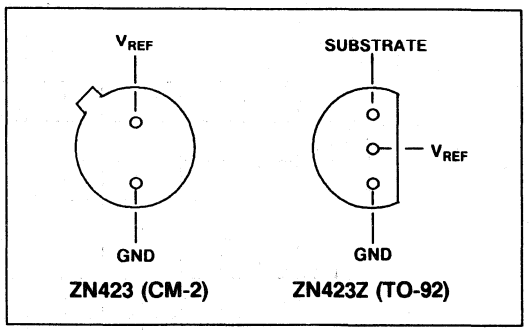



*Fig.1 Pin connections (bottom view)*

### FEATURES

- Low Voltage
- Low Temperature Coefficient
- Very Good Long Term Stability
- Low Slope Resistance
- Low RMS Noise
- Tight Tolerance
- High Power Supply Rejection Ratio
- ZN423 - 2-Lead TO-18 Metal Can Package
- ZN423Z - 3-Lead TO-92 Plastic Package

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current, $I_{REF}$ | 20mA |
| Operating temperature range : | |
| ZN423 | -55°C to +125°C |
| ZN423Z | 0°C to +70°C |
| Storage temperature range: | |
| ZN423 | -65°C to +165°C |
| ZN423Z | -55°C to +155°C |

### ORDERING INFORMATION

| Device type | Operating temperature | Package |
|---|---|---|
| **ZN423** | –55°C to +125°C | CM2 |
| **ZN423Z** | 0°C to +70°C | TO-92 |

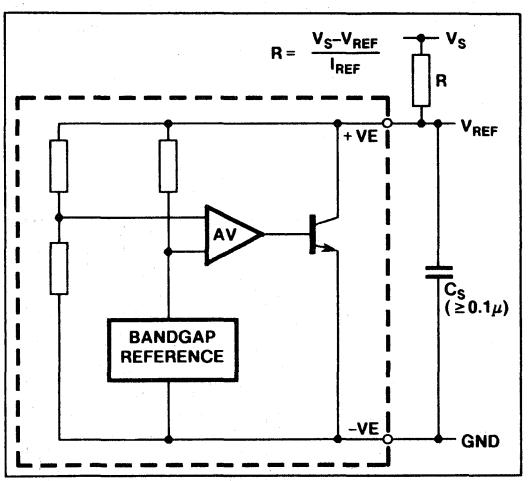



*Fig.2 Circuit diagram*

### ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
$T_{amb}$ = 25°C, Shaping capacitor, $C_S$ = 0.1μF

| Characteristic | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output voltage | $V_{REF}$ | 1.2 | 1.26 | 1.32 | V | |
| Slope resistance | $R_{REF}$ | | 0.5 | 1.5 | Ω | $I_{REF}$ = 5mA |
| Reference current | $I_{REF}$ | 1.5 | | 12 | mA | |
| Temperature coefficient | | | 30 | | ppm/°C | |
| External resistor | $R_{EXT}$ | 100 | | | Ω | $R_{EXT} = (V_{CC}-V_{REF})/I_{REF}$ |
| RMS noise voltage | | | 6 | | μV | 1Hz to 10kHz |
| Power supply ratio | $P_{SRR}$ | | 60 | | dB | $P_{SRR} = R_{EXT}/R_{REF}$, $V_{REF}$ = 1.26V, $I_{REF}$ = 2.5mA, $V_{CC}$ = 5.0V |

Reference current $I_{REF}$ (max.) v operating temperature.

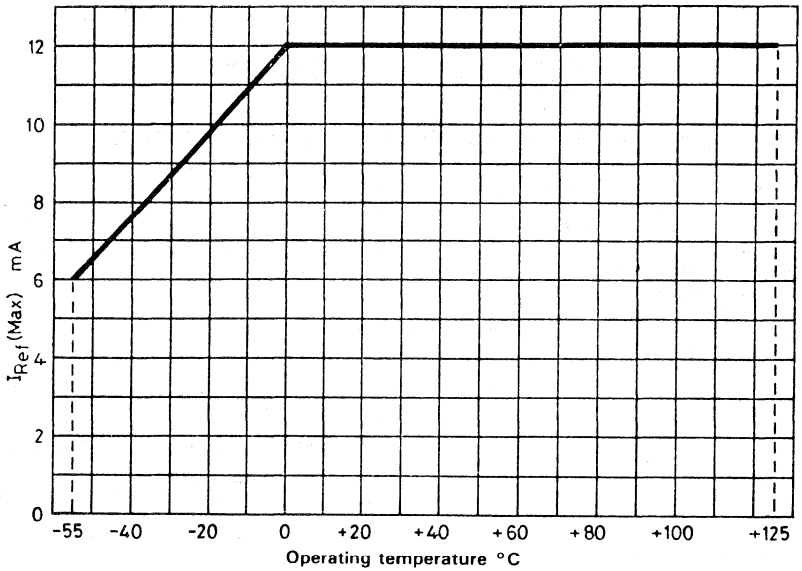



*Fig.2 Derating curve*

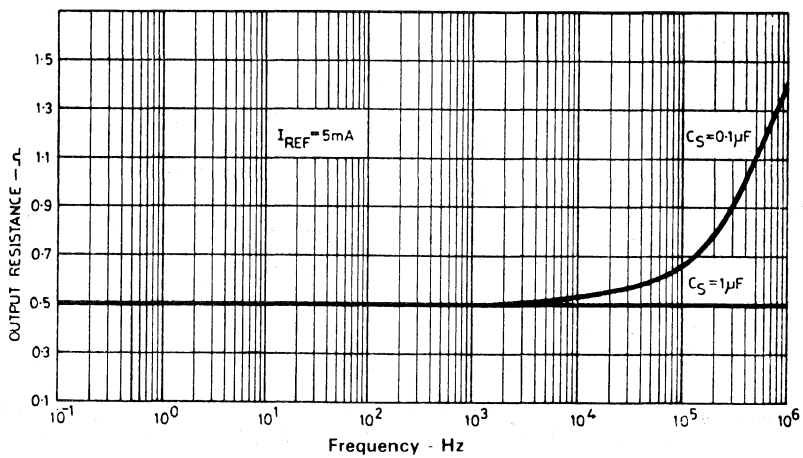



*Fig.3 Slope resistance v frequency ($I_{REF}$ = 5mA)*

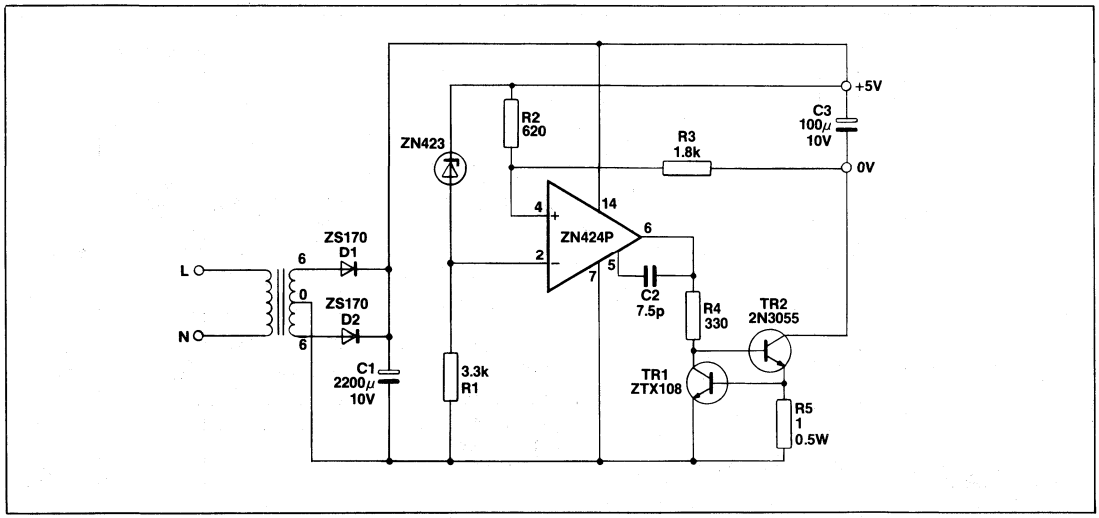



*Fig.4 5V, 0.5A power supply*

## APPLICATIONS

### 5V, 0.5A Power Supply

The circuit shown in Fig.4 is essentially a constant current source modified by the feedback components R2 and R3 to give a constant voltage output.

The output of the ZN424P need only be 2V above the negative rail, by placing the load in the collector of the output transistor TR2. Current control is achieved by TR1 and R5. This simple circuit has the following performance characteristics:

Output noise and ripple (full load) = 1mV rms
Load regulation (0 to 0.5A) = 0.1%
Temperature coefficient = ±100ppm/°C
Current limit = 0.65A.

### 5V, 1.0A Power Supply

The circuit detailed in Fig.5 provides improved performance over that in Fig.4. This is achieved by feeding the ZN423 reference and the ZN424P error amplifier from a more stable source, derived from the emitter-follower stage (TR1). The supply rejection ratio is improved by the factor R1/R5, where R5 is the slope resistance of the ZN423.

The output voltage is given by:

$$\frac{(R3 + R4)}{R3} \quad V_{REF}$$

and may be adjusted by replacing R3 with a 220 and a 500Ω preset potentiometer.

The output is protected against short circuits by TR2 setting a current limit of 1.6A.

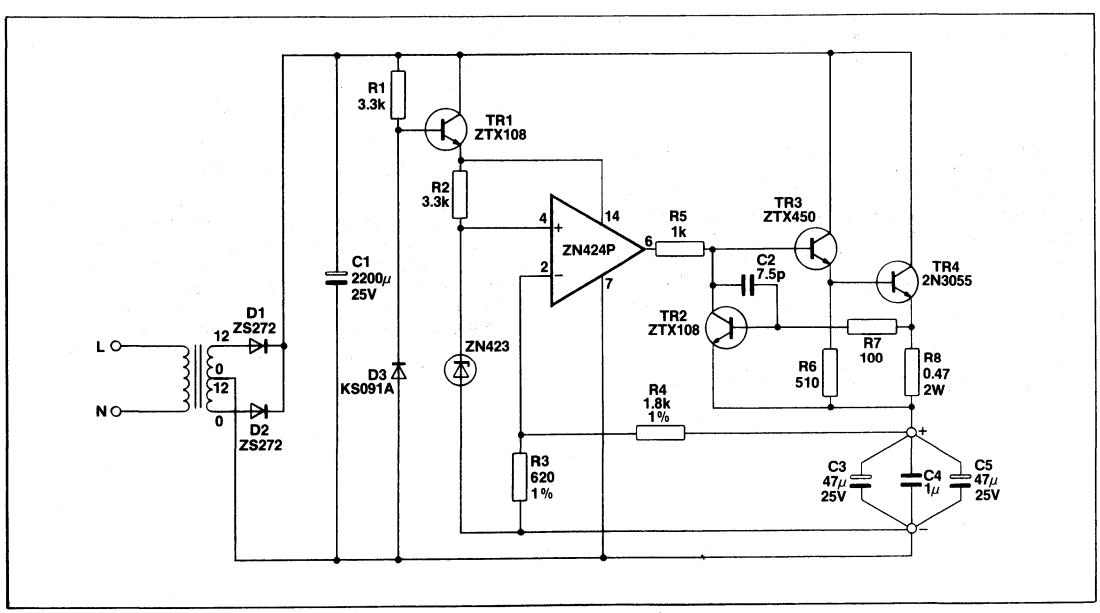



*Fig.5 5V, 1.0A power supply*

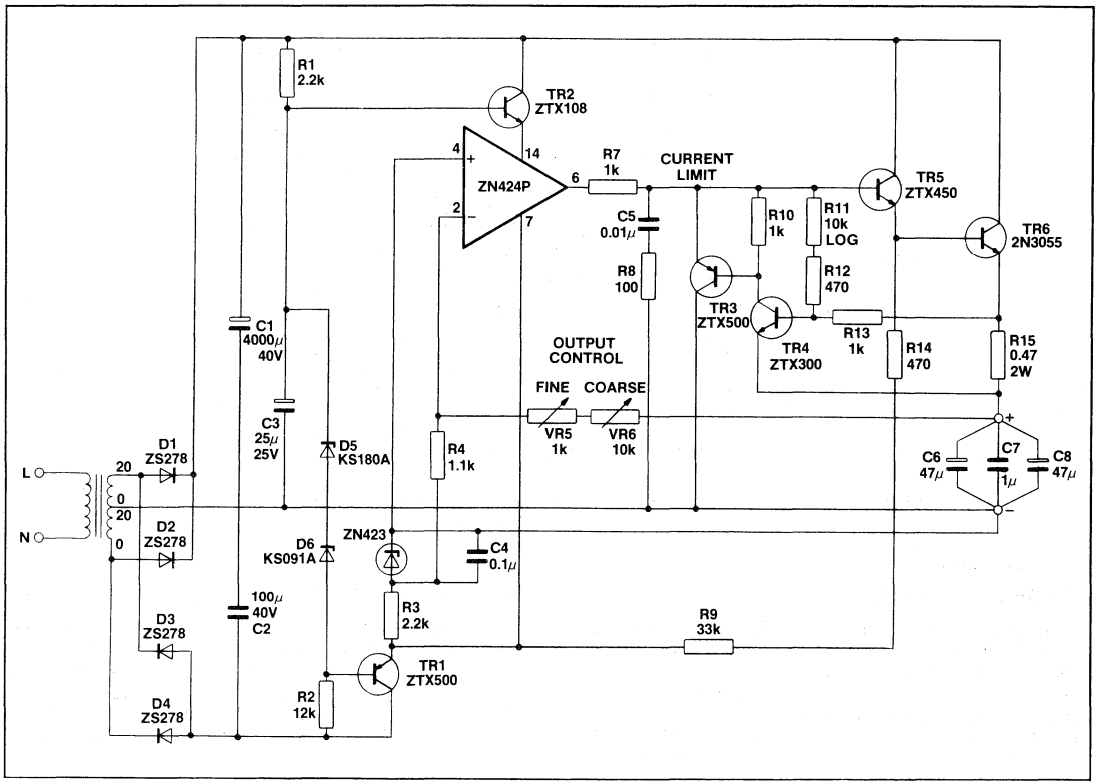



*Fig.6 0V to 12V, 1A power supply*

## 0V to 12V, 1A Power Supply

The circuit of Fig.6 provides a continuously variable, highly stable voltage for load currents up to 1A. The output voltage is given by:

$$V_O = \frac{(VR5 + VR6)}{R4} V_{REF}$$

and is controlled by VR5 and VR6 which should be high quality components (preferably wire wound).

The emitter follower stages TR1 and TR2 buffer the bias and reference from the output stage. The negative rail allows the output to operate down to 0V.

The current limit stage monitors output current through R15. As the potential across R15 increases due to load current, TR4 conducts and supplies base current for TR3, thus diverting part of the output from the ZN424P via TR3 to TR5.

Shaping is achieved by the network C5, R8 together with the output decoupling capacitors which also maintain low output resistance at frequencies above 100kHz.

The power supply has the following performance characteristics:

Output noise and ripple (full load) $<100\mu V$ rms
Output resistance (0 to 1A) $1M\Omega$
Temperature coefficient $\pm$ 100ppm/°C

## Variable 100mA to 2A Current Source

In the circuit of Fig.7 the output current is set by the resistor R in the collector of TR2, which may be switched to offer a range of output currents from 100mA to 2A with fine control by means of VR3 which varies the reference voltage to the non-inverting input of the ZN424P.

The feedback path from the output to the inverting input of the ZN424P maintains a constant voltage across R, equal to $(V_{CC} - V_{IN})$ and hence a constant current to the load given by $(V_{CC} - V_{IN})/R$.

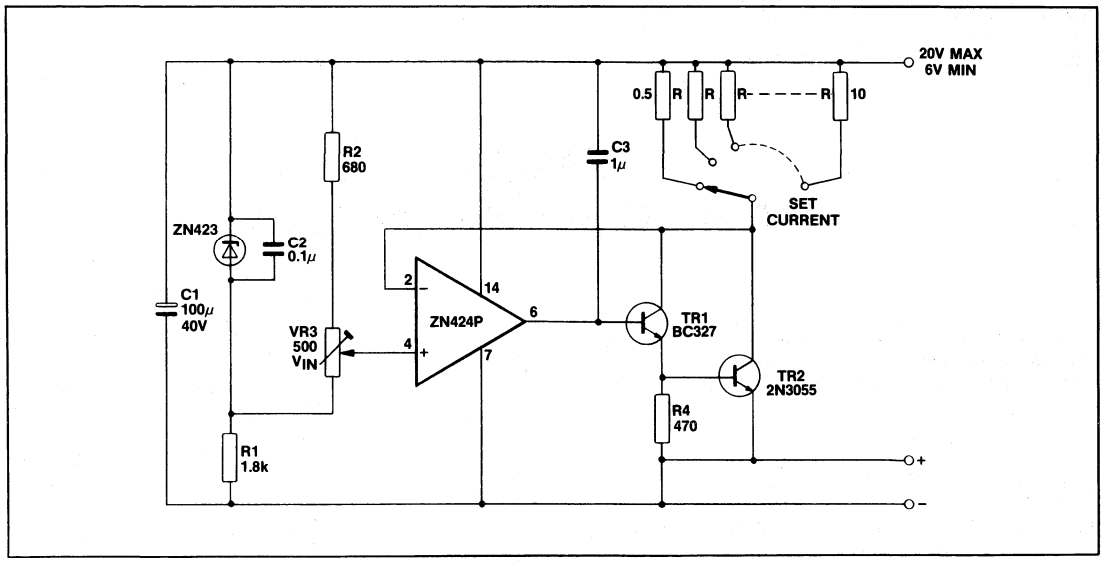
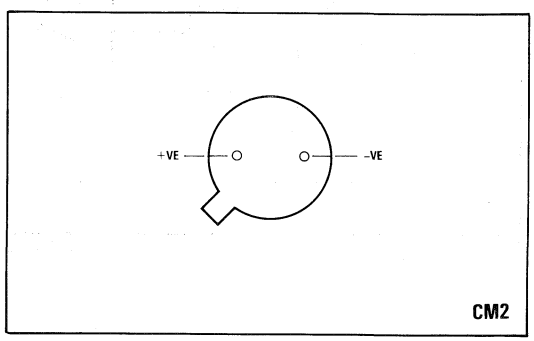



*Fig.7 Variable current source*

# ZN458

## 2.45V PRECISION REFERENCE REGULATOR

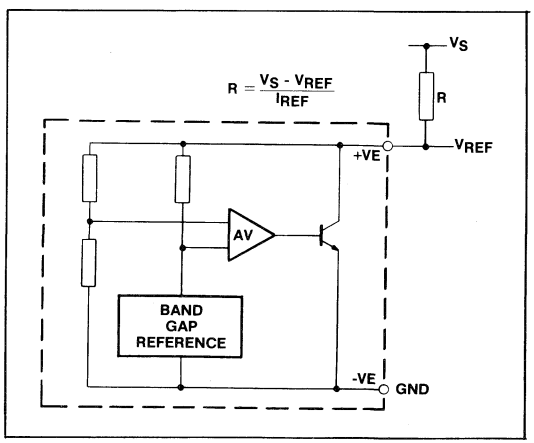
The ZN458 is a monolithic integrated circuit providing a precise stable reference source of 2.45V in a two lead package without the need for an external shaping capacitor.




Pin connections - bottom view

### FEATURES

- Guaranteed 5mV Maximum Deviation over Full Temperature Range
- Low Temperature Coefficient 0.003%/ °C
- Low Slope Resistance — 0.1 Ohms
- Very Good Long Term Stability — 10ppm
- Low Noise — 10 microvolts
- Internally Shaped
- Tight Tolerance ±1.43%
- Two Pin Package
- Wide Operating Current 2-120mA




Circuit diagram

### ORDERING INFORMATION

| Device | TC (ppm/°C) | Temperature range |
|---|---|---|
| **ZN458** | 99 | -20°C to +70°C |
| **ZN458A** | 49 | -20°C to +70°C |
| **ZN458B** | 29 | -20°C to +70°C |

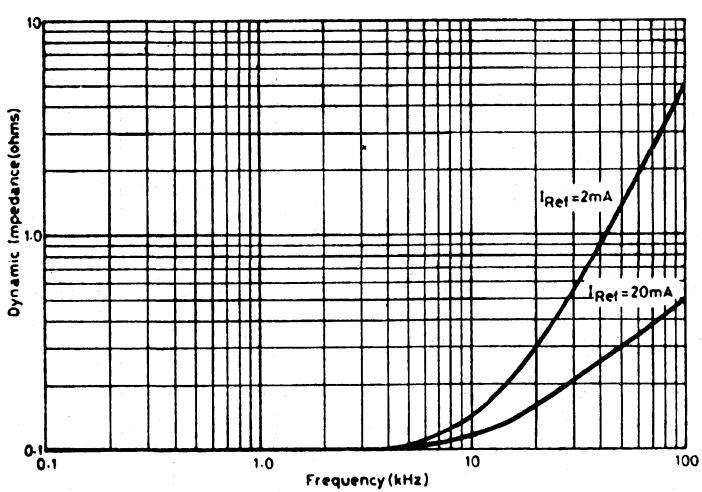
## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Dissipation | 300mW |
| Operating temperature range | −20 to +70°C |
| Storage temperature range | −55 to +150°C |

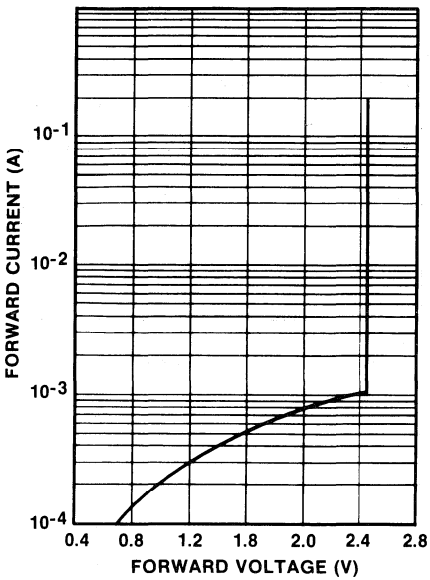
**ELECTRICAL CHARACTERISTICS** (at $T_{amb}$ = 25°C unless otherwise specified).

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Output voltage | $V_{REF}$ | 2.42 | 2.45 | 2.49 | V | Measured at 2mA |
| Slope resistance | $R_{REF}$ | – | 0.1 | 0.2 | Ω | |
| Reference current | $I_{REF}$ | 2.0 | – | 120 | mA | |
| Maximum change in $V_{REF}$ ZN458 | $\Delta V_{REF}$ | – | 10 | 17 | mV | 0 to +70°C |
| Maximum change in $V_{REF}$ ZN458A | $\Delta V_{REF}$ | – | 6 | 8.5 | mV | 0 to +70°C |
| Maximum change in $V_{REF}$ ZN458B | $\Delta V_{REF}$ | – | 4 | 5 | mV | 0 to +70°C |
| RMS noise voltage 1Hz-10kHz | | – | 10 | – | μV | |
| $V_{REF}$ drift at 70°C | | – | ±10 | – | ppm/1000 hours | |

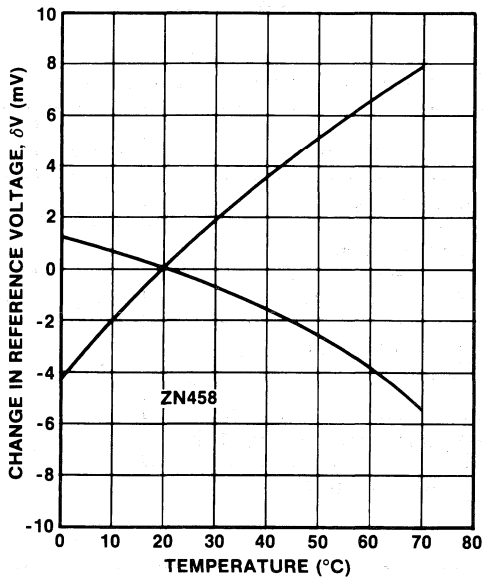
**Dynamic impedance**



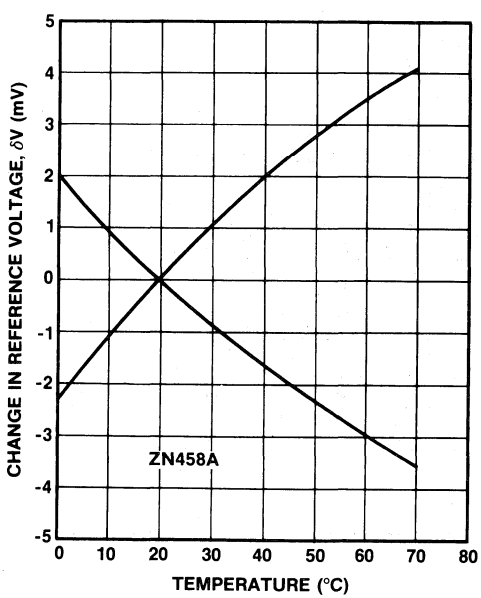
Forward characteristic

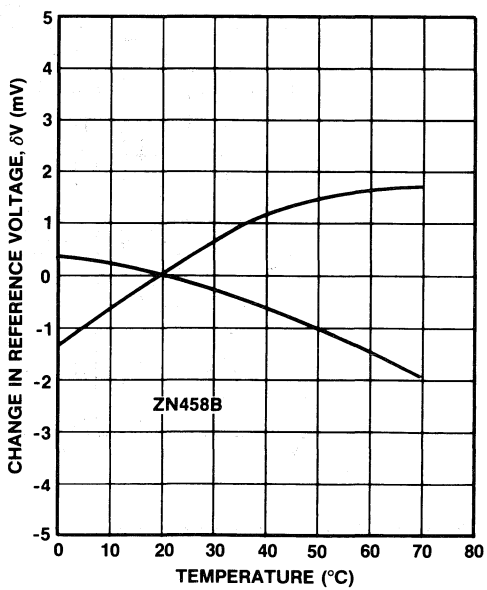



Temperature characteristic (typical)

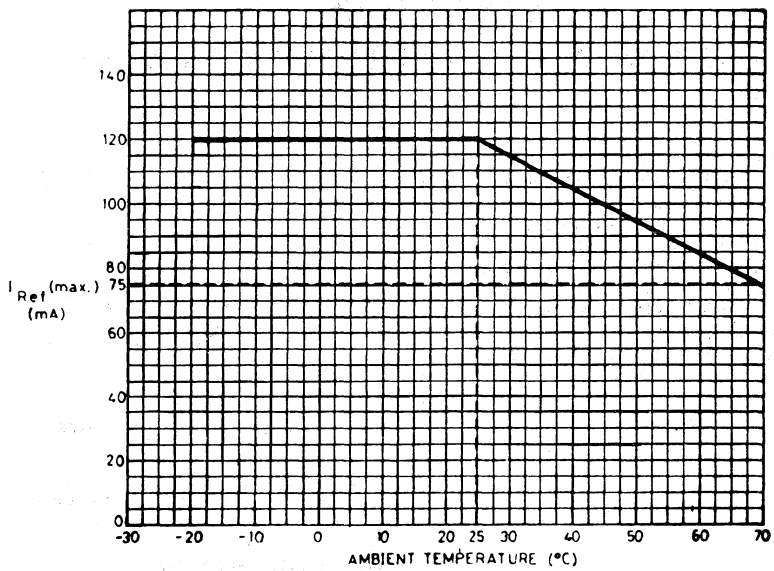



Temperature characteristics (typical)



## Derating curve



2472-1.0

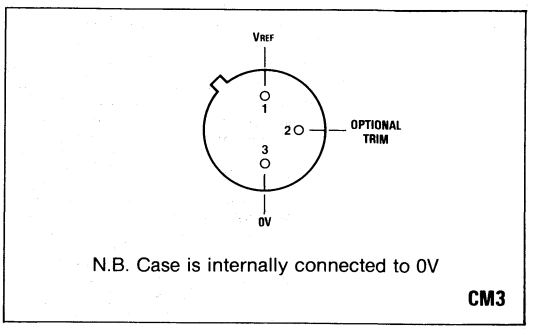
# ZNREF025

## 2.5V LOW POWER PRECISION REFERENCE SOURCE

The ZNREF025 is a monolithic integrated circuit providing a precise stable reference voltage of 2.50V at 500$\mu$A.

The circuit features a knee current of 150$\mu$A and operation over a wide range of temperatures and currents.

The ZNREF025 is available in a 3-pin metal can package with pin 2 offering a trim facility whereby the output voltage can be adjusted as shown in Fig.1. This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used, pin 2 should be left open circuit.




*Pin connections (bottom view)*

### FEATURES

- Trimmable Output
- Excellent Temperature Stability
- Low Output Noise Figure
- Available in Two Temperature Ranges
- 1 and 2% Initial Voltage Tolerance Versions Available
- No External Stabilising Capacitor required in most cases
- Low Slope Resistance

### ORDERING INFORMATION

| Device type | Tol. (%) | Temperature Range |
|---|---|---|
| **ZNREF025 A1** | 1 | –55°C to +125°C |
| **ZNREF025 C1** | 1 | 0°C to +70°C |
| **ZNREF025 C2** | 2 | 0°C to +70°C |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 10mA* |
| Power dissipation | 300mW |
| Operating temperature range | See ordering information |
| Storage temperature range | –55°C to +175°C |
| Soldering temperature for a maximum time of 10s | |
| Within $\frac{1}{16}$ in of the seating plane | 300°C |
| Within $\frac{1}{32}$ in of the seating plane | 265°C |

*Below –25°C this figure should be linearly derated to 1.5mA maximum at –55°C.

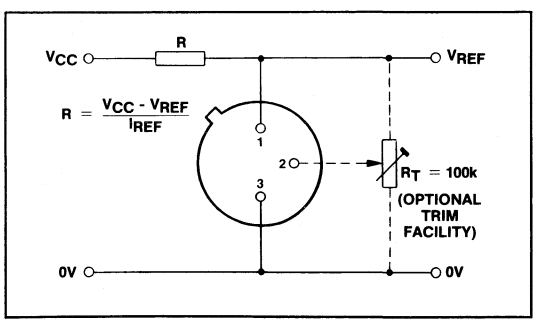



*Fig.1 ZNREF025 application circuit*

## TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Initial voltage tolerance % | Grade A −55 to 125°C | | Grade C 0 to 70°C | | Units |
|---|---|---|---|---|---|---|---|
| | | | Typ. | Max. | Typ. | Max. | |
| Output voltage change over relevant temperature range (See note (a)) | $\Delta V_{REF}$ | 1 & 2 | 16.0 | 22.5 | 2.7 | 8.8 | mV |
| Output voltage temperature coefficient (See note (b)) | $TCV_{REF}$ | 1 & 2 | 35 | 50 | 15 | 50 | ppm/°C |

**ELECTRICAL CHARACTERISTICS** (at $T_{amb} = 25°C$ and Pin 2 o/c unless otherwise specified). **(LOAD CAPACITANCE** should be less than 220pF or greater than 22nF).

| Parameter | Symbol | Min. | Typ. | Max. | Units | Comments |
|---|---|---|---|---|---|---|
| Output voltage<br>1% tolerance (A1 C1)<br>2% tolerance (C2) | $V_{REF}$ | <br>2.475<br>2.450 | <br>2.500<br>2.500 | <br>2.525<br>2.550 | V | $I_{REF} = 500\mu A$ |
| Output voltage adjustment range | $\Delta V_{TRIM}$ | – | ±5 | – | % | $R_T = 100k\Omega$ |
| Change in $TCV_{REF}$ with output adjustment | $TC\Delta V_{TRIM}$ | – | 0.8 | – | ppm/°C/% | |
| Operating current range | $I_{REF}$ | 0.15 | – | 10 | mA | See note (c) |
| Turn-on time<br>Turn-off time | $t_{on}$<br>$t_{off}$ | –<br>– | 40<br>0.3 | –<br>– | μS | $R_L = 1k\Omega$ |
| Output voltage noise (over the range 0.1 to 10Hz) | $e_{np-p}$ | – | 50 | – | μV | Peak to peak measurement |
| Slope resistance | $R_{REF}$ | – | 1.5 | 2.0 | Ω | $I_{REF}$ 0.5mA to 5mA See note (d) |

### NOTES

**(a) Output change with temperature ($\Delta V_{REF}$)**
The absolute maximum difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

**(b) Output temperature coefficient ($TCV_{REF}$)**
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

$\Delta T$ = Full temperature change.

**(c) Operating current ($I_{REF}$)**
Maximum operating current must be derated as indicated in maximum ratings.

**(d) Slope resistance ($R_{REF}$)**
The slope resistance is defined as $R_{REF}$ = change in $V_{REF}$ overspecified current range

$$\Delta I_{REF} = 5 - 0.5 = 4.5mA \text{ (typically)}$$

**(e) Line regulation**

The ratio of change in output voltage to the change in input voltage producing it.

$$\frac{R_{REF} \times 100}{V_{REF} \times R_S} \text{ %/V}$$

$R_S$ = Source resistance

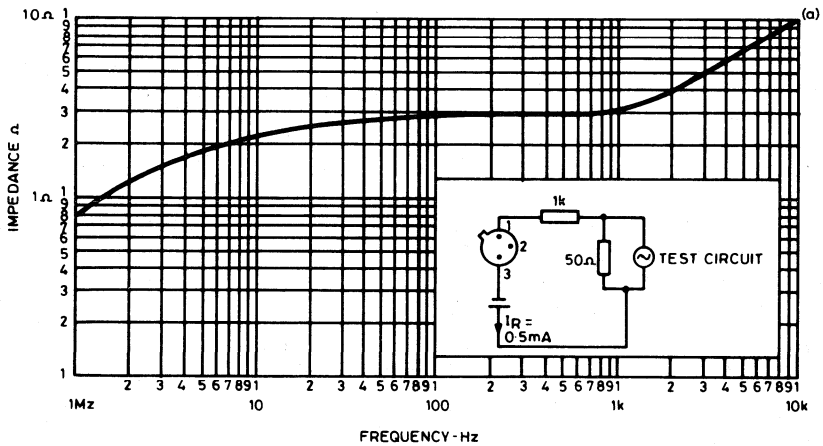



*Fig.2 Dynamic impedance (typical)*

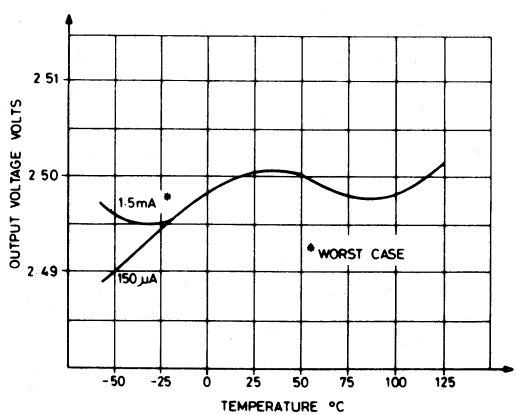



*Fig.3 Typical temperature characteristics*

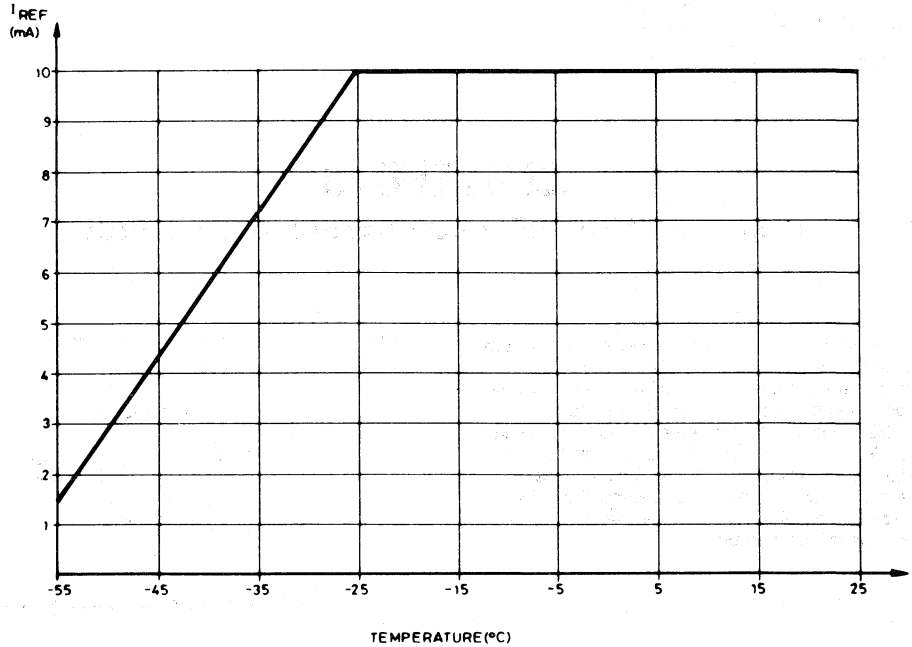



*Fig.4 $I_{REF}$ derating for ZNREF025*

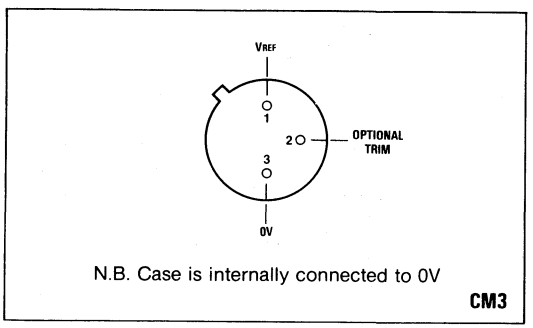
# ZNREF040

## 4V LOW POWER PRECISION REFERENCE SOURCE

The ZNREF040 is a monolithic integrated circuit providing a precise stable reference voltage of 4.01V at 500$\mu$A.

The circuit features a knee current of 150$\mu$A and operation over a wide range of temperatures and currents.

The ZNREF040 is available in a 3-pin metal can package with pin 2 offering a trim facility whereby the output voltage can be adjusted as shown in Fig.1. This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used, pin 2 should be left open circuit.




*Pin connections (bottom view)*

### FEATURES

- Trimmable Output
- Excellent Temperature Stability
- Low Output Noise Figure
- Available in Two Temperature Ranges
- 1 and 2% Initial Voltage Tolerance Versions Available
- No External Stabilising Capacitor required in most cases
- Low Slope Resistance

### ORDERING INFORMATION

| Device type | Tol. (%) | Temperature Range |
|---|---|---|
| **ZNREF040 A1** | 1 | –55°C to +125°C |
| **ZNREF040 C1** | 1 | 0°C to +70°C |
| **ZNREF040 C2** | 2 | 0°C to +70°C |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 75mA* |
| Power dissipation | 300mW |
| Operating temperature range | See ordering information |
| Storage temperature range | –55°C to +175°C |
| Soldering temperature for a maximum time of 10s | |
| Within $\frac{1}{16}$ in of the seating plane | 300°C |
| Within $\frac{1}{32}$ in of the seating plane | 265°C |

* Above 25°C this figure should be linearly derated to 20mA at +125°C.

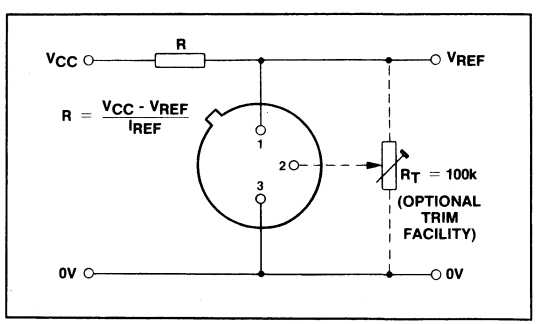



*Fig.1 ZNREF040 application circuit*

## TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Initial voltage tolerance % | Grade A −55 to 125°C | | Grade C 0 to 70°C | | Units |
|---|---|---|---|---|---|---|---|
| | | | Typ. | Max. | Typ. | Max. | |
| Output voltage change over relevant temperature range (See note (a)) | $\Delta V_{REF}$ | 1 & 2 | 25.6 | 36 | 4.2 | 14 | mV |
| Output voltage temperature coefficient (See note (b)) | $TCV_{REF}$ | 1 & 2 | 35 | 50 | 15 | 50 | ppm/°C |

**ELECTRICAL CHARACTERISTICS** (at $T_{amb} = 25°C$ and Pin 2 o/c unless otherwise specified).

| Parameter | Symbol | Min. | Typ. | Max. | Units | Comments |
|---|---|---|---|---|---|---|
| Output voltage<br>1% tolerance (A1 C1)<br>2% tolerance (C2) | $V_{REF}$ | <br>3.97<br>3.93 | <br>4.01<br>4.01 | <br>4.05<br>4.09 | V | $I_{REF} = 500\mu A$ |
| Output voltage adjustment range | $\Delta V_{TRIM}$ | – | ±5 | – | % | $R_T = 100k\Omega$ |
| Change in $TCV_{REF}$ with output adjustment | $TC\Delta V_{TRIM}$ | – | 0.8 | – | ppm/°C/% | |
| Operating current range | $I_{REF}$ | 0.15 | – | 75 | mA | See note (c) |
| Turn-on time<br>Turn-off time | $t_{on}$<br>$t_{off}$ | –<br>– | 40<br>0.3 | –<br>– | μs | $R_L = 1k\Omega$ |
| Output voltage noise (over the range 0.1 to 10Hz) | $e_{np-p}$ | – | 50 | – | μV | Peak to peak measurement |
| Slope resistance | $R_{REF}$ | – | 2 | 3 | Ω | $I_{REF}$ 0.5mA to 5mA, See note (d) |

### NOTES

**(a) Output change with temperature ($\Delta V_{REF}$)**
The absolute maximum difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

**(b) Output temperature coefficient ($TCV_{REF}$)**
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

$\Delta T$ = Full temperature change.

**(c) Operating current ($I_{REF}$)**
Maximum operating current must be derated as indicated in maximum ratings.

**(d) Slope resistance ($R_{REF}$)**
The slope resistance is defined as $R_{REF}$ = change in $V_{REF}$ overspecified current range

$\Delta I_{REF} = 5 - 0.5 = 4.5mA$ (typically)

**(e) Line regulation**

The ratio of change in output voltage to the change in input voltage producing it.

$$\frac{R_{REF} \times 100}{V_{REF} \times R_S} \text{ %/V}$$ $R_S$ = Source resistance

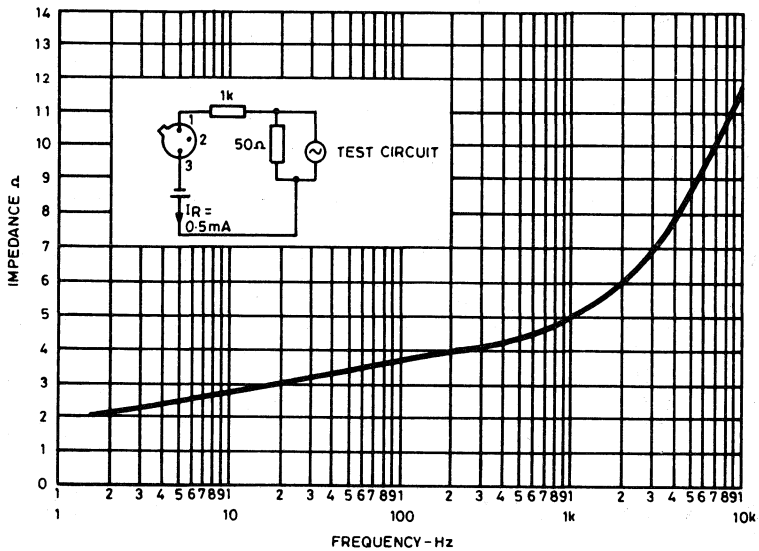



*Fig.2 Dynamic impedance (typical)*

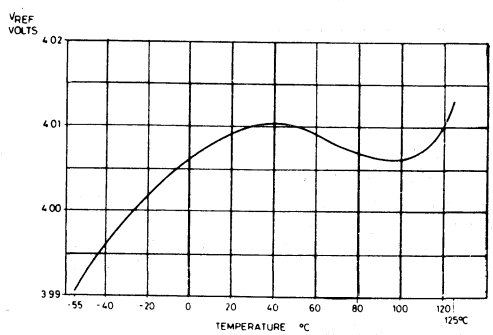



*Fig.3 Typical temperature characteristics*

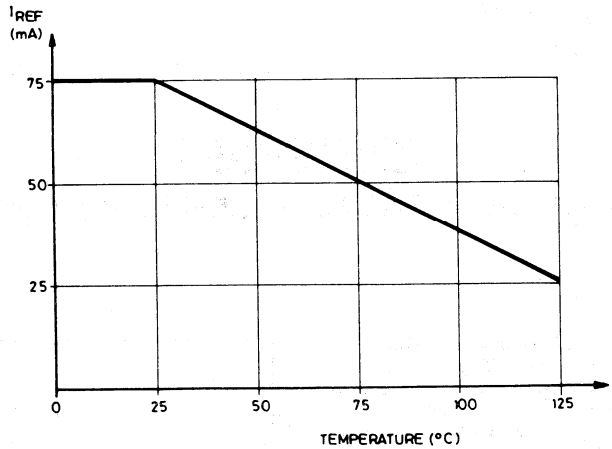



*Fig.4 $I_{REF}$ derating for ZNREF040*

2473-1.0

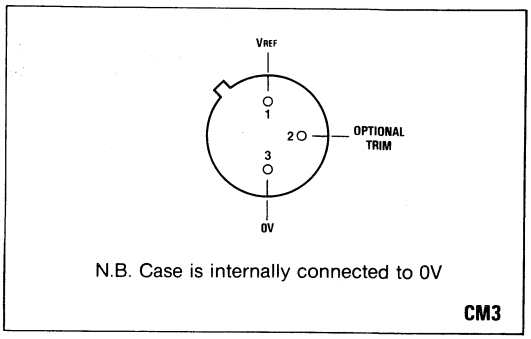
# ZNREF050

## 5V LOW POWER PRECISION REFERENCE SOURCE

The ZNREF050 is a monolithic integrated circuit providing a precise stable reference voltage of 4.90V at 500$\mu$A.

The circuit features a knee current of 150$\mu$A and operation over a wide range of temperatures and currents.

The ZNREF050 is available in a 3-pin metal can package with pin 2 offering a trim facility whereby the output voltage can be adjusted as shown in Fig.1. This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used, pin 2 should be left open circuit.




*Pin connections (bottom view)*

### FEATURES

- Trimmable Output
- Excellent Temperature Stability
- Low Output Noise Figure
- Available in Two Temperature Ranges
- 1 and 2% Initial Voltage Tolerance Versions Available
- No External Stabilising Capacitor required in most cases
- Low Slope Resistance

### ORDERING INFORMATION

| Device type | Tol. (%) | Temperature Range |
|---|---|---|
| **ZNREF050 A1** | 1 | –55°C to +125°C |
| **ZNREF050 C1** | 1 | 0°C to +70°C |
| **ZNREF050 C2** | 2 | 0°C to +70°C |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 60mA* |
| Power dissipation | 300mW |
| Operating temperature range | See ordering information |
| Storage temperature range | –55°C to +175°C |
| Soldering temperature for a maximum time of 10s | |
| Within $\frac{1}{16}$ in of the seating plane | 300°C |
| Within $\frac{1}{32}$ in of the seating plane | 265°C |

*Above 25°C this figure should be linearly derated to 20mA at +125°C.

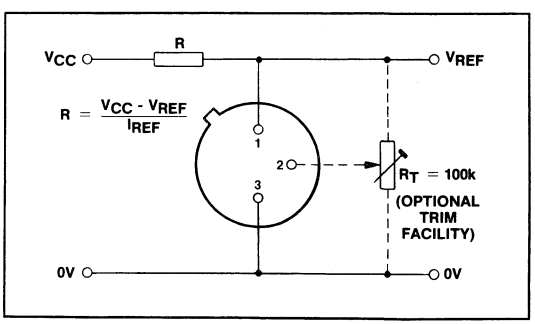



*Fig.1 ZNREF050 application circuit*

## TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Initial voltage tolerance % | Grade A −55 to 125°C | | Grade C 0 to 70°C | | Units |
|---|---|---|---|---|---|---|---|
| | | | Typ. | Max. | Typ. | Max. | |
| Output voltage change over relevant temperature range (See note (a)) | $\Delta V_{REF}$ | 1 & 2 | 32 | 45 | 5.4 | 17.2 | mV |
| Output voltage temperature coefficient (See note (b)) | $TCV_{REF}$ | 1 & 2 | 35 | 50 | 15 | 50 | ppm/°C |

**ELECTRICAL CHARACTERISTICS** (at $T_{amb} = 25°C$ and Pin 2 o/c unless otherwise specified).

| Parameter | Symbol | Min. | Typ. | Max. | Units | Comments |
|---|---|---|---|---|---|---|
| Output voltage<br>1% tolerance (A1 C1)<br>2% tolerance (C2) | $V_{REF}$ | <br>4.85<br>4.80 | <br>4.90<br>4.90 | <br>4.95<br>5.00 | V | $I_{REF} = 500\mu A$ |
| Output voltage adjustment range | $\Delta V_{TRIM}$ | – | ±5 | – | % | $R_T = 100k\Omega$ |
| Change in $TCV_{REF}$ with output adjustment | $TC\Delta V_{TRIM}$ | – | 0.8 | – | ppm/°C/% | |
| Operating current range | $I_{REF}$ | 0.15 | – | 60 | mA | See note (c) |
| Turn-on time<br>Turn-off time | $t_{on}$<br>$t_{off}$ | –<br>– | 40<br>0.3 | –<br>– | μs | $R_L = 1k\Omega$ |
| Output voltage noise (over the range 0.1 to 10Hz) | $e_{np-p}$ | – | 50 | – | μV | Peak to peak measurement |
| Slope resistance | $R_{REF}$ | – | 1.5 | 2 | Ω | $I_{REF}$ 0.5mA to 5mA, See note (d) |

### NOTES

**(a) Output change with temperature ($\Delta V_{REF}$)**
The absolute maximum difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

**(b) Output temperature coefficient ($TCV_{REF}$)**
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

$\Delta T$ = Full temperature change.

**(c) Operating current ($I_{REF}$)**
Maximum operating current must be derated as indicated in maximum ratings.

**(d) Slope resistance ($R_{REF}$)**
The slope resistance is defined as $R_{REF}$ = change in $V_{REF}$ overspecified current range

$$\Delta I_{REF} = 5 - 0.5 = 4.5mA \text{ (typically)}$$

**(e) Line regulation**

The ratio of change in output voltage to the change in input voltage producing it.

$$\frac{R_{REF} \times 100}{V_{REF} \times R_S} \text{ %/V}$$

$R_S$ = Source resistance

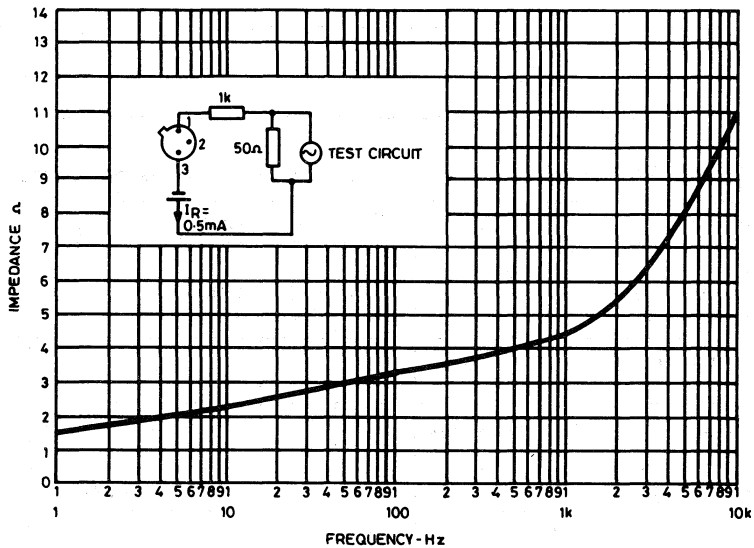



*Fig.2 Dynamic impedance (typical)*

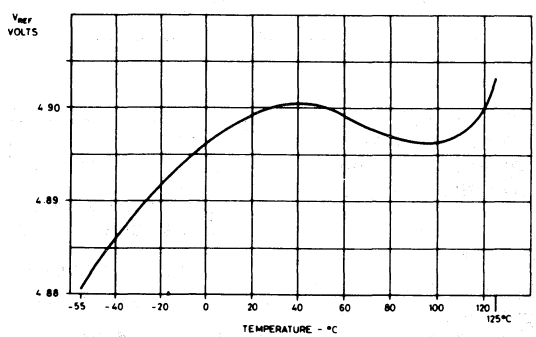



*Fig.3 Typical temperature characteristics*

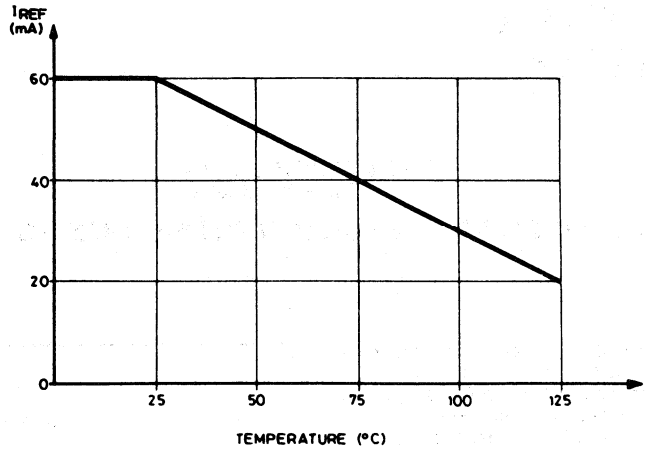



*Fig.4 $I_{REF}$ derating for ZNREF050*

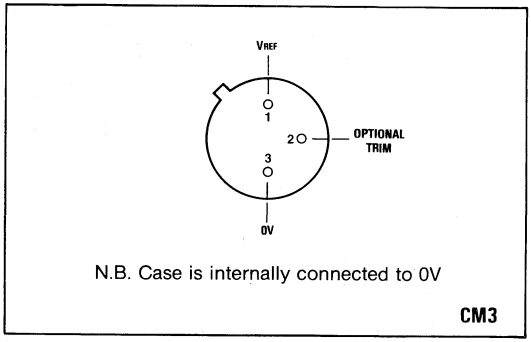
# ZNREF062

## 6.2V LOW POWER PRECISION REFERENCE SOURCE

The ZNREF062 is a monolithic integrated circuit providing a precise stable reference voltage of 6.17V at 500$\mu$A.

The circuit features a knee current of 150$\mu$A and operation over a wide range of temperatures and currents.

The ZNREF062 is available in a 3-pin metal can package with pin 2 offering a trim facility whereby the output voltage can be adjusted as shown in Fig.1. This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used, pin 2 should be left open circuit.




*Pin connections (bottom view)*

### FEATURES

- Trimmable Output
- Excellent Temperature Stability
- Low Output Noise Figure
- Available in Two Temperature Ranges
- 1 and 2% Initial Voltage Tolerance Versions Available
- No External Stabilising Capacitor required in most cases
- Low Slope Resistance

### ORDERING INFORMATION

| Device type | Tol. (%) | Temperature Range |
|---|---|---|
| **ZNREF062 A1** | 1 | –55°C to +125°C |
| **ZNREF062 C1** | 1 | 0°C to +70°C |
| **ZNREF062 C2** | 2 | 0°C to +70°C |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 50mA* |
| Power dissipation | 300mW |
| Operating temperature range | See ordering information |
| Storage temperature range | –55°C to +175°C |
| Soldering temperature for a maximum time of 10s | |
| Within $\frac{1}{16}$ in of the seating plane | 300°C |
| Within $\frac{1}{32}$ in of the seating plane | 265°C |

*Below –25°C this figure should be linearly derated to 20mA at +110°C.

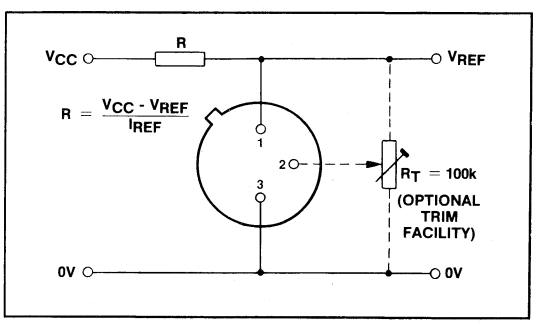



*Fig.1 ZNREF062 application circuit*

## TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Initial voltage tolerance % | Grade AB -55 to 110°C | | Grade C 0 to 70°C | | Units |
|---|---|---|---|---|---|---|---|
| | | | Typ. | Max. | Typ. | Max. | |
| Output voltage change over relevant temperature range (See note (a)) | $\Delta V_{REF}$ | 1 & 2 | 26 | 40 | 6.5 | 22 | mV |
| Output voltage temperature coefficient (See note (b)) | $TCV_{REF}$ | 1 & 2 | 25 | 40 | 15 | 50 | ppm/°C |

**ELECTRICAL CHARACTERISTICS** (at $T_{amb} = 25°C$ and Pin 2 o/c unless otherwise specified).

| Parameter | Symbol | Min. | Typ. | Max. | Units | Comments |
|---|---|---|---|---|---|---|
| Output voltage<br>1% tolerance (AB C1)<br>2% tolerance (C2) | $V_{REF}$ | <br>6.11<br>6.05 | <br>6.17<br>6.17 | <br>6.23<br>6.29 | V | $I_{REF} = 500\mu A$ |
| Output voltage adjustment range | $\Delta V_{TRIM}$ | – | ±5 | – | % | $R_T = 100k\Omega$ |
| Change in $TCV_{REF}$ with output adjustment | $TC\Delta V_{TRIM}$ | – | 0.8 | – | ppm/°C/% | |
| Operating current range | $I_{REF}$ | 0.15 | – | 50 | mA | See note (c) |
| Turn-on time<br>Turn-off time | $t_{on}$<br>$t_{off}$ | –<br>– | 40<br>0.3 | –<br>– | $\mu s$ | $R_L = 1k\Omega$ |
| Output voltage noise (over the range 0.1 to 10Hz) | $e_{np\text{-}p}$ | – | 50 | – | $\mu V$ | Peak to peak measurement |
| Slope resistance | $R_{REF}$ | – | 2 | 3 | Ω | $I_{REF}$ 0.5mA to 5mA, See note (d) |

### NOTES

**(a) Output change with temperature ($\Delta V_{REF}$)**
The absolute maximum difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

**(b) Output temperature coefficient ($TCV_{REF}$)**
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

$\Delta T$ = Full temperature change.

**(c) Operating current ($I_{REF}$)**
Maximum operating current must be derated as indicated in maximum ratings.

**(d) Slope resistance ($R_{REF}$)**
The slope resistance is defined as $R_{REF}$ = change in $V_{REF}$ overspecified current range

$\Delta I_{REF} = 5 - 0.5 = 4.5mA$ (typically)

**(e) Line regulation**

The ratio of change in output voltage to the change in input voltage producing it.

$$\frac{R_{REF} \times 100}{V_{REF} \times R_S} \text{ \%/V}$$ $R_S$ = Source resistance

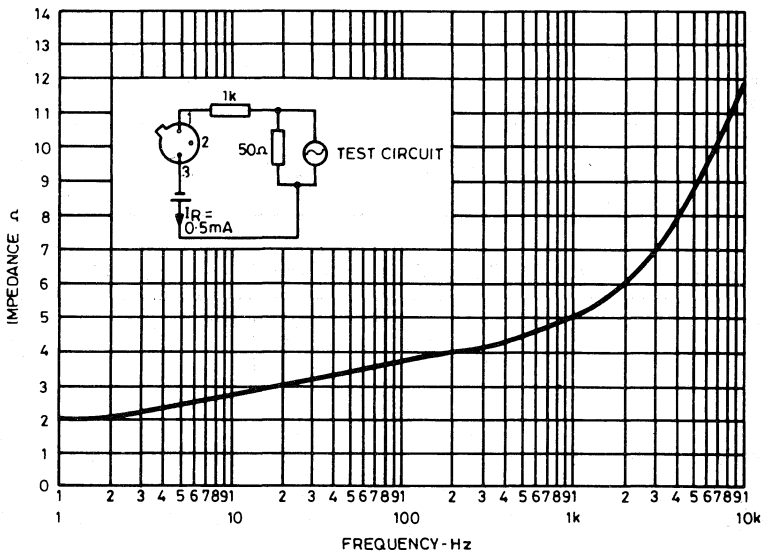



*Fig.2 Dynamic impedance (typical)*

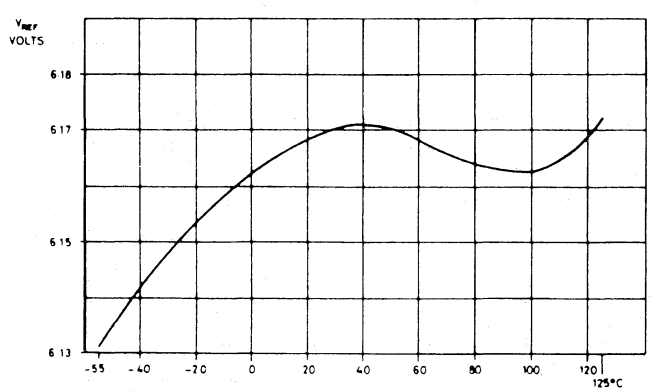



*Fig.3 Typical temperature characteristics*

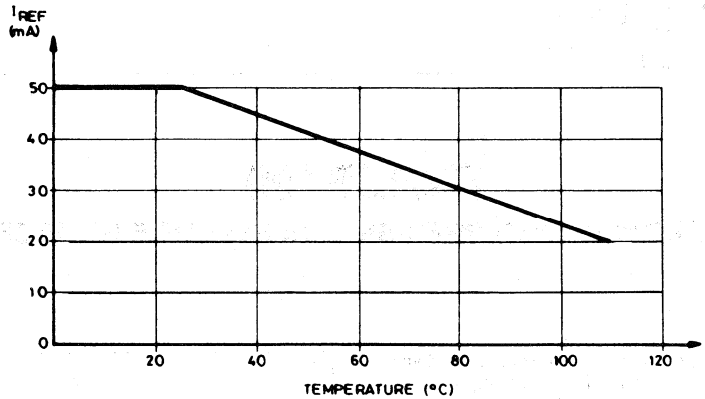



*Fig.4 $I_{REF}$ derating for ZNREF062*

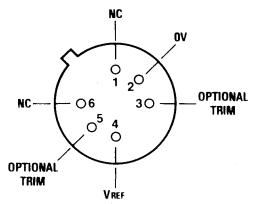
# ZNREF100

## 10V LOW POWER PRECISION REFERENCE SOURCE

The ZNREF100 is a monolithic integrated circuit providing a precise stable reference voltage of 9.80V at 500$\mu$A.

The circuit features a knee current of 150$\mu$A and operation over a wide range of temperatures and currents.

The ZNREF100 is available in a 6-pin metal can package with pins 3 and 5 offering a trim facility whereby the output voltage can be adjusted as shown in Fig.1. This facility is used when compensating for system errors or setting the reference output to a particular value. When the trim facility is not used, pins 3 and 5 should be left open circuit.




No connection should be made to pins 1 and 6

CM6

*Pin connections (bottom view)*

### FEATURES

- Trimmable Output
- Excellent Temperature Stability
- Low Output Noise Figure
- Available in Two Temperature Ranges
- 1 and 2% Initial Voltage Tolerance Versions Available
- No External Stabilising Capacitor required in most cases
- Low Slope Resistance

### ORDERING INFORMATION

| Device type | Tol. (%) | Temperature Range |
|---|---|---|
| **ZNREF100 A1** | 1 | –55°C to +125°C |
| **ZNREF100 C1** | 1 | 0°C to +70°C |
| **ZNREF100 C2** | 2 | 0°C to +70°C |

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Reference current | 50mA* |
| Power dissipation | 500mW |
| Operating temperature range | See ordering information |
| Storage temperature range | -55°C to +175°C |
| Soldering temperature for a maximum time of 10s | |
| Within 1/16 in of the seating plane | 300°C |
| Within 1/32 in of the seating plane | 265°C |

*Above 25°C this figure should be linearly derated to 16mA at +125°C.

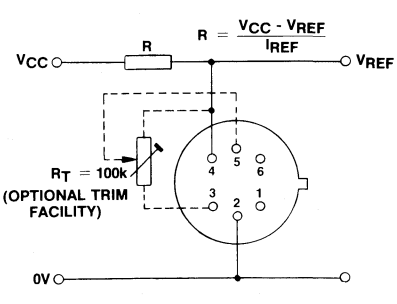



*Fig.1 ZNREF100 application circuit*

## TEMPERATURE DEPENDENT ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Initial voltage tolerance % | Grade A −55 to 125°C | | Grade C 0 to 70°C | | Units |
|---|---|---|---|---|---|---|---|
| | | | Typ. | Max. | Typ. | Max. | |
| Output voltage change over relevant temperature range (See note (a)) | $\Delta V_{REF}$ | 1 & 2 | 64 | 90 | 10.8 | 34.4 | mV |
| Output voltage temperature coefficient (See note (b)) | $TCV_{REF}$ | 1 & 2 | 35 | 50 | 15 | 50 | ppm/°C |

**ELECTRICAL CHARACTERISTICS** (at $T_{amb} = 25°C$ and pins 3 and 5 o/c unless otherwise noted).

| Parameter | Symbol | Min. | Typ. | Max. | Units | Comments |
|---|---|---|---|---|---|---|
| Output voltage<br>1% tolerance (A1 C1)<br>2% tolerance (C2) | $V_{REF}$ | <br>9.70<br>9.60 | <br>9.80<br>9.80 | <br>9.90<br>10.00 | V | $I_{REF} = 500\mu A$ |
| Output voltage adjustment range | $\Delta V_{TRIM}$ | – | ±2.5 | – | % | $R_T = 100k\Omega$ |
| Change in $TCV_{REF}$ with output adjustment | $TC\Delta V_{TRIM}$ | – | 0.8 | – | ppm/°C/% | |
| Operating current range | $I_{REF}$ | 0.15 | – | 50 | mA | See note (c) |
| Turn-on time<br>Turn-off time | $t_{on}$<br>$t_{off}$ | –<br>– | 40<br>0.3 | –<br>– | μs | $R_L = 1k\Omega$ |
| Output voltage noise (over the range 0.1 to 10Hz) | $e_{np-p}$ | – | 50 | – | μV | Peak to peak measurement |
| Slope resistance | $R_{REF}$ | – | 3 | 4 | Ω | $I_{REF}$ 0.5mA to 5mA, See note (d) |

### NOTES

**(a) Output change with temperature ($\Delta V_{REF}$)**
The absolute maximum difference between the maximum output voltage and the minimum output voltage over the specified temperature range

$$\Delta V_{REF} = V_{max} - V_{min}$$

**(b) Output temperature coefficient ($TCV_{REF}$)**
The ratio of the output change with temperature to the specified temperature range expressed in ppm/°C.

$$TCV_{REF} = \frac{\Delta V_{REF} \times 10^6}{V_{REF} \times \Delta T} \text{ ppm/°C}$$

$\Delta T$ = Full temperature change.

**(c) Operating current ($I_{REF}$)**
Maximum operating current must be derated as indicated in maximum ratings.

**(d) Slope resistance ($R_{REF}$)**
The slope resistance is defined as $R_{REF}$ = change in $V_{REF}$ overspecified current range

$\Delta I_{REF} = 5 - 0.5 = 4.5mA$ (typically)

**(e) Line regulation**

The ratio of change in output voltage to the change in input voltage producing it.

$$\frac{R_{REF} \times 100}{V_{REF} \times R_S} \text{ %/V}$$ $R_S$ = Source resistance

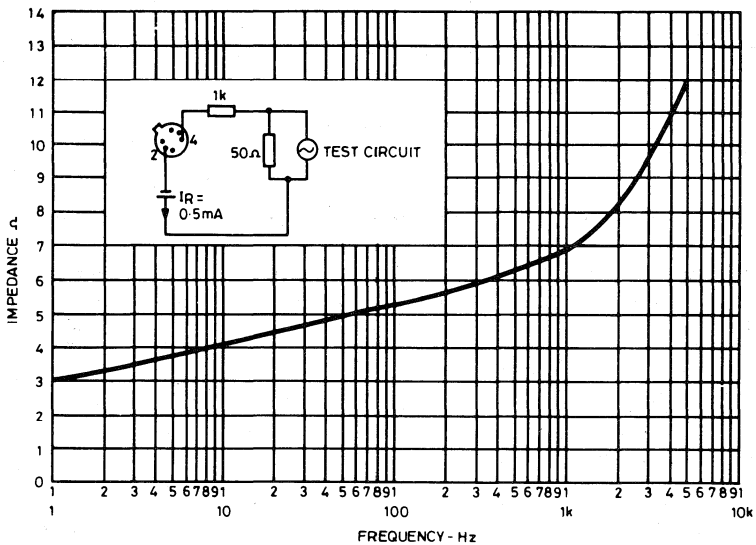



*Fig.2 Dynamic impedance (typical)*

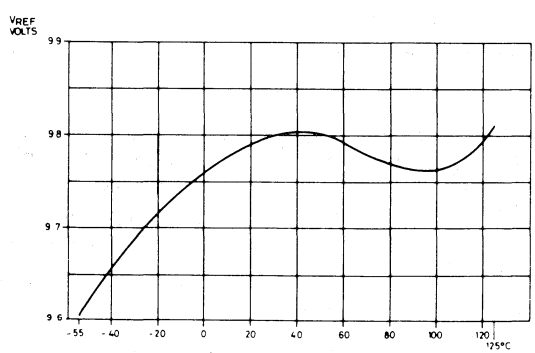



*Fig.3 Typical temperature characteristics*

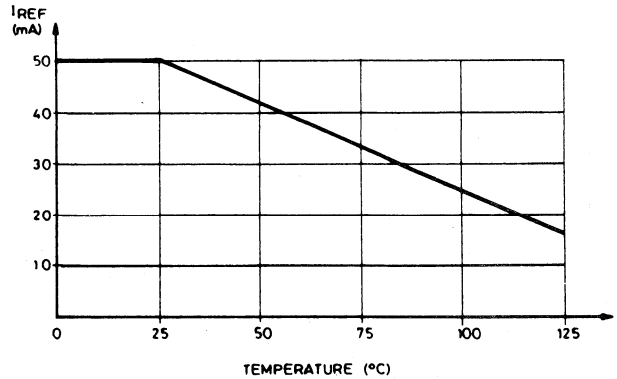



*Fig.4 $I_{REF}$ derating for ZNREF100*

# Section 3
## Networking and Communications

# MJ2812/13

## 32 WORDS × 8/9 BIT FIFO MEMORIES

The MJ2812 and MJ2813 are 32-word by 8-bit and 9-bit first-in first-out memories, respectively. Both devices have completely independent read and write controls and have three state outputs controlled by an output enable pin (OE). Data on the data inputs ($D_O$ – $D_7$) is written into the memory by a pulse on load (PL). The data word automatically ripples through the memory until it reaches the output or another data word.

Data is read from the memory by applying a shift out pulse on PD. This dumps the word on the outputs ($Q_O$ – $Q_7$) and the next word in the buffer moves to the output. An output ready signal (OR) indicates that data is available at the output and also provides a memory empty signal. An input ready signal (IR) indicates that the device is ready to accept data and also provides a memory full signal.

Both the MJ2812 and MJ2813 have master reset inputs which initialise the FIFO control logic and clear all data from the device (reset to all lows). A FLAG signal goes high when the memory is approximately half full.

The MJ2812 can perform input and output data transfer on a bit-serial basis as well as on 8-bit parallel words. The input buffer is an 8-bit shift register which can be loaded in parallel by the PL command or can be loaded serially through the $D_O$ input by using the SL clock. When 8 bits have been shifted into the input buffer serially, the 8-bit word automatically moves in parallel through the memory. The output includes a built in parallel-to-serial converter, so that data can be shifted out of the Q7 output by using the SD clock. After 8 clock pulses a new 8-bit word appears at the outputs.

The timing and function of the four control signals PL, IR, PD and OR are designed so that two FIFOs can be placed end-to-end, with OR of the first driving PL of the second and IR of the second driving PD of the first. With this simple interconnection, strings of FIFOs can control each other reliably to make a FIFO array any number of words deep.

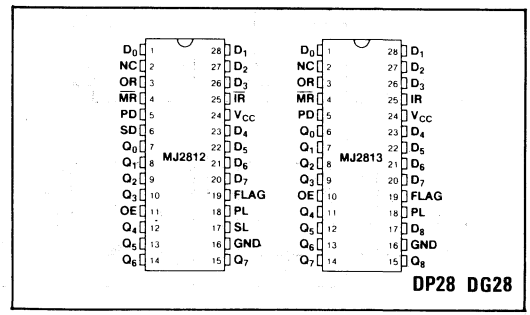



*Fig.1 MJ2812 (32×8) and MJ2813 (32×9) pin connections (top view).*

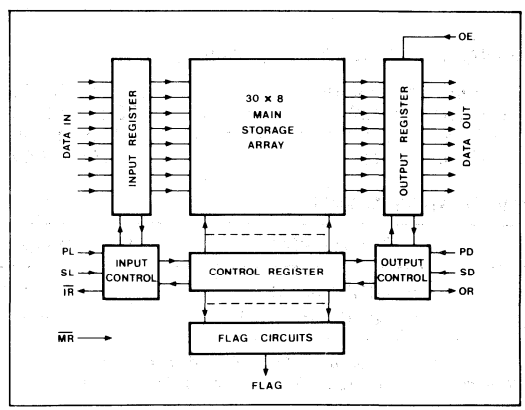



*Fig.2 MJ2812 simplified block diagram*

### FEATURES

- Serial or Parallel Inputs and Outputs (MJ2812)
- 32 Words × 8 Bits (MJ2812) and 32 Words × 9 Bits (MJ2813)
- Easily Stacked - Sideways or Lengthways
- Independent Reading and Writing
- Half-Full Flag
- Data Rates up to 2.0MHz
- Last Word Retention
- TTL-Compatible Tristate Outputs
- Input and Output Ready Signals
- Master Reset
- Single + 5V Supply
- Commercial (0°C to + 70°C) and Military (–55°C to + 125°C) Operating Temperatures

### APPLICATIONS

- Smoothing Data Rates from Keyboards
- Buffer between Differently-Clocked Systems (Short Fast Bursts into Steady Data Stream and Vice Versa)
- Temporary Storage in Error Removing Systems which use Repeated Transmission
- Buffer Store in Interrupt-Orientated Systems
- Computer to Line Printer Buffer

### ORDERING INFORMATION

**MJ2812 DG** (Commercial - Ceramic DIL package)
**MJ2812 DP** (Commercial - Plastic DIL package)
**MJ2812 MB DG** (Military - Ceramic DIL package and Plessey High Reliability screening)
**MJ2813 DG** (Commercial - Ceramic DIL package)
**MJ2813 DP** (Commercial - Plastic DIL package)
**MJ2813 MB DG** (Military - Ceramic DIL package and Plessey High Reliability screening)

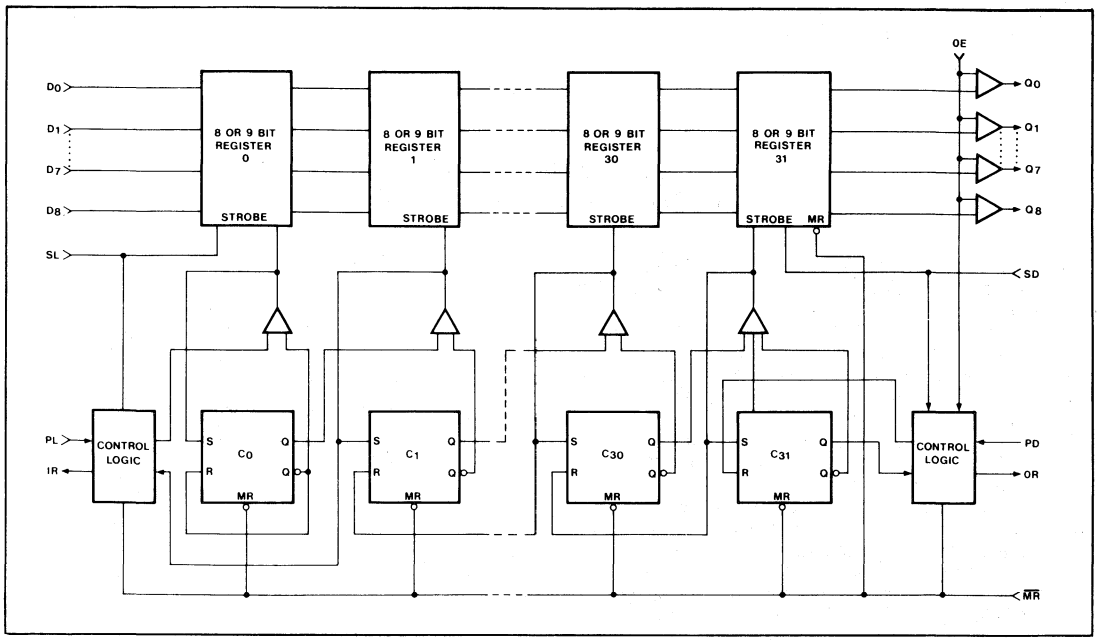



*Fig.3 Logic block diagram*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage temperature | −65°C to +150°C |
| Temperature (ambient) under bias | −55°C to +125°C |
| Voltage on any pin w.r.t. ground (0V) | −0.3V to +9V |
| DC input voltage | −0.3V to +6V |

## OPERATING RANGE

| Type number | Ambient temperature | $V_{CC}$ | Ground |
|---|---|---|---|
| MJ2812/MJ2813 | 0°C to +70°C | 5.0V ±5% | 0V |
| MJ2812M/MJ2813M * | −55°C to +125°C | 5.0V ±5% | 0V |

*These parts are only offered with the addition of High Reliability Screening (see Ordering Information on p.1).

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

As specified in Operating Range table (above)

**Static Characteristics**

| Characteristic | Symbol | Value | | | Unit | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output high voltage | $V_{OH}$ | 2.4 | | | V | $I_{OH}$ = −0.3mA |
| Output low voltage | $V_{OL}$ | | | 0.4 | V | $I_{OL}$ = 1.6mA |
| Input high voltage | $V_{IH}$ | 2.5 | | | V | |
| Input low voltage | $V_{IL}$ | | | 0.8 | V | |
| Input leakage current | $I_{IL}$ | | | 10 | μA | $V_{IN}$ = 0V |
| Input high current | $I_{IH}$ | | | 10 | μA | $V_{IN}$ = 0'5.25V |
| $V_{CC}$ curent | $I_{CC}$ | | 70 | 114 | mA | $T_{AMB}$ = 0°C to + 70°C |
| | | | 70 | 120 | mA | $T_{AMB}$ = −55°C to + 125°C |
| OFF state output current, Q0-Q8 | $I_{OFFL}$ | | | −50 | μA | $T_{AMB}$ = 0°C to + 70°C |
| | $I_{OFFH}$ | | | + 50 | μA | $T_{AMB}$ = 0°C to + 70°C |

## Switching Characteristics

| Characteristic | Symbol | Type | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Maximum parallel load or dump frequency | $f_p$ | 2812/13 | 2.05 | | | MHz | |
| | | 2812M/13M | 1.5 | | | MHz | |
| Delay, PL or SL high to IR inactive | $t_{IR+}$ | 2812/13 | | 90 | 200 | ns | |
| | | 2812M/13M | | 90 | 250 | ns | |
| Delay, PL or SL low to IR active | $t_{IR-}$ | 2812/13 | | 140 | 350 | ns | |
| | | 2812M/13M | | 140 | 400 | ns | |
| Minimum PL or PD high time | $t_{pwH(P)}$ | All | | | 80 | ns | |
| Minimum PL or PD low time | $t_{pwL(P)}$ | All | | | 100 | ns | |
| Minimum SL or SD high time | $t_{pwH(S)}$ | All | | | 80 | ns | |
| Minimum SL or SD low time | $t_{pwl(S)}$ | All | | | 80 | ns | |
| Data hold time | $t_{h(D)}$ | All | | 130 | 200 | ns | |
| Data set-up time | $t_{s(D)}$ | All | | | 0 | ns | to PL |
| | | All | | | 0 | ns | to SL |
| Delay, PD or SD high to OR low | $t_{OR+}$ | 2812/13 | | 110 | 240 | ns | OE high |
| | | 2812M/13M | | 110 | 260 | ns | OE high |
| Delay, PD or SD low to OR high | $t_{OR-}$ | 2812/13 | | 180 | 400 | ns | DE high |
| | | 2812M/13M | | 180 | 400 | ns | DE high |
| Ripple through time | $t_{PT}$ | 2812/13 | | 1.0 | 2.5 | µs | FIFO empty |
| | | 2812M/13M | | 1.0 | 3.0 | µs | FIFO empty |
| Delay, OR low to data out changing | $t_{DH}$ | All | | 90 | | ns | PD=low |
| Delay, data out to OR high | $t_{DA}$ | All | | 70 | | ns | PD=high |
| Minimum reset pulse width | $t_{MRW}$ | 2812/13 | | | 290 | ns | |
| | | 2812M/13M | | | 300 | ns | |
| Delay, OE low to output off | $t_{DO}$ | All | | | 250 | ns | |
| Delay, OE high to output active | $t_{EO}$ | All | | | 250 | ns | |
| Delay from PL or SL low to FLAG high or PD or SD low to FLAG low | $t_{DF}$ | All | | | 1.0 | µs | |
| Input capacitance | $c_I$ | All | | | 7 | pF | |

NOTES
1. IR is active high on MJ2813 and active low on MJ2812
2. Minimum and maximum delays generally occur at opposite temperature extremes. Devices at approximately the same temperature will have compatible switching characteristics and will drive each other.

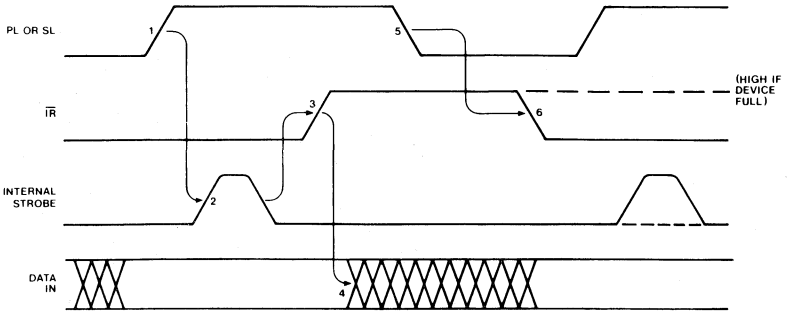
## MJ2812 AND MJ2813 FIFO OPERATION

The MJ2812 and MJ2813 FIFO's consist internally of 32 data registers and one 32-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the (n)th bit of the control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the (n)th data register, simultaneously setting the (n+1)th control register bit and clearing the (n)th control register bit, so that the control strobe moves with the data. In this fashion data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the data inputs by applying a low-to-high transition on the parallel load (PL) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned buffered, to the input ready (IR) output, and this pin goes inactive indicating that data has been entered into the first data register and the input is now 'busy', unable to accept more data. When PL next goes low, the fall-through process begins (assuming that at least the second location is empty). The data in the first register is copied into the second, and the first control register bit is cleared. This caused IR to go active, indicating the inputs are available for another data word.

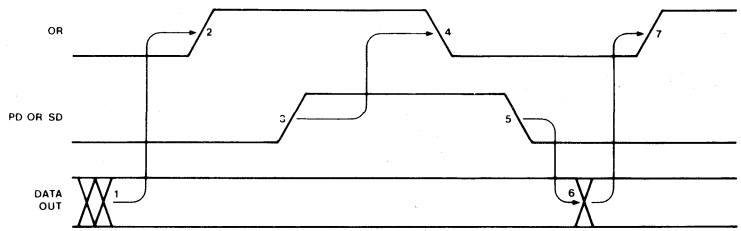
Note: The device will malfunction if a data load is attempted when the inputs are not ready (as indicated by the IR output signals).

The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output Ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the data outputs. A parallel dump command is used to shift the data word out of the FIFO. A low-to-high transition on PD clears the last register bit, causing OR to go LOW, indicating that the data on the




**MJ2812 INPUT TIMING**

When data is steady PL is brought high (1) causing internal data strobe to be generated (2). When data has been loaded, $\overline{IR}$ goes high (3) and data may be changed (4). $\overline{IR}$ remains high until PL is brought low (5); then $\overline{IR}$ goes low (6) indicating new data may be entered.




**MJ2812 OUTPUT TIMING**

When data out is steady (1), OR goes high (2). When PD goes high (3), OR goes low (4). When PD goes low again (5), the output data changes (6) and OR returns high (7).

The input and output timing diagram above illustrate the sequence of control on the MJ2812. Note that PL matches OR and $\overline{IR}$ matches PD in time, as though the signals were driving each other. The MJ2813 pattern is similar, but IR is active high instead of active low.

*Fig.4 MJ2812 timing diagram*

outputs may no longer be valid. When PD goes low, the '0' which is now present at the last control register bit allows the data in the next to the last register to move into the last register position and on to the outputs. The '0' in the control register than 'bubbles' back toward the input as the data shifts toward the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and PD goes high, OR will go low as before, but when PD next goes low, there is no data to move into the last location, so OR remains low until more data arrives at the output. The previous word is retained at the output. Similarly, when the memory is full data written into the first location will not shift into the second when PL goes low, and IR will remain inactive instead of returning to an active state.

The pairs of input and output control signals are designed so that the PD input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the PL input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

Because the input ready signal is active low on the MJ2812 a peculiarity occurs when several devices are placed end-to-end. When the second unit of two MJ2812 fills up, the data out of the first is not dumped immediately. That is, no shift out command occurs, so that the data last written into the second device remains on the output of the first until an empty location bubbles up from the output. The net effect is that n MJ2812s connected end-to-end store 31n+1 words (instead of 32n). The MJ2813 stores 32n words in this configuration, because IR is active high and does dump the last word written into the second device.

## Flag Output

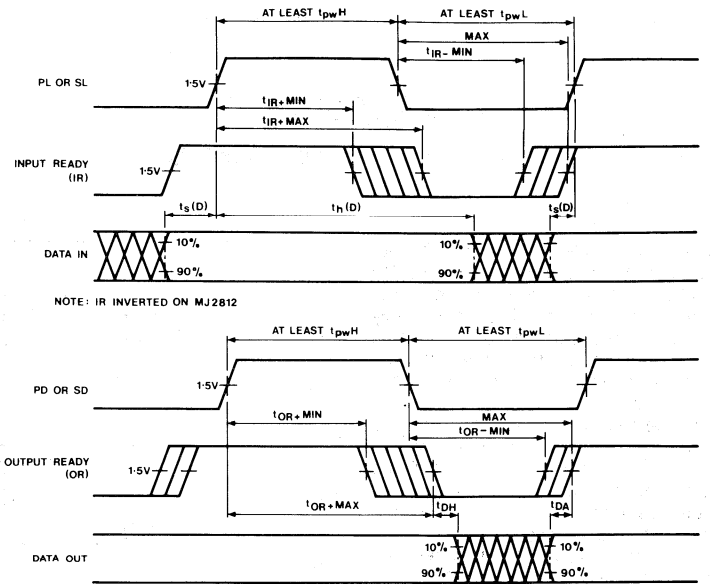
A flag output is available on the MJ2812 and MJ2813 to indicate when the FIFO is approximately half full. Assuming the memory is empty, the flag output will go high within 1µs of the 13th word being loaded into the memory (14 high-low transitions on PL or 112 transitions on SL). Assuming a full memory the flag output will go low within 1µs of the 20th PD or 160th SD high-low transition, ie. when 13 words remain in the memory.

## Serial Input and Output (MJ2812 Only)

The MJ2812 also has the ability to read or write serial bit streams, rather than 8-bit words. The device then works like a 256 by 1-bit FIFO. A serial data stream can be loaded into the device by using the serial load input and applying data to $D_0$ input.

The SL signal operates just like the PL input, causing $\overline{IR}$ to go high and low as the bits are entered. The data is simply shifted across the 8-bit input register until 8 bits have been entered; the 8 bits then fall through the register as though they have been loaded in parallel. Following the 8th SL pulse, $\overline{IR}$ will remain inactive if the FIFO is full.

A corresponding operation occurs on the output, with clock pulses on SD causing successive bits of data to appear on the $Q_7$ output. OR moves high and low with SD exactly as it does with PD. When 8 bits have been shifted out, the




**KEY TO TIMING DIAGRAM**

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| ——— | MUST BE STEADY | WILL BE STEADY |
| ⟋⟍ | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| ⟍⟋ | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| ⟋⟍⟋⟍ | DONT CARE ANY CHANGE PERMITTED | CHANGING STATE UNKNOWN |

*Fig.5 timing diagram*

next word appears at the output. If a PD command is applied after the 8 bits on the outputs have been partially shifted out, the remainder of the word is dumped and the new 8-bit word is brought to the output. OR will stay low if the FIFO is empty.

When the serial input or output clock is used, the corresponding parallel control line should be grounded and when the PD or PL controls are used the corresponding serial clocks should be grounded.

## OPERATING NOTES

1. When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However, OR will remain low, indicating data at the output is not valid.

2. When the output data changes as a result of a pulse on PD, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.

3. If PD is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least $t_{OR+}$) and then will go back low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until PD has been brought low.

4. When the master reset is brought low, the control register and the outputs are cleared and the control logic is initialised. $\overline{IR}$ and OR go low. If PL is high when the master reset goes high then $\overline{IR}$ will remain in the high state until PL is brought low. If PL is low when the master reset is ended, then $\overline{IR}$ will be low until PL goes high.

5. The output enable pin OE inhibits dump commands while it is low and forces the Q outputs to a high impedance state.

6. The serial load and dump lines should not be used for interconnecting two FIFOs. Use the parallel interconnection instead.

7. If less than eight bits have been shifted in using the serial load command, a parallel load pulse will destroy the data in the partially filled input register.

8. The $\overline{IR}$ and OR signals are provided to ensure that data is written into, or read out of, the FIFO correctly. If the specified minimum pulse widths, for PL, SL, PD or SD are not provided *after* an $\overline{IR}$ or OR transition the memory may corrupt and lock out any further data input. The memory should be cleared to restore normal operation.

# MJ2841
## 64 WORD × 4 BIT FIFO MEMORY

The MJ2841 is an asynchronous first-in first-out memory stack, organized as 64 four-bit words. The device accepts a four bit parallel word $D_0$-$D_3$ under control of the shift in (SI) input. Data entered into the FIFO immediately ripples through the device to the outputs $Q_0$-$Q_3$. Up to 64 words may be entered before any words are read from the memory. The stored words line up at the output end in the order in which they were written.

A read command on the shift out input (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals act as memory full and memory empty flags and also provide the necessary pulses for interconnecting FIFO's to obtain deeper stacks.

Parallel expansion to wider words only requires that rows of FIFO's be placed side by side. Reading and writing operations are completely independent, so the device can be used as a buffer between two digital machines operating asynchronously and at widely differing clock rates.

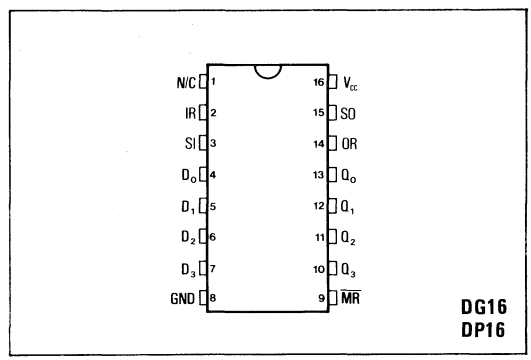



*Fig.1 Pin connections (top view)*

### FEATURES

- Single 5V Supply
- 1.75MHz Guaranteed Data Rate (Typically 4MHz)
- Pin Compatible with AM2841/Fairchild 3341
- Asynchronous Buffer For Up To 64 Four Bit Words
- Easily Expandable To Larger Buffers

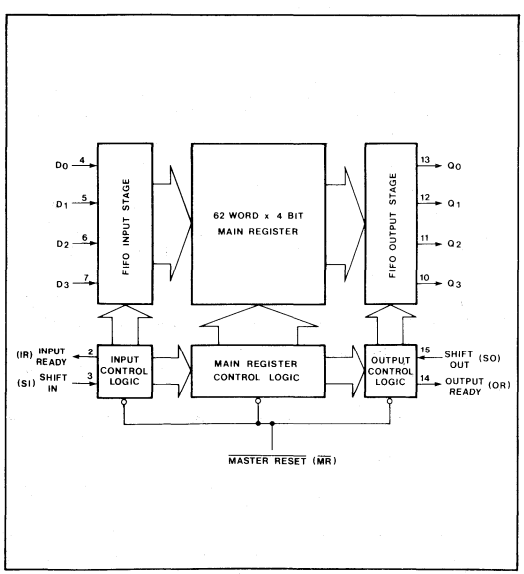



*Fig.2 Block diagram*

### ORDERING INFORMATION

**MJ2841 DG** (Commercial - Ceramic DIL package)
**MJ2841 DP** (Commercial - Plastic DIL package)

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Storage temperature range | -55°C to +125°C |
| Ambient operating temperature | 0°C to +70°C |
| Lead temperature (soldering, 10s max.) | 300°C |
| Voltage on any pin with respect to ground | -0.3V to +7V |

### MJ2841 FIFO OPERATION

The MJ2841 FIFO consists internally of 64 four-bit data registers and one 64-bit control register, as shown in the logic block diagram. A '1' in a bit of the control register indicates that a four-bit data word is stored in the corresponding data register. A '0' in a bit of the control register indicates that the corresponding data register does not contain valid data. The control register directs the movement of data through the data registers. Whenever the $n^{th}$ bit of control register contains a '1' and the (n+1)th bit contains a '0', then a strobe is generated causing the (n+1)th data register to read the contents of the $n^{th}$ data register, simultaneously setting the (n+1)th control register bit, so that the control flag moves with the data. In this fashion, data in the data register moves down the stack of data registers toward the output as long as there are 'empty' locations ahead of it. The fall through operation stops when the data reaches a register n with a '1' in the (n+1)th control register bit, or the end of the register.

Data is initially loaded from the four data inputs $D_0$-$D_3$ by applying a low to high transition on the shift in (SI) input. A '1' is placed in the first control register bit simultaneously. The first control register bit is returned, buffered, to the input ready (IR) output, and this pin goes low indicating that data has been entered into the first data register and

the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the first control register bit is cleared. This causes IR to go high indicating the inputs are available for another data word.

The data falling through the register stacks up at the output end. At the output the last control register bit is buffered and brought out as Output ready (OR). A high on OR indicates there is a '1' in the last control register bit and therefore there is valid data on the four data outputs $Q_0$-$Q_3$. An input signal, shift out (SO) is used to shift the data out of the FIFO. A low to high transition on SO clears the last register bit, causing OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the '0' which is now present at the last register allows the data in the next to last register position to move into the last register position and on to the outputs. The '0' in the control register then 'bubbles' back towards the input as the data shifts towards the output.

If the memory is emptied by reading out all the data, then when the last word is being read out and SO goes high, OR will go low as before, but when SO next goes low, there is no data to move into the last location so OR remains low until more data arrives at the output. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The pairs of input and output control signals are designed so that the SO input of one FIFO can be driven by the IR output of another, and the OR output of the first FIFO can drive the SI input of the second, allowing simple expansion of the FIFO to any depth. Wider buffers are formed by allowing parallel rows of FIFO's to operate together.

An over-riding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the outputs to all low).

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

Supply voltage ($V_{CC}$) = +5V ±5%, $T_{amb}$ = 0°C to +70°C Typical Values at $V_{CC}$ = 5V and $T_{amb}$ = +25°C

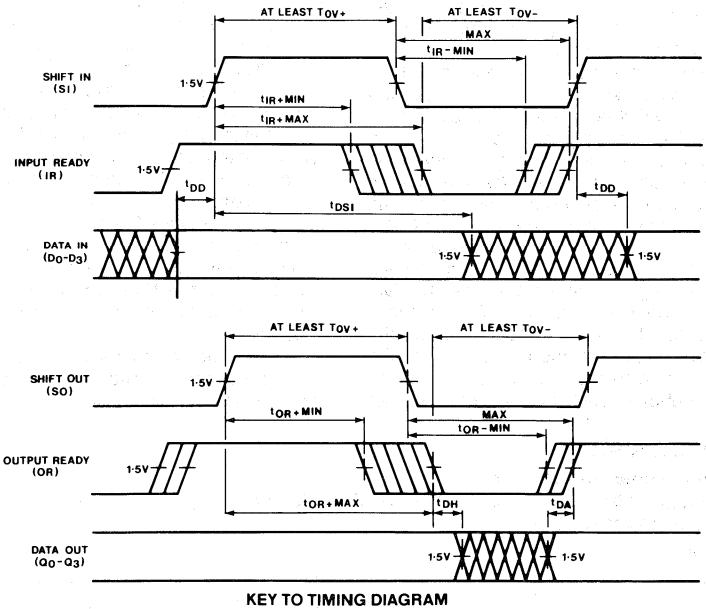
All voltages with respect to ground

### Static Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| O/P high voltage | $V_{OH}$ | 2.7 | 3.2 | | V | $I_{OH}$ = -0.2mA |
| O/P low voltage | $V_{OL}$ | | 0.2 | 0.5 | V | $I_{OL}$ = 2mA |
| I/P high level | $V_{IH}$ | 2.5 | | | V | |
| I/P low level | $V_{IL}$ | | | 0.8 | V | |
| I/P leakage current | $I_{IL}$ | -5 | | +10 | μA | $V_{IN}$ = 0V or 5V |
| Supply current | $I_{CC}$ | | 50 | 81 | mA | |

### Switching Characteristics

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Max. SI or SO frequency | $f_{MAX}$ | 1.75 | 4.4 | | MHz | |
| Delay, SI high to IR low | $t_{IR}+$ | | 50 | 120 | ns | |
| Delay, SI low to IR high | $t_{IR}-$ | | 80 | 200 | ns | |
| Min. time SI and IR both high | $t_{OV}+$ | | <25 | 45 | ns | |
| Min. time SI and IR both low | $t_{OV}-$ | | <25 | 45 | ns | |
| Data release time | $t_{DSI}$ | | 45 | 110 | ns | |
| Data set-up time | $t_{DD}$ | 0 | | | ns | |
| Delay, SO high to OR low | $t_{OR}+$ | | 80 | 190 | ns | |
| Delay, SO low to OR high | $t_{OR}-$ | | 120 | 290 | ns | |
| Ripple through time | $t_{PT}$ | | 2.5 | 7 | μs | FIFO empty |
| Delay, OR low to data out | $t_{DH}$ | 50 | 85 | | ns | SO = low |
| Reset pulse width | $t_{MRW}$ | 50 | 20 | | ns | |
| Delay, data out to OR high | $t_{DA}$ | 0 | 35 | | ns | SO = high |
| Input capacitance | CI | | | 7 | pF | Any pin |




**KEY TO TIMING DIAGRAM**

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | MUST BE STEADY | WILL BE STEADY |
| | MAY CHANGE FROM H TO L | WILL BE CHANGING FROM H TO L |
| | MAY CHANGE FROM L TO H | WILL BE CHANGING FROM L TO H |
| | DONT CARE ANY CHANGE PERMITTED | CHANGING STATE UNKNOWN |

*Fig.3 Timing diagram*

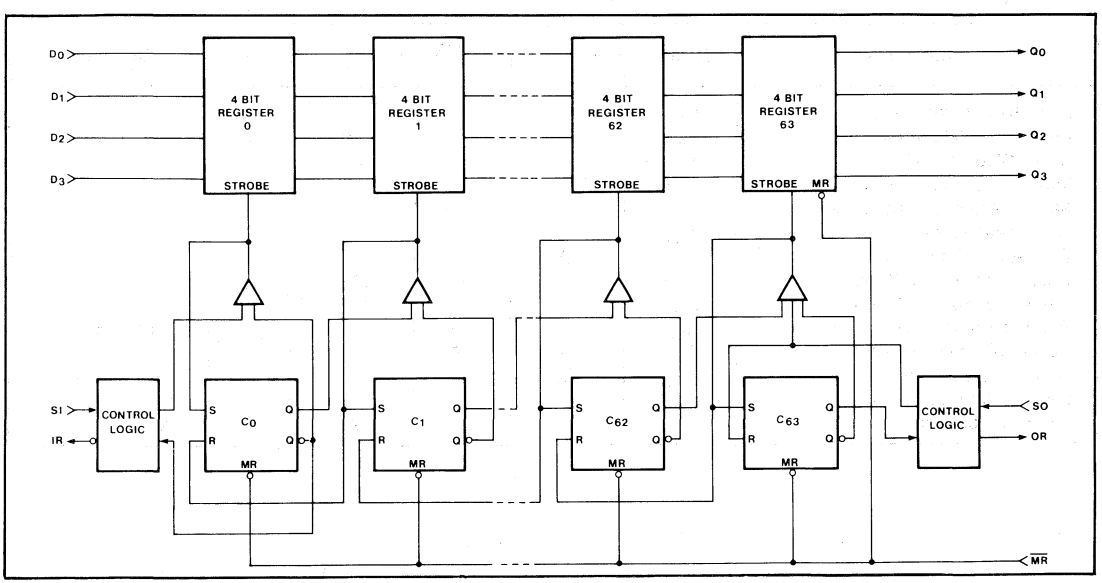



*Fig.4 Logic block diagram*

## OPERATING NOTES

**1.** When the memory is empty the last word read will remain on the outputs until the master reset is strobed or a new data word falls through to the output. However OR will remain low, indicating data at the output is not valid.
**2.** When the output data changes as a result of a pulse on SO, the OR signal always goes low before there is any change in output data and always stays low until after the new data has appeared on the outputs, so anytime OR is high, there is good, stable data on the outputs.
**3.** If SO is held high while the memory is empty and a word is written into the input, then that word will fall through the memory to the output. OR will go high for one internal cycle (at least $t_{OR}+$) and then will go back to low again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought low.
**4.** When the master reset is brought low, the control register and the outputs are cleared. IR goes high and OR goes low. If SI is high when the master reset goes high then the data on the inputs will be written into the memory and IR will return to the low state until SI is brought low. If SI is low when the master reset is ended, the IR will go high, but the data on the inputs will not enter the memory until SI goes high.

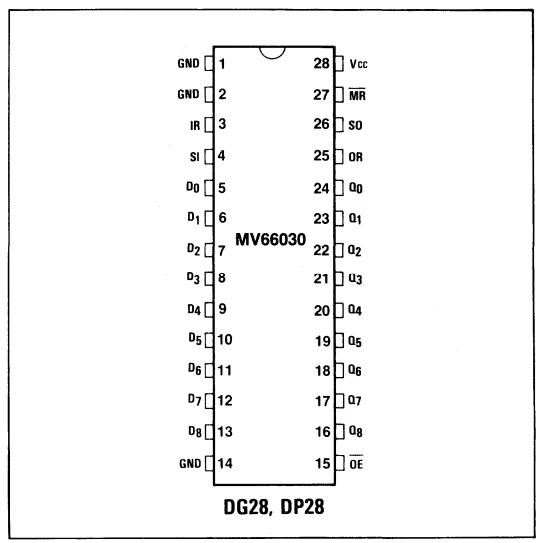
# MV66030

## 64-WORD x 9-BIT FIRST-IN FIRST-OUT MEMORY

The MV66030 is an asynchronous first-in first-out memory, organised as 64 9-bit words. The device accepts a 9-bit parallel word, D0 - D8, under control of the shift in (SI) input. Multiple devices can be used in parallel to satisfy wider data requirements or can be cascaded to any depth to give more words of storage. Data entered into the FIFO ripples through the device to the outputs Q0 - Q8. Up to 64 words may be entered before any words are read from the memory. The stored words stack up at the output in the order in which they were entered.

Activating the shift out control (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals respectively indicate that the device can accept new data or that the output contains valid data. If the input ready output remains inactive, the device is full. If the output ready signal remains inactive, the device is empty.

Since reading and writing operations are completely independent, the device can be used as a buffer between two digital systems operating asynchronously and with widely differing clock frequencies.




**DG28, DP28**

*Fig.1 Pin connections - top view*

### FEATURES

- 25MHz Guaranteed Data Rate when Cascaded (MV66030-25)
- < 200mW at 25MHz
- < 55mW Standby
- Industrial Operating Temperature Range: -40°C to +85°C
- Single 5V Supply, ±10% Tolerance
- Tri-State Outputs

### APPLICATIONS

- Asynchronous Buffer between Digital Systems
- I/O Formatting in DSP Systems
- Video Time Base Correction
- Printer Buffers
- Disk or Tape Interfaces

### ASSOCIATED PRODUCTS

**MV66401/2/3/4** 64x4/5, Bistate/Tristate Cascadable FIFOs
**MJ2812/13** 32x8/9 Cascadable FIFOs
**MJ2841** 64x4 Cascadable FIFO

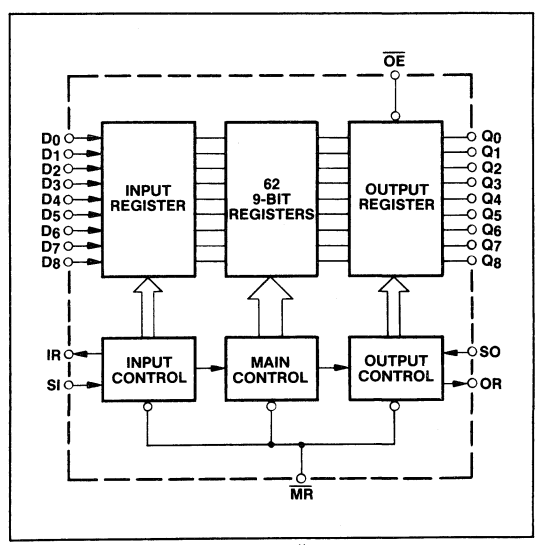



*Fig.2 Block diagram*

## FIFO OPERATION

The MV66030 FIFO contain 64 nine bit data registers. Data is initially loaded from the data inputs D0 - D8 by applying a low to high transition on the shift in (SI) input. IR goes low indicating that data has been entered into the first data register and the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the IR goes high indicating the inputs are available for another data word.

The data falling through the registers stacks up at the output end. A high on OR indicates there is valid data on the data outputs Q0 - Q8. A shift out (SO) can then be used to shift the data out of the FIFO. A low to high transition on SO causes OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the data in the next to last register position moves into the last register position and on to the outputs. If the memory is emptied by reading out all of the data, then, when the last word is being read out and SO goes high, OR will go low as before. When SO next goes low however, there is no data to move into the last location so OR will remain low until more data is entered. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The data word can be extended in width by using more than one FIFO as shown in Fig.10. The status flags must be gated as shown to allow for possible delay variations between devices.

The depth of the FIFO can be extended by tying the data outputs of one device to the data inputs of the next, as shown in Fig.10, the IR input of the receiving device is connected to SO pin of the sending device. Similarly the OR pin of the sending device is connected to the SI pin of the receiving device.

An overriding master reset (MR) is used to reset all control register bits and remove the data from the output (i.e. reset the output to all low).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | -0.5V to 7.0V |
| Input voltage $V_{IN}$ (see Note 3) | -0.9V to $V_{CC}$ +0.9V |
| DC voltage applied to output when high impedance | -0.5V to 7.0V |
| Clamp diode current per pin (see Note 2) | +18mA |
| Storage temperature $T_S$ | -65°C to +150°C |
| Ambient temperature with power applied $T_{amb}$ | -55°C to +125°C |
| Package power dissipation DP | 450mW |
| DG | 1000mW |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Input voltages more negative than -0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply voltage $V_{CC}$ | 5V ± 10% |
| Min. input high level $V_{IH}$ | +2V |
| Max. input low level $V_{IL}$ | +0.8V |
| Ambient temperature | -40°C to 85°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Under Recommended operating conditions

### DC Characteristics

| Characteristic | Symbol | INDUSTRIAL | | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | MV66030-10 | | MV66030-25 | | | |
| | | Min. | Max. | Min. | Max. | | |
| Output high level<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OH}$ = -1mA | $V_{OH}$ | 2.4 | | 2.4 | | V | |
| Output low level<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$, $I_{OL}$ = 8mA | $V_{OL}$ | | 0.5 | | 0.5 | V | |
| Input leakage<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{IN}$ | -10 | +10 | -10 | +10 | μA | |
| Output leakage GND ≤ $V_{OUT}$ ≤ $V_{CC}$<br>$V_{CC}$ = $V_{CC}$ max. | $I_{OZ}$ | -50 | +50 | -50 | +50 | μA | |
| Short circuit current | $I_{OS}$ | | 100 | | 100 | mA | Note 2 |
| Supply current | $I_{CC}$ | | 30 | | 40 | mA | $V_{CC}$ = max.<br>$T_{amb}$ = 85°C<br>$I_{LOAD}$ = 0mA |
| Standby current | | | 10 | | 10 | mA | $V_{CC}$ = max.<br>$I_{LOAD}$ = 0mA<br>All inputs at $V_{IL}$ |

**AC Characteristics - Using test circuit, except where stated.**

| Characteristic | Symbol | INDUSTRIAL | | | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | MV66030-10 | | MV66030-25 | | | |
| | | Min. | Max. | Min. | Max. | | |
| Maximum operating frequency | $f_O$ | 10 | | 25 | | MHz | Note 4 |
| SI HIGH time | $t_{PHSI}$ | 30 | | 15 | | ns | +85°C, 4.5V Note 11 |
| SI LOW time | $t_{PLSI}$ | 40 | | 20 | | ns | |
| Data setup to SI | $t_{SSI}$ | 0 | | 0 | | ns | Note 5 |
| Data hold from SI | $t_{HSI\ (a)}$ | 50 | | 30 | | ns | Note 5,6 |
| | $t_{HSI\ (b)}$ | $t_{PHSI}$ +5 | | $t_{PHSI}$ +5 | | ns | |
| Delay, SI HIGH to IR LOW | $t_{DLIR}$ | | 30 | | 18 | ns | Note 10 |
| Delay, SI LOW to IR HIGH | $t_{DHIR}$ | | 40 | | 22 | ns | Note 10 |
| SO HIGH time | $t_{PHSO}$ | 30 | | 12 | | ns | +85°C, 4.5V Note 11 |
| SO LOW time | $t_{PLSO}$ | 40 | | 20 | | ns | |
| Delay, SO HIGH to OR LOW | $t_{DLOR}$ | | 30 | | 18 | ns | Note 10 |
| Delay, SO LOW to OR HIGH | $t_{DHOR}$ | | 40 | | 22 | ns | Note 10 |
| Data setup to OR HIGH | $t_{SOR}$ | -20 | | -15 | | ns | |
| Data hold from SO LOW | $t_{HSO}$ | 10 | | 8 | | ns | |
| IR pulse HIGH | $t_{PIR}$ | 9 | | 6 | | ns | -40°C, 5.5V Note 11 |
| OR pulse HIGH | $t_{POR}$ | 10 | | 7 | | ns | -40°C, 5.5V Note 11 |
| Data setup to IR | $t_{SIR}$ | 0 | | 0 | | ns | Note 8 |
| Data hold from IR | $t_{HIR}$ | 50 | | 30 | | ns | Note 8 |
| Bubble through time | $t_{BT}$ | | 2400 | | 1200 | ns | |
| $\overline{MR}$ pulse width | $t_{PMR}$ | 60 | | 50 | | ns | Note 9 |
| $\overline{MR}$ HIGH to SI transition | $t_{DSI}$ | 60 | | 50 | | ns | |
| $\overline{MR}$ LOW to OR LOW | $t_{DOR}$ | | 60 | | 50 | ns | |
| $\overline{MR}$ LOW to IR HIGH | $t_{DIR}$ | | 60 | | 50 | ns | |
| $\overline{MR}$ LOW to output LOW | $t_{LZMR}$ | | 60 | | 50 | ns | Note 7 |
| Output valid from $\overline{OE}$ LOW | $t_{OOE}$ | | 60 | | 40 | ns | |
| Output HIGH-Z from $\overline{OE}$ HIGH | $t_{HZOE}$ | | 60 | | 40 | ns | |

NOTES
4. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} + t_{DHOR}$.
5. $t_{SSI}$ and $t_{HSI}$ apply when memory is not full.
6. Hold time is the lesser of the two parameters (a) and (b).
7. All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.
8. These times apply when the device is full and SI is held high.
9. For cascade applications, $t_{PMR}$ must be double that specified.
10. Under cascade conditions.
11. Plessey devices are guaranteed to cascade at 25MHz (under typical operating conditions $t_{PHSI}$ = 10ns, $t_{POR}$ = 13ns, $t_{PHSO}$ = 8ns, $t_{PIR}$ = 12ns).

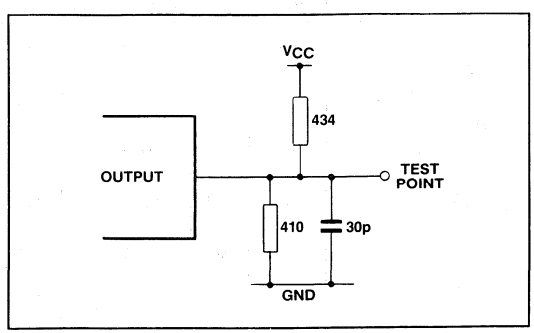



*Fig.3 Test circuit*

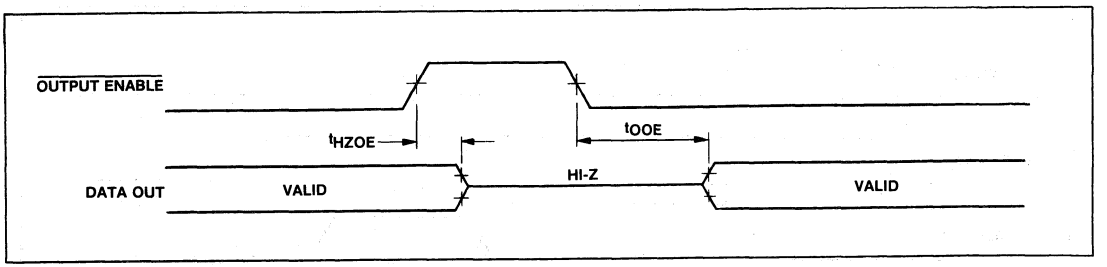



*Fig.4 Output enable timing*

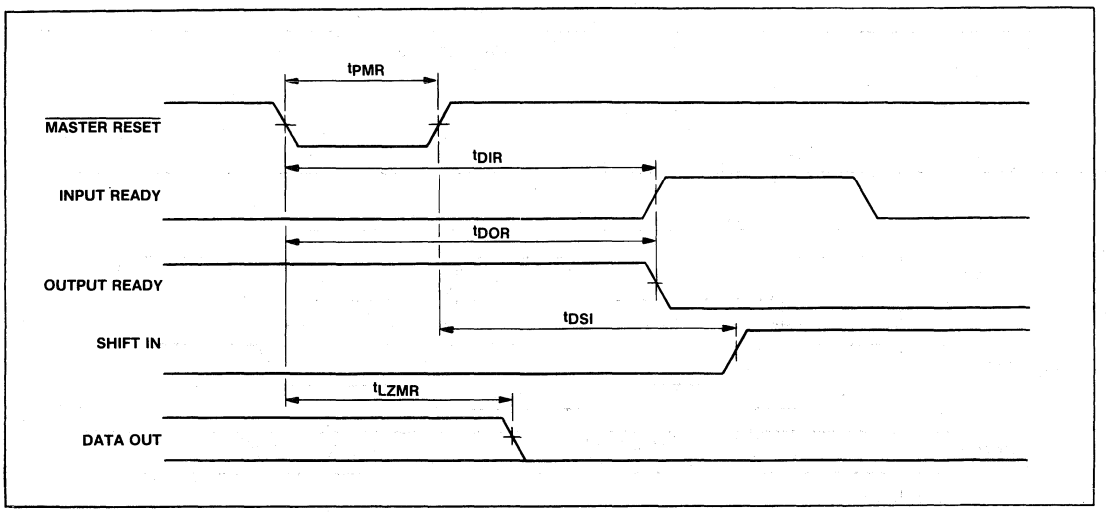



*Fig.5 Master reset timing*

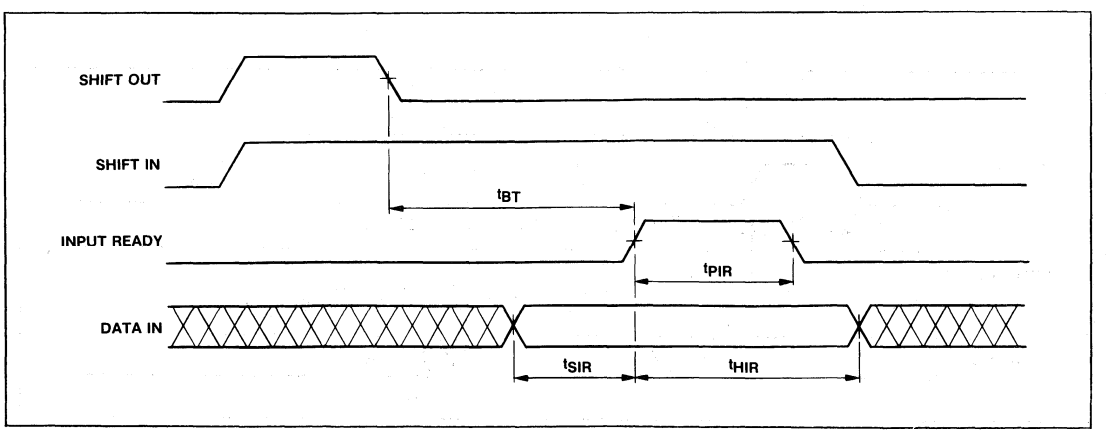



*Fig.6 Data Out to Data In bubble through time*

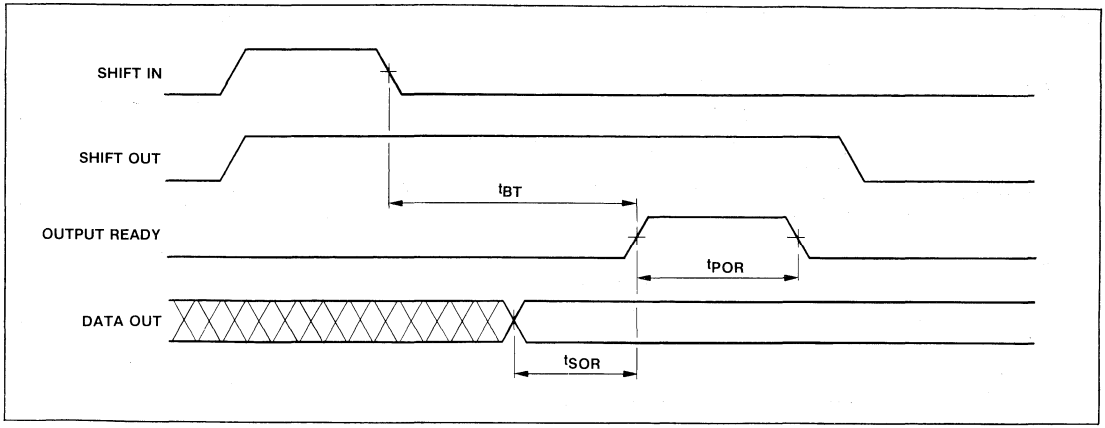



*Fig.7 Data In to Data Out fall through time*

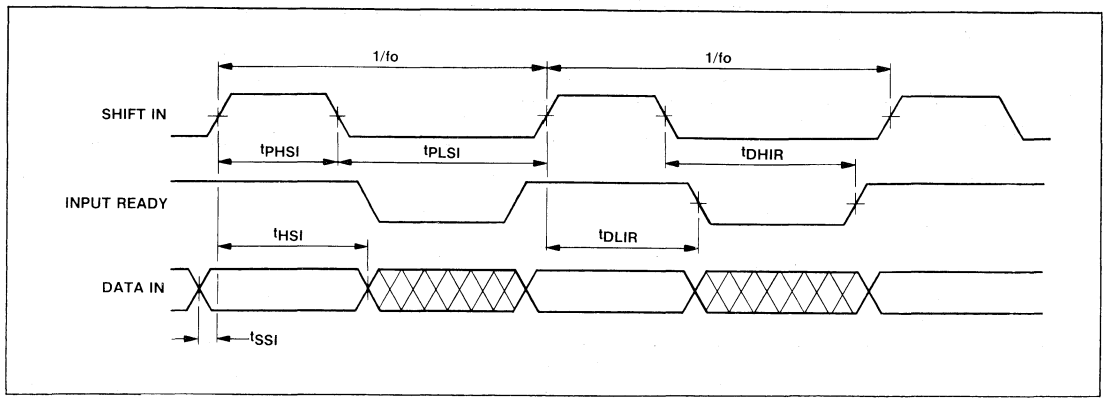



*Fig.8 Switching waveforms - Data In timing*

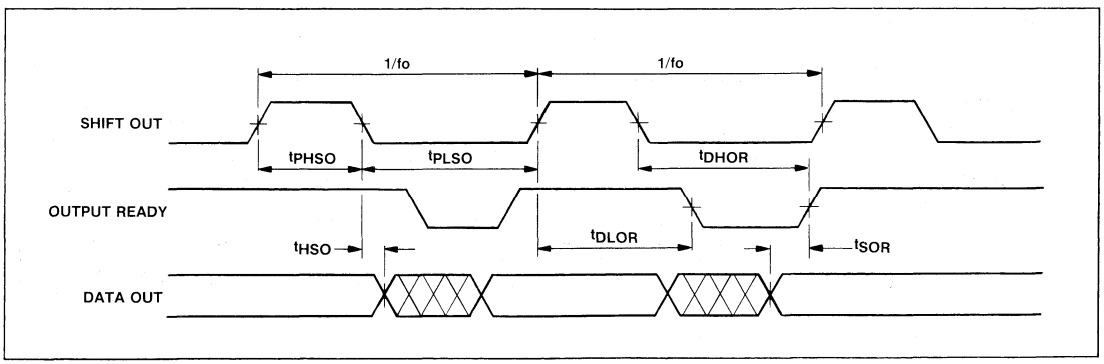



*Fig.9 Switching waveforms - Data Out timing*

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the variation of delays of the FIFOs.

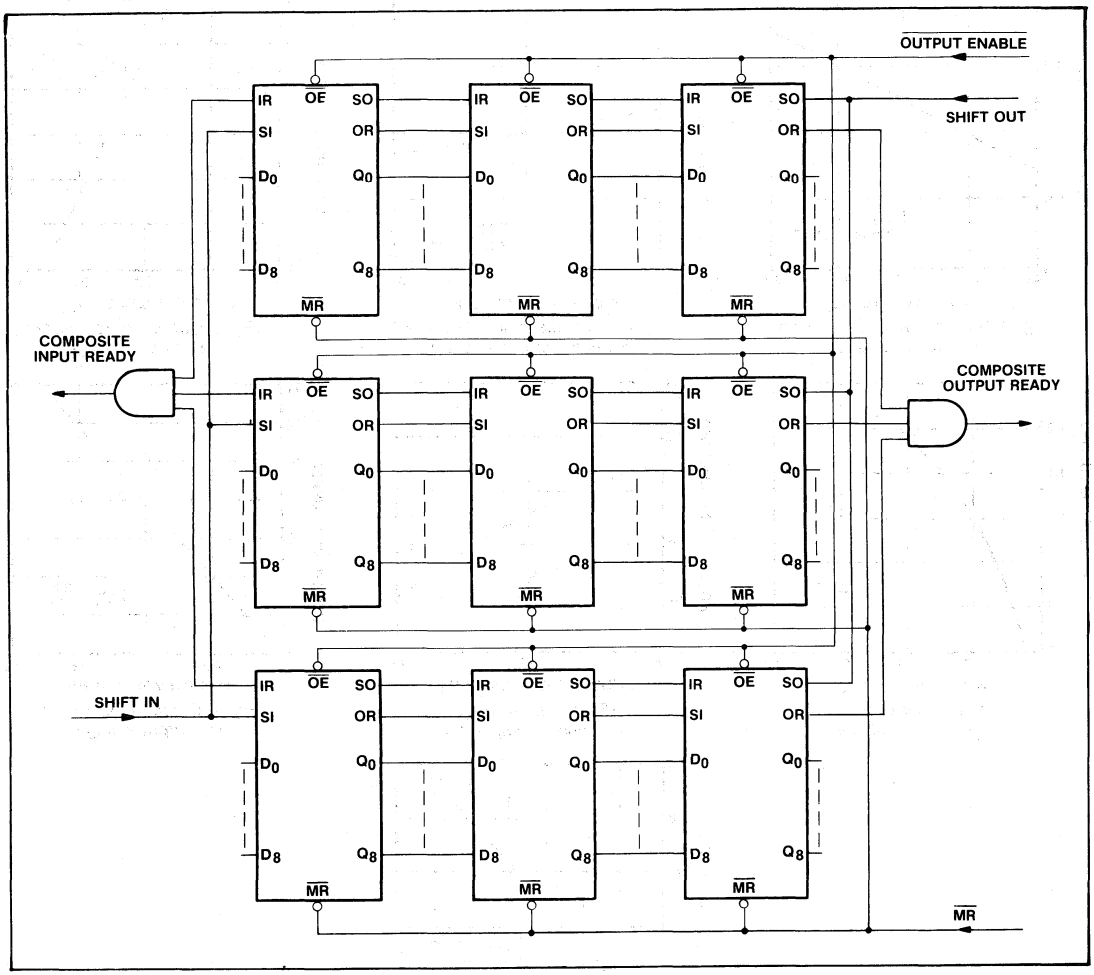



*Fig.10 192 x 27 application*

## USER NOTES

1. When the memory is *empty the last word read will remain on the outputs* until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle ($t_{POR}$) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, the IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. All MV66XXX FIFO's will cascade with other MV66XXX devices, but may not cascade with pin compatible devices from other manufacturers.
6. The IR and OR signals are provided to ensure that data is written into, or read out of, the FIFO correctly. If SI or SO are clocked without reference to these flags, the memory may corrupt and lock out any further data input. The memory should be reset to restore normal operation.

## TYPICAL CHARACTERISTICS

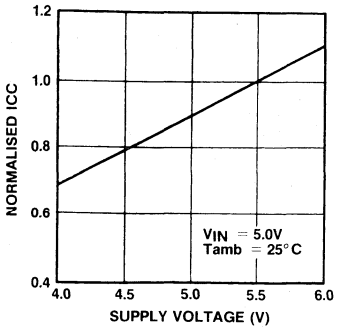



*Fig.11 Normalised supply current vs. supply voltage*

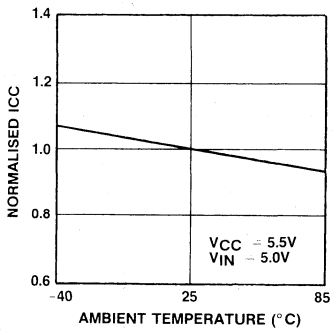



*Fig.12 Normalised supply current vs. ambient temperature*

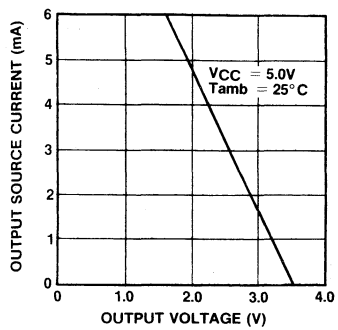



*Fig.13 Output source current vs. output voltage*

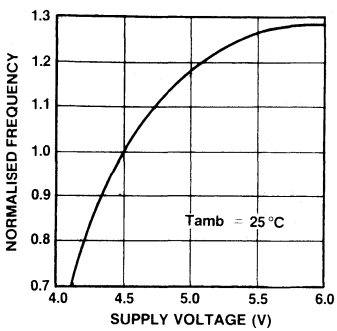



*Fig.14 Normalised frequency vs. supply voltage*

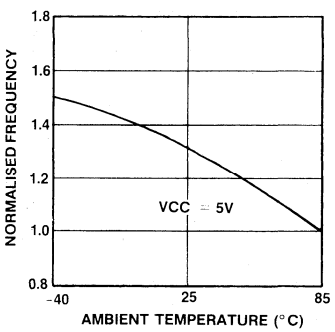



*Fig.15 Normalised frequency vs. ambient temperature*

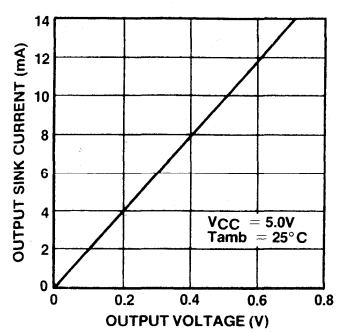



*Fig.16 Output sink current vs. output voltage*

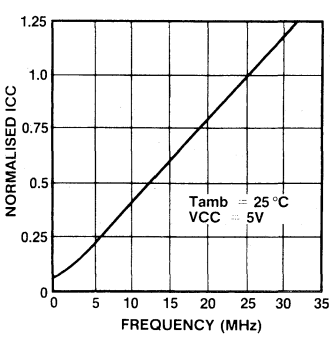



*Fig.17 Normalised Icc vs. frequency*

## ORDERING INFORMATION

**MV66030-10 B0 DG** (Industrial - Ceramic DIL package)
**MV66030-25 B0 DG** (Industrial - Ceramic DIL package)
**MV66030-10 B0 DP** (Industrial - Plastic DIL package)
**MV66030-25 B0 DP** (Industrial - Plastic DIL package)

# MV66401/2/3/4

## 64-WORD x 4/5-BIT FIRST-IN FIRST-OUT MEMORIES

The MV66401/2/3/4 are asynchronous first-in first-out memories, organised as 64 by 4 or 5-bit words. Each device accepts a 4/5-bit parallel word, D0 - D4, under control of the shift in (SI) input. Multiple devices can be used to satisfy wider data requirements. Data entered into the FIFO ripples through the device to the outputs Q0 - Q4. Up to 64 words may be entered before any words are read from the memory. The stored words stack up at the output in the order in which they were entered.

Activating the shift out control (SO) causes the next to the last word of data to move to the output and all data shifts one place down the stack. Input ready (IR) and output ready (OR) signals respectively indicate that the device can accept new data or that the output contains valid data. If the input ready output remains inactive, the device is full. If the output ready signal remains inactive, the device is empty.

Since reading and writing operations are completely independent, the device can be used as a buffer between two digital systems operating asynchronously and with widely differing clock frequencies.

The MV66401/2 are respectively four and five bit devices with TTL compatible outputs. The MV66403/4 have the additional feature of tri-state outputs.

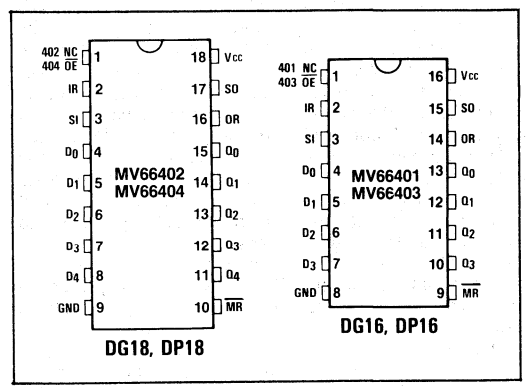



*Fig.1 Pin connections - top view*

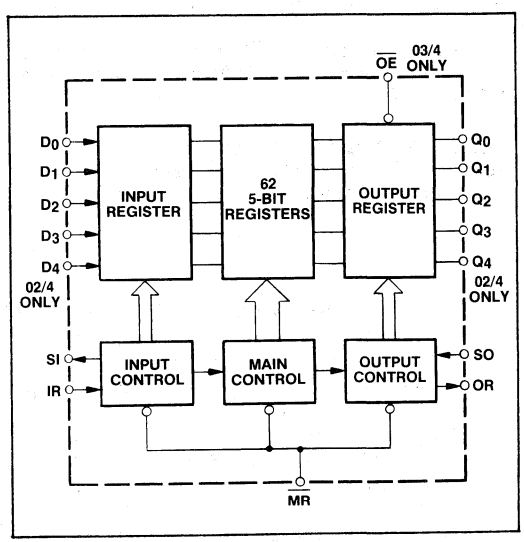



*Fig.2 Block diagram*

### FEATURES

- 25MHz Guaranteed Data Rate when Cascaded (MV66401/2/3/4-25)
- < 200mW at 25MHz
- < 55mW Standby
- Industrial Operating Temperature Range -40°C to +85°C
- Single 5V Supply, ±10% Tolerance
- Tri-State Outputs on the MV66403/4

### APPLICATIONS

- Asynchronous Buffer between Digital Systems
- I/O Formatting in DSP Systems
- Video Time Base Correction
- Printer Buffers
- Disk or Tape Interfaces

### ASSOCIATED PRODUCTS

**MV66030** 64x9, Tristate Cascadable FIFO
**MJ2812/13** 32x8/9 Cascadable FIFOs
**MJ2841** 64x4 Cascadable FIFO

## FIFO OPERATION

The MV66401/2/3/4 FIFOs contain 64 four or five bit data registers. Data is initially loaded from the data inputs D0 - D4 by applying a low to high transition on the shift in (SI) input. IR goes low indicating that data has been entered into the first data register and the input is now 'busy' unable to accept more data. When SI next goes low the fall-through process begins, (assuming that at least the second location is empty). The data in the first register is copied into the second and the IR goes high indicating the inputs are available for another data word.

The data falling through the registers stacks up at the output end. A high on OR indicates there is valid data on the data outputs Q0 - Q4. A shift out (SO) can then be used to shift the data out of the FIFO. A low to high transition on SO causes OR to go low, indicating that the data on the outputs may no longer be valid. When SO goes low, the data in the next to last register position moves into the last register position and on to the outputs. If the memory is emptied by reading out all of the data, then, when the last word is being read out and SO goes high, OR will go low as before. When SO next goes low however, there is no data to move into the last location so OR will remain low until more data is entered. Similarly, when the memory is full, data written into the first location will not shift into the second when SI goes low, and IR will remain low instead of returning to a high state.

The data word can be extended in width by using more than one FIFO as shown in Fig.10. The status flags must be gated as shown to allow for possible delay variations between devices.

The depth of the FIFO can be extended by tying the data outputs of one device to the data inputs of the next, as shown in Fig.11. The IR input of the receiving device is connected to the SO pin of the sending device. Similarly the OR pin of the sending device is connected to the SI pin of the receiving device.

An overriding master reset ($\overline{MR}$) is used to reset all control register bits and remove the data from the output (i.e. reset the output to all low).

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | -0.5V to 7.0V |
| Input voltage $V_{IN}$ (see Note 3) | -0.9V to $V_{CC}$ +0.9V |
| DC voltage applied to output when high impedance | -0.5V to 7.0V |
| Clamp diode current per pin (see Note 2) | +18mA |
| Storage temperature $T_S$ | -65°C to +150°C |
| Ambient temperature with power applied $T_{amb}$ | -55°C to +125°C |
| Package power dissipation DP | 450mW |
| DG | 1000mW |

NOTES
1. Exceeding these ratings may cause permanent damage. Functional operation under these conditions is not implied.
2. Maximum dissipation or 1 second should not be exceeded, only one output to be tested at any one time.
3. Input voltages more negative than -0.9V cause clamp diode current to flow. The maximum negative voltage depends on the source impedance.

## RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply voltage $V_{CC}$ | 5V ± 10% |
| Min. input high level $V_{IH}$ | +2V |
| Max. input low level $V_{IL}$ | +0.8V |
| Ambient temperature | -40°C to 85°C |

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**
Under Recommended operating conditions

### DC Characteristics

| Characteristic | Symbol | INDUSTRIAL | | | | Unit | Conditions |
|---|---|---|---|---|---|---|---|
| | | MV6640X-10 | | MV6640X-25 | | | |
| | | Min. | Max. | Min. | Max. | | |
| Output high level<br>$V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OH} = -1mA$ | $V_{OH}$ | 2.4 | | 2.4 | | V | |
| Output low level<br>$V_{IN} = V_{IH}$ or $V_{IL}$, $I_{OL} = 8mA$ | $V_{OL}$ | | 0.5 | | 0.5 | V | |
| Input leakage<br>$V_{IN} = V_{IH}$ or $V_{IL}$ | $I_{IN}$ | -10 | +10 | -10 | +10 | μA | |
| Output leakage GND ≤ $V_{OUT}$ ≤ $V_{CC}$<br>$V_{CC} = V_{CC}$ max. | $I_{OZ}$ | -50 | +50 | -50 | +50 | μA | |
| Short circuit current | $I_{OS}$ | | 100 | | 100 | mA | Note 2 |
| Supply current | $I_{CC}$ | | 30 | | 40 | mA | $V_{CC}$ = max.<br>$T_{amb}$ = 85°C<br>$I_{LOAD}$ = 0mA |
| Standby current | | | 10 | | 10 | mA | $V_{CC}$ = max.<br>$I_{LOAD}$ = 0mA<br>All inputs at $V_{IL}$ |

**AC Characteristics - Using test circuit, except where stated.**

| Characteristic | Symbol | INDUSTRIAL | | | | Unit | Condition |
|---|---|---|---|---|---|---|---|
| | | MV6640X-10 | | MV6640X-25 | | | |
| | | Min. | Max. | Min. | Max. | | |
| Maximum operating frequency | $f_O$ | 10 | | 25 | | MHz | Note 4 |
| SI HIGH time | $t_{PHSI}$ | 30 | | 15 | | ns | +85°C, 4.5V Note 11 |
| SI LOW time | $t_{PLSI}$ | 40 | | 20 | | ns | |
| Data setup to SI | $t_{SSI}$ | 0 | | 0 | | ns | Note 5 |
| Data hold from SI | $t_{HSI\ (a)}$ | 50 | | 30 | | ns | Note 5,6 |
| | $t_{HSI\ (b)}$ | $t_{PHSI}$ +5 | | $t_{PHSI}$ +5 | | ns | |
| Delay, SI HIGH to IR LOW | $t_{DLIR}$ | | 30 | | 18 | ns | Note 10 |
| Delay, SI LOW to IR HIGH | $t_{DHIR}$ | | 40 | | 22 | ns | Note 10 |
| SO HIGH time | $t_{PHSO}$ | 30 | | 12 | | ns | +85°C, 4.5V Note 11 |
| SO LOW time | $t_{PLSO}$ | 40 | | 20 | | ns | |
| Delay, SO HIGH to OR LOW | $t_{DLOR}$ | | 30 | | 18 | ns | Note 10 |
| Delay, SO LOW to OR HIGH | $t_{DHOR}$ | | 40 | | 22 | ns | Note 10 |
| Data setup to OR HIGH | $t_{SOR}$ | -20 | | -15 | | ns | |
| Data hold from SO LOW | $t_{HSO}$ | 10 | | 8 | | ns | |
| IR pulse HIGH | $t_{PIR}$ | 9 | | 6 | | ns | -40°C, 5.5V Note 11 |
| OR pulse HIGH | $t_{POR}$ | 10 | | 7 | | ns | -40°C, 5.5V Note 11 |
| Data setup to IR | $t_{SIR}$ | 0 | | 0 | | ns | Note 8 |
| Data hold from IR | $t_{HIR}$ | 50 | | 30 | | ns | Note 8 |
| Bubble through time | $t_{BT}$ | | 2400 | | 1200 | ns | |
| $\overline{MR}$ pulse width | $t_{PMR}$ | 60 | | 50 | | ns | Note 9 |
| $\overline{MR}$ HIGH to SI transition | $t_{DSI}$ | 60 | | 50 | | ns | |
| $\overline{MR}$ LOW to OR LOW | $t_{DOR}$ | | 60 | | 50 | ns | |
| $\overline{MR}$ LOW to IR HIGH | $t_{DIR}$ | | 60 | | 50 | ns | |
| $\overline{MR}$ LOW to output LOW | $t_{LZMR}$ | | 60 | | 50 | ns | Note 7 |
| Output valid from $\overline{OE}$ LOW | $t_{OOE}$ | | 60 | | 40 | ns | |
| Output HIGH-Z from $\overline{OE}$ HIGH | $t_{HZOE}$ | | 60 | | 40 | ns | |

NOTES
4. $1/f_O > t_{PHSI} + t_{DHIR}$, $1/f_O > t_{PHSO} + t_{DHOR}$.
5. $t_{SSI}$ and $t_{HSI}$ apply when memory is not full.
6. Hold time is the lesser of the two parameters (a) and (b).
7. All data outputs will be at LOW level after reset goes high until data is entered into the FIFO.
8. These times apply when the device is full and SI is held high.
9. For cascade applications, $t_{PMR}$ must be double that specified.
10. Under cascade conditions.
11. Plessey devices are guaranteed to cascade at 25MHz (under typical operating conditions $t_{PHSI}$ = 10ns, $t_{POR}$ = 13ns, $t_{PHSO}$ = 8ns, $t_{PIR}$ = 12ns).

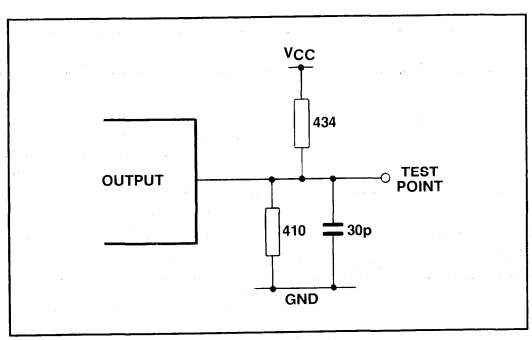



*Fig.3 Test circuit*

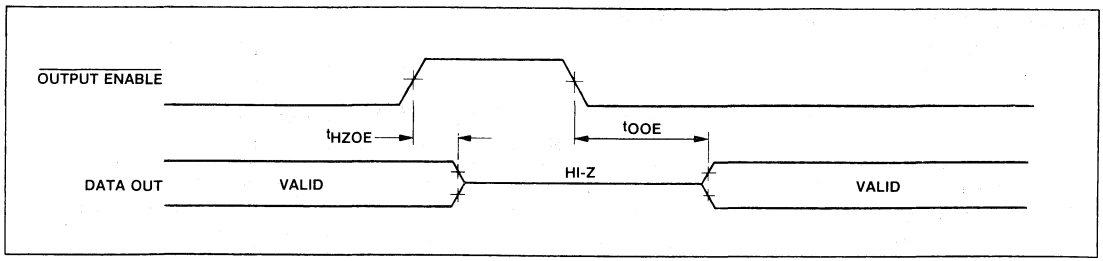



*Fig.4 Output enable timing*

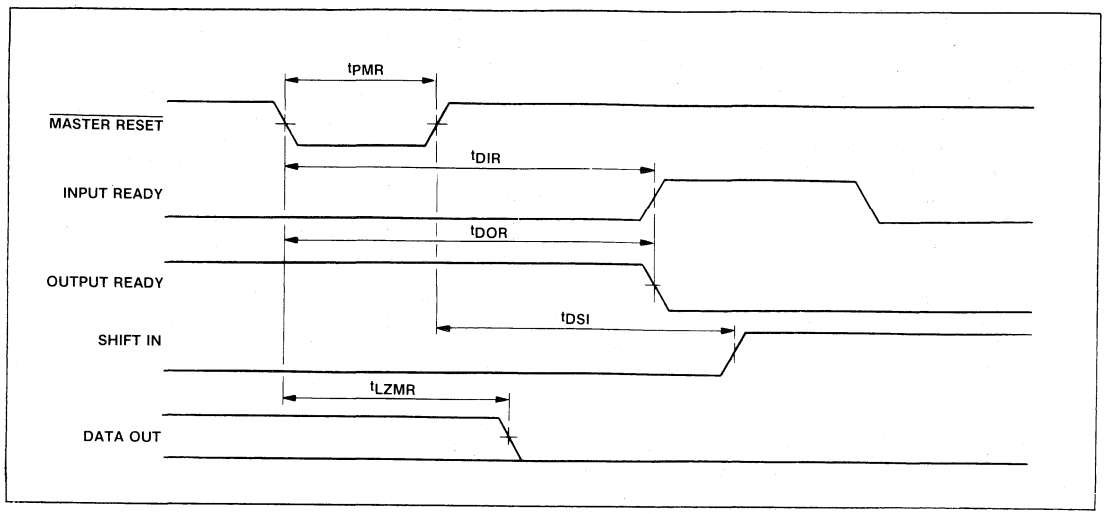



*Fig.5 Master reset timing*

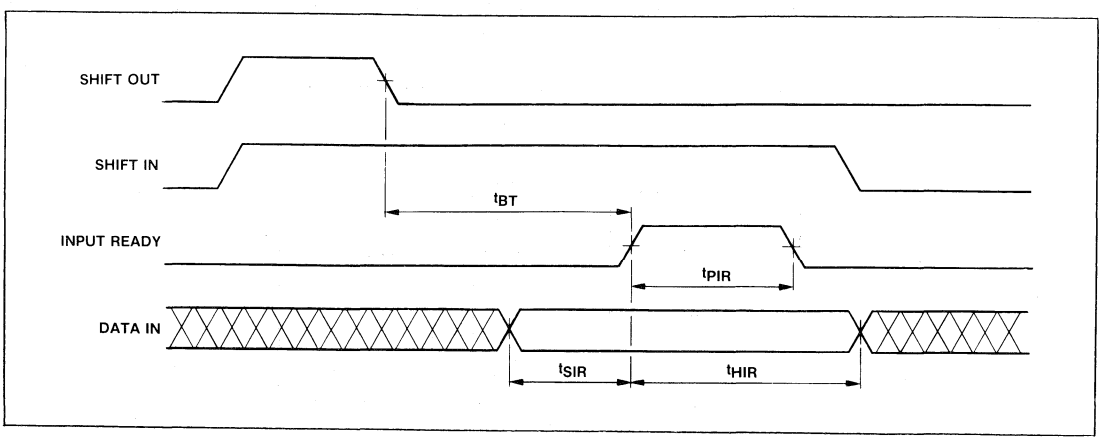



*Fig.6 Data Out to Data In bubble through time*

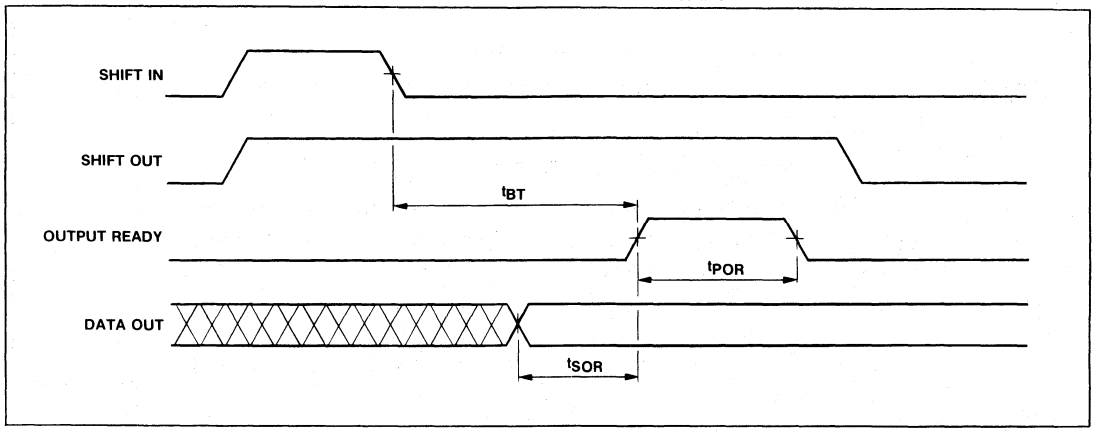



*Fig.7 Data In to Data Out fall through time*

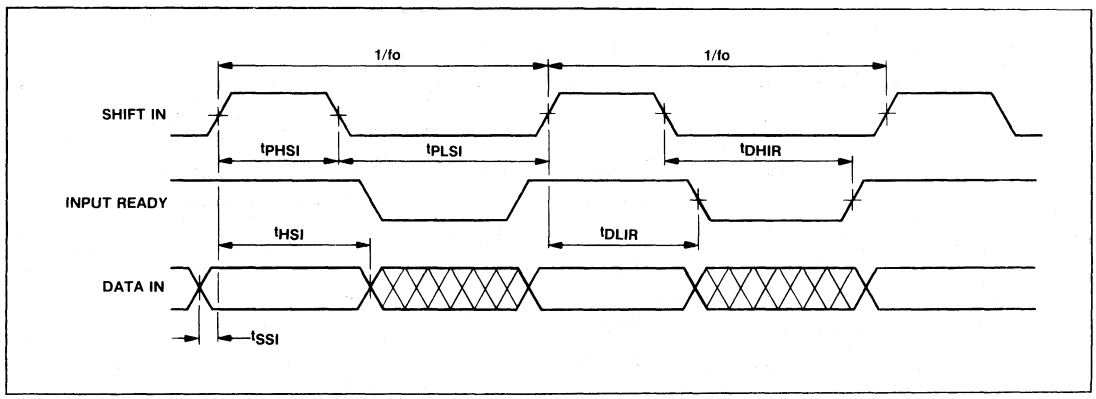



*Fig.8 Switching waveforms - Data In timing*

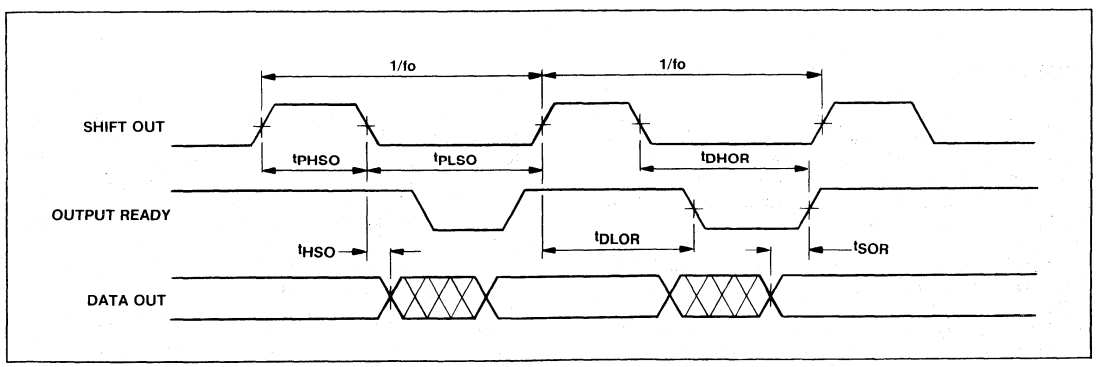



*Fig.9 Switching waveforms - Data Out timing*

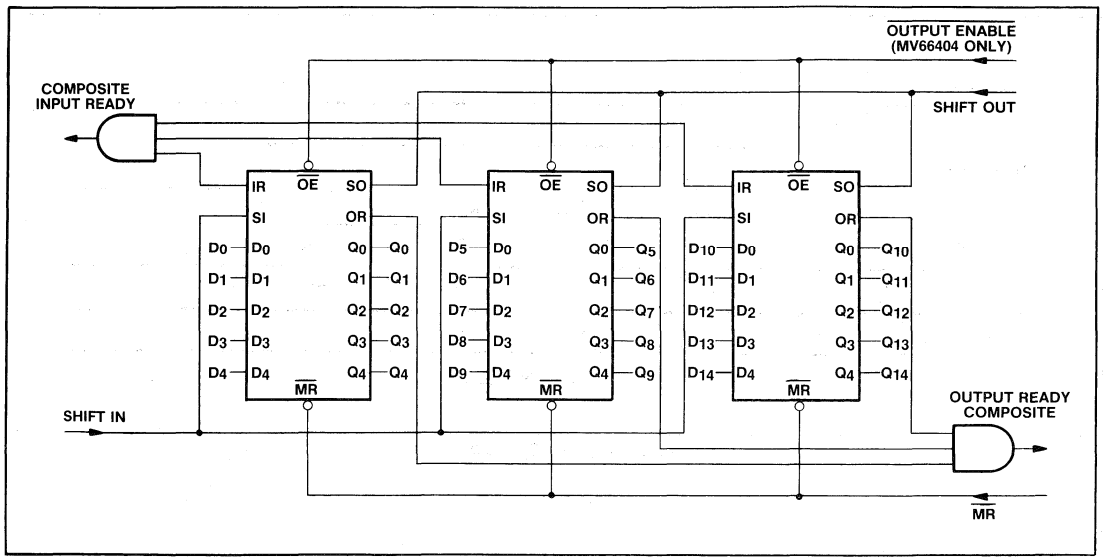



*Fig.10 64 x 15 application (MV66402/MV66404)*

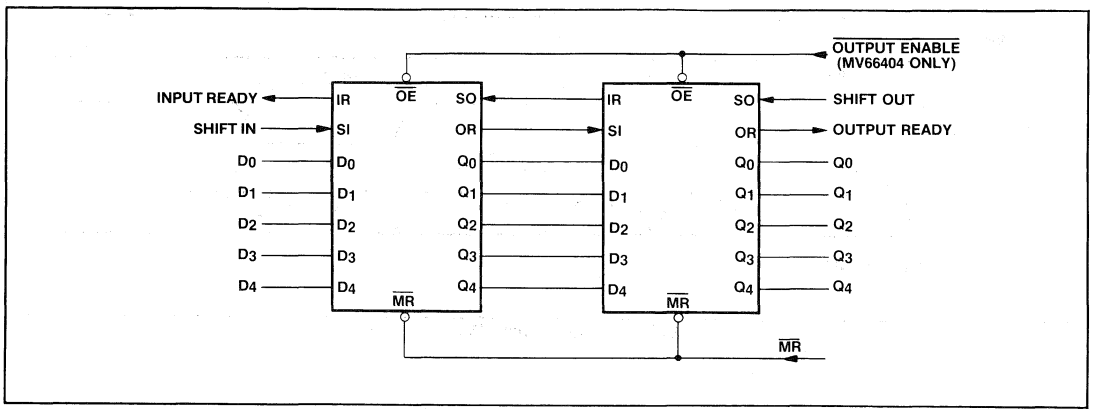



*Fig.11 128 by 5 application (MV66402/MV66404)*

## USER NOTES

1. When the memory is *empty the last word read will remain on the outputs* until the master reset is strobed or a new data word falls through to the output. However, OR will remain LOW, indicating data at the output is not valid.
2. When the output changes as a result of a pulse on SO, the OR signal always goes LOW before there is any change in output data.
3. If SO is held HIGH while the memory is empty and a word is written into the input, that word will ripple through the memory to the output. OR will go HIGH for one internal cycle ($t_{POR}$) and then go back LOW again. The stored word will remain on the outputs. If more words are written into the FIFO, they will line up behind the first word and will not appear on the outputs until SO has been brought LOW.
4. When the master reset is brought LOW, the outputs are cleared to LOW, IR goes HIGH and OR goes LOW. If SI is HIGH when the master reset goes HIGH then the data on the inputs will be written into the memory and IR will return to the LOW state until SI is brought LOW. If SI is LOW when the master reset is ended, the IR will go HIGH, but the data on the inputs will not enter the memory until SI goes HIGH.
5. All MV66XXX FIFO's will cascade with other MV66XXX devices, but may not cascade with pin compatible devices from other manufacturers.
6. The IR and OR signals are provided to ensure that data is written into, or read out of, the FIFO correctly. If SI or SO are clocked without reference to these flags, the memory may corrupt and lock out any further data inputs. The memory should be reset to restore normal operation.

## TYPICAL CHARACTERISTICS

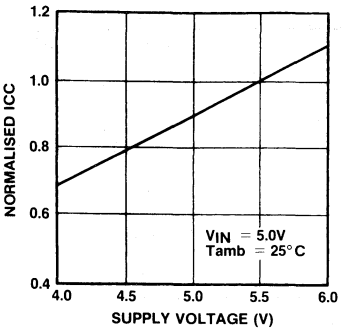



*Fig.12 Normalised supply current vs. supply voltage*

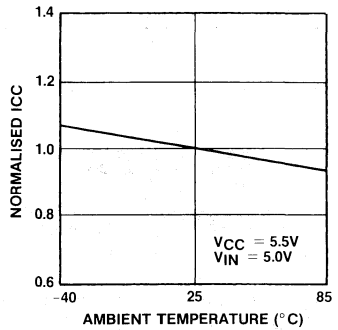



*Fig.13 Normalised supply current vs. ambient temperature*

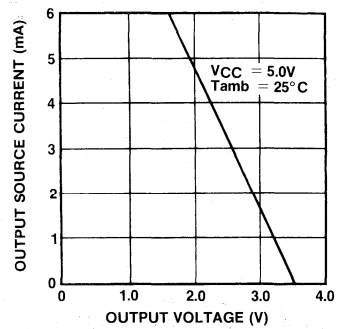



*Fig.14 Output source current vs. output voltage*

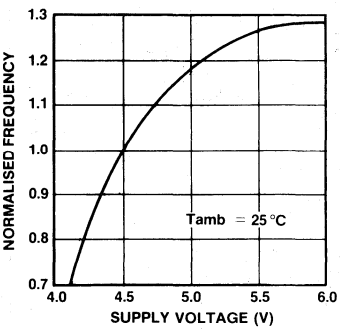



*Fig.15 Normalised frequency vs. supply voltage*

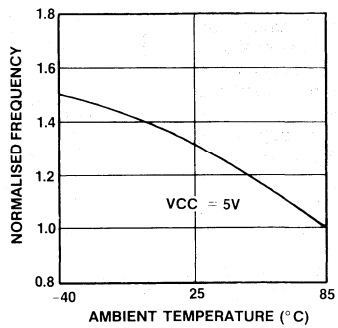



*Fig.16 Normalised frequency vs. ambient temperature*

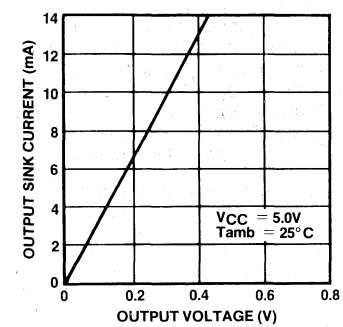



*Fig.17 Output sink current vs. output voltage*

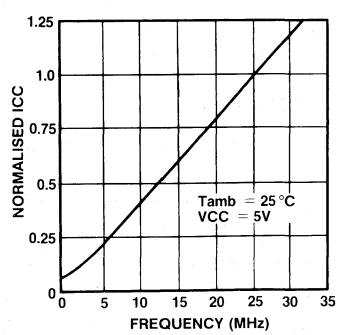



*Fig.18 Normalised $I_{CC}$ vs. frequency*

## ORDERING INFORMATION

**MV66401-10 B0 DP** (Industrial - Plastic DIL package)
**MV66401-25 B0 DP** (Industrial - Plastic DIL package)
**MV66402-10 B0 DP** (Industrial - Plastic DIL package)
**MV66402-25 B0 DP** (Industrial - Plastic DIL package)
**MV66403-10 B0 DP** (Industrial - Plastic DIL package)
**MV66403-25 B0 DP** (Industrial - Plastic DIL package)
**MV66404-10 B0 DP** (Industrial - Plastic DIL package)
**MV66404-25 B0 DP** (Industrial - Plastic DIL package)

**MV66401-10 B0 DG** (Industrial - Ceramic DIL package)
**MV66401-25 B0 DG** (Industrial - Ceramic DIL package)
**MV66402-10 B0 DG** (Industrial - Ceramic DIL package)
**MV66402-25 B0 DG** (Industrial - Ceramic DIL package)
**MV66403-10 B0 DG** (Industrial - Ceramic DIL package)
**MV66403-25 B0 DG** (Industrial - Ceramic DIL package)
**MV66404-10 B0 DG** (Industrial - Ceramic DIL package)
**MV66404-25 B0 DG** (Industrial - Ceramic DIL package)

# SP1648
## ECL OSCILLATOR

The SP1648 is an emitter-coupled oscillator, constructed on a single monolithic silicon chip. Output levels are compatible with ECL III logic levels. The oscillator requires an external parallel tank circuit consisting of an inductor (L) and capacitor (C).

A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The device may also be used in phase locked loops and many other applications requiring a fixed or variable frequency clock source of high spectral purity.

The SP1648 may be operated from a +5.0V dc supply or a -5.2V dc supply, depending upon system requirements.

**Operating temperature range:**
-30° C to +85° C (Ceramic)
0° C to +75° C (Plastic)

| SUPPLY VOLTAGE | GND PINS | SUPPLY PINS |
|---|---|---|
| +5.0V dc | 7,8 | 1,14 |
| -5.2V dc | 1,14 | 7,8 |

### ORDERING INFORMATION
**SP1648DP** (Industrial - Plastic DIL package)
**SP1648DG** (Industrial - Ceramic DIL package)
**SP1648BB DG** (Plessey High Reliability Ceramic DIL package)
**SP1648 LC** (Industrial - LCC package)
**SP1648 MP** (Industrial - Miniature Plastic package)

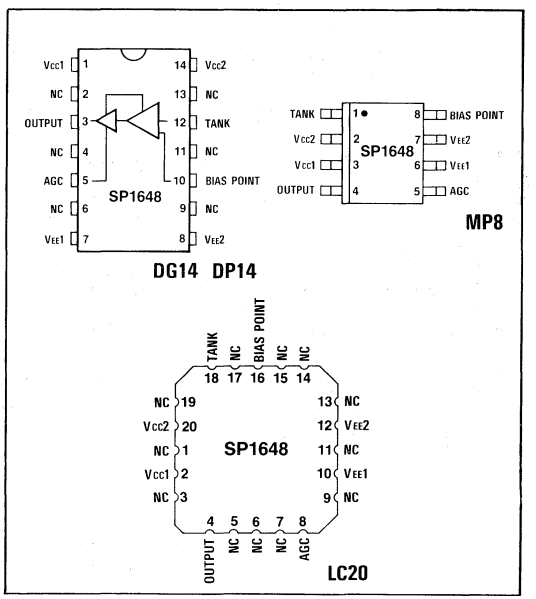



*Fig.1 Block diagram and pin connections (top view)*

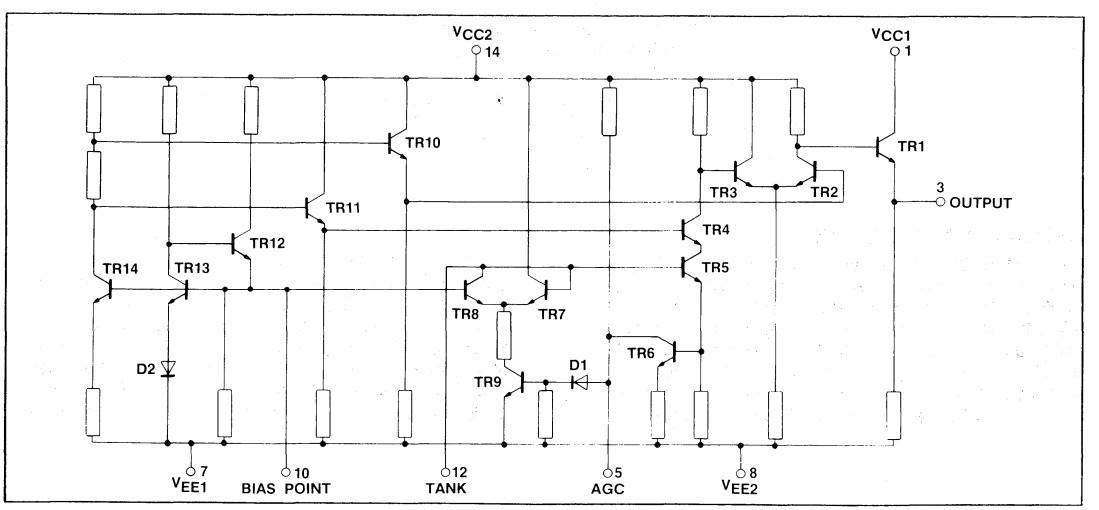



*Fig.2 Circuit diagram of SP1648*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $V_{CC}$ - $V_{EE}$ 8V |
| Output source current | <40mA |
| AGC input | $V_{CC}$ to $V_{EE}$ |
| Storage temperature range | -65°C to +150°C (Ceramic) |
| | -55°C to +150°C (Plastic) |
| Operating junction temperature DG | <175°C |
| Operating junction temperature DP | <150°C |

## ELECTRICAL CHARACTERISTICS

**Supply Voltage = +5.0V**

| Characteristic | Symbol | Pin under test | SP1648 Test Limits | | | | | | | | Unit | TEST VOLTAGE/CURRENT | | | | | | $V_{EE}$ (Gnd) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -30° C | | +25° C | | +85° C | | | | | Volts | | | mAdc | | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | | | Test temp. | $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{CC}$ | $I_L$ | | |
| | | | | | | | | | | | | -30° C | +1.960 | +1.410 | 5.0 | 5.0 | | |
| | | | | | | | | | | | | +25° C | +1.800 | +1.300 | 5.0 | 5.0 | | |
| | | | | | | | | | | | | +85° C | +1.680 | +1.180 | 5.0 | 5.0 | | |
| Power supply drain current | $I_E$ | 8 | - | - | - | 40 | - | - | | | mAdc | TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW | | | | | | |
| Logic '1' output voltage | $V_{OH}$ | 3 | 3.94 | 4.18 | 4.04 | 4.25 | 4.11 | 4.36 | | | Vdc | | - | - | 1.14 | - | | 7,8 |
| Logic '0' output voltage | $V_{OL}$ | 3 | 3.16 | 3.40 | 3.20 | 3.43 | 3.23 | 3.46 | | | Vdc | | 12 | 12 | 1.14 | 3 | | 7,8 |
| Bias voltage | $V_{bias}$* | 10 | 1.51 | 1.86 | 1.40 | 1.70 | 1.28 | 1.58 | | | Vdc | | - | - | 1.14 | - | | 7,8 |
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | | | | | | |
| Peak-to-peak tank voltage | $V_{P-P}$ | 12 | - | - | - | - | 500 | - | - | - | - | mV | See Fig.4 | - | 1.14 | 3 | | 7,8 |
| Output duty cycle | $V_{DC}$ | 3 | - | - | - | - | 50 | - | - | - | - | % | See Fig.4 | - | 1.14 | 3 | | 7,8 |
| Oscillation frequency | $f_{max}$ | - | - | - | - | 200 | 225 | - | - | - | - | MHz | See Fig.4 | - | 1.14 | 3 | | 7,8 |

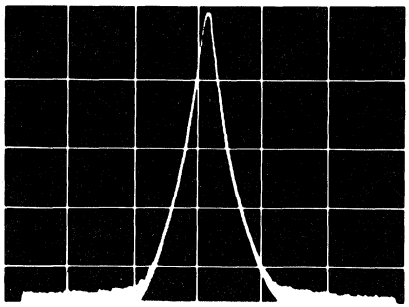
Thermal characteristics

DG14 $\theta_{JA} = 125°$ C/W
$\theta_{JC} = 40°$ C/W

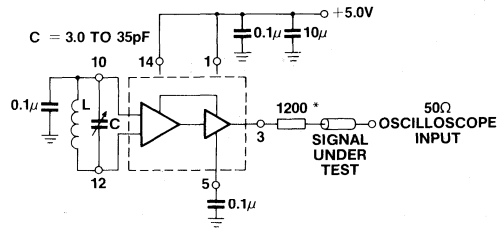
DP14 $\theta_{JA} = 107°$ C/W
$\theta_{JC} = 52°$ C/W

**Supply Voltage = -5.2V**

| Characteristic | Symbol | Pin under test | SP1648 Test Limits | | | | | | | | Unit | TEST VOLTAGE/CURRENT | | | | | | $V_{EE}$ (Gnd) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -30° C | | +25° C | | +85° C | | | | | Volts | | | mAdc | | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | | | | Test temp. | $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{CC}$ | $I_L$ | | |
| | | | | | | | | | | | | -30° C | -3.240 | -3.790 | 5.2 | 5.0 | | |
| | | | | | | | | | | | | +25° C | -3.400 | -3.900 | 5.2 | 5.0 | | |
| | | | | | | | | | | | | +85° C | -3.520 | -4.020 | 5.2 | 5.0 | | |
| Power supply drain current | $I_E$ | 8 | - | - | - | 41 | - | - | | | mAdc | TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW | | | | | | |
| Logic '1' output voltage | $V_{OH}$ | 3 | 1.045 | -0.815 | -0.960 | -0.750 | -0.890 | -0.650 | | | Vdc | | - | - | 7.8 | - | | 1,14 |
| Logic '0' output voltage | $V_{OL}$ | 3 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | | | Vdc | | 12 | 12 | 7.8 | 3 | | 1,14 |
| Bias voltage | $V_{bias}$* | 10 | -3.690 | -3.340 | -3.800 | -3.500 | -3.920 | -3.620 | | | Vdc | | - | - | 7.8 | - | | 1,14 |
| | | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | | | | | | |
| Peak-to-peak tank voltage | $V_{P-P}$ | 12 | - | - | - | - | 500 | - | - | - | - | mV | See Fig.4 | - | 7.8 | 3 | | 1,14 |
| Output duty cycle | $V_{DC}$ | 3 | - | - | - | - | 50 | - | - | - | - | % | See Fig.4 | - | 7.8 | 3 | | 1,14 |
| Oscillation frequency | $f_{max}$ | - | - | - | - | 200 | 225 | - | - | - | - | MHz | See Fig.4 | - | 7.8 | 3 | | 1,14 |

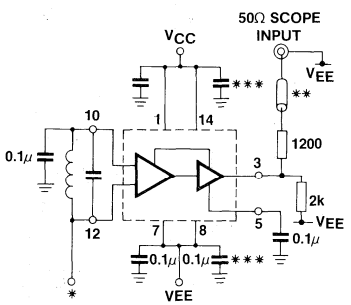


B.W. = 10kHz
Center Frequency = 100MHz
Scan Width = 50kHz/div
Vertical Scale = 10dB/div




*The 1200Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe.

*Fig.3 Spectral purity of signal at output (DIL pin numbers)*




*Use high impedance probe (>1.0MΩ must be used).

**The 1200Ω resistor and the scope termination impedance constitute a 25:1 attenuator probe.

***Bypass only that supply opposite ground.

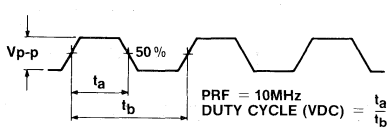



*Fig.4 Test circuit and waveforms (DIL pin numbers)*

## OPERATING CHARACTERISTICS

Fig.1 illustrates the circuit schematic for the SP1648. The oscillator incorporates positive feedback by coupling the base of transistor TR7 to the collector of TR8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (TR7 and TR8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, a cascode transistor (TR4) is used to translate from the emitter follower (TR5) to the output differential pair TR2 and TR3. TR2 and TR3, in conjunction with output transistor TR1, provide a highly buffered output which produces a square wave. Transistors TR10 through TR14 provide this bias drive for the oscillator and output buffer. Fig.3 indicates the high spectral purity of the oscillator output.

When operating the oscillator in the voltage controlled mode (Fig.5), it should be noted that the cathode of the varactor diode (D) should be biased at least 2 $V_{BE}$ above $V_{EE}$ (≈1.4V for positive supply operation).

When the SP1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Fig.6.

Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figs.7,8 and 9. Figs.7 and 9 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6pF typical). Fig.8 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1kΩ resistor in Figs.7 and 8 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51kΩ) in Fig.9 is required to

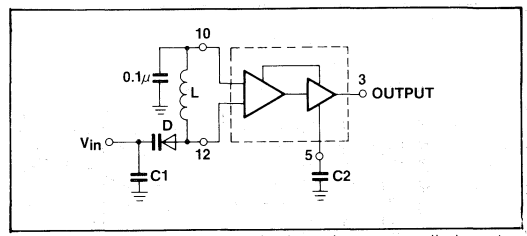



*Fig.5 The SP1648 operating in the voltage-controlled mode (DIL pin numbers)*

provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D\,(max) + C_S}}{\sqrt{C_D\,(min) + C_S}}$$

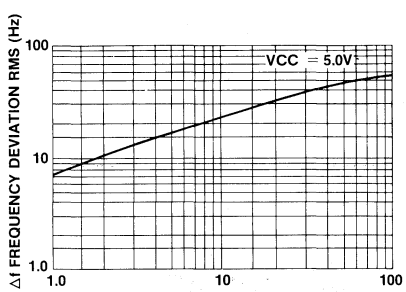
$$\text{where } f_{min} = \frac{1}{2\pi\sqrt{L\,(C_D\,(max) + C_S)}}$$

$C_S$ = shunt capacitance (input plus external capacitance).
$C_D$ = varactor capacitance as a function of bias voltage.

Good RF and low-frequency by-passing is necessary on the power supply pins (see Fig.3).

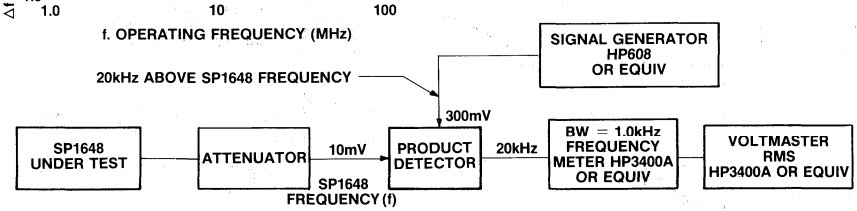
Capacitors (C1 and C2 of Fig.5) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1MHz and 50MHz a 0.1μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At higher frequencies the value of bypass capacitors depends directly




**OSCILLATOR TANK COMPONENTS (CIRCUIT OF FIGURE 5)**

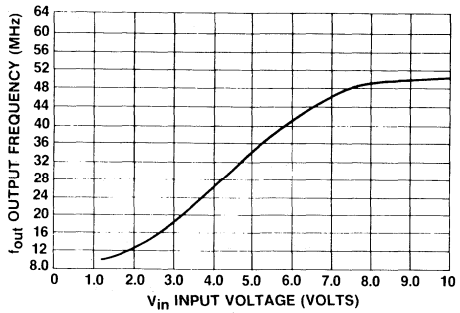
| f MHz | D | L μH |
|---|---|---|
| 1.0-10 | MV2115 | 100 |
| 10-60 | MV2115 | 2.3 |
| 60-100 | MV2106 | 0.15 |




$$\text{FREQUENCY DEVIATION} = \frac{\text{(HP5210A OUTPUT VOLTAGE) (FULL SCALE FREQUENCY)}}{\text{1.0VOLT}}$$

Note: Any frequency deviation caused by the signal generator and SP1648 power supply should be determined and minimised prior to testing.

*Fig.6 Frequency deviation test circuit*



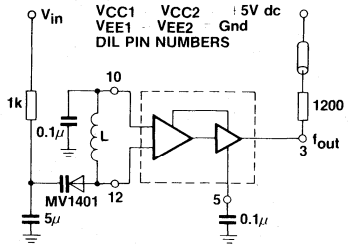
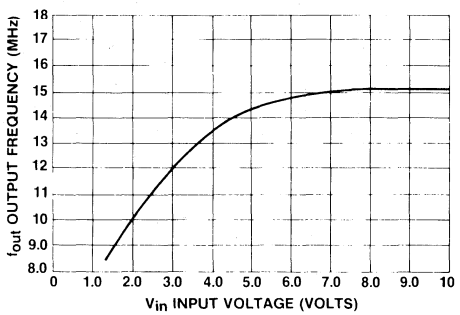




Fig.7



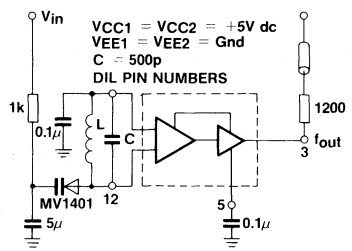
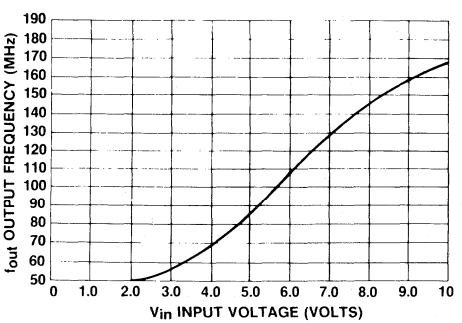




Fig.8



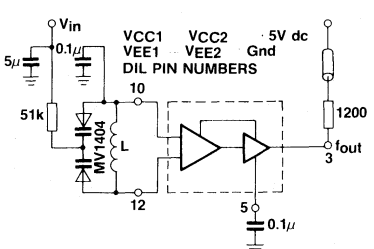




Fig.9

upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimise unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the SP1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0V supply is used, -5.2V if a negative supply is used).

At frequencies above 100MHz typ. it may be necessary to increase the tank circuit peak-to-peak voltage in order to maintain a square wave at the output of the SP1648. This is accomplished by attaching a series resistor (1kΩ minimum) from the AGC to the most positive power potential ( +5.0V if a +5.0V supply is used, ground if a -5.2V supply is used).

# SP1658

## VOLTAGE-CONTROLLED MULTIVIBRATOR

The SP1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with ECL III and ECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.

The SP1658 is useful in frequency modulation, phase-locked loops, frequency synthesiser and clock signal generation applications for instrumentation, communication and computer systems.

### FEATURES

- Operating Temperature Range:
  -30°C to +85°C (Ceramic)
  0°C to +75°C (Plastic)
- Supply Voltages -5.2V, 0V
- Oscillator Frequency Max. 190MHz
- Voltage Controlled

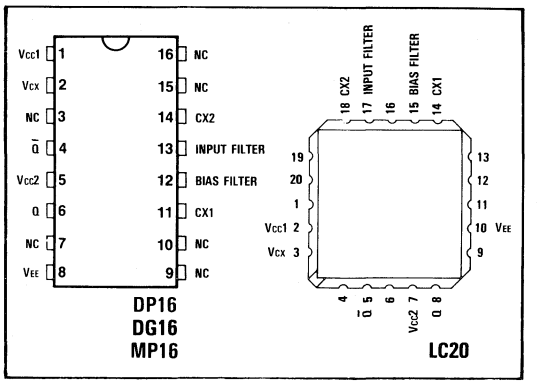



*Fig.1 Pin connections(top view)and block diagram*

### ORDERING INFORMATION

**SP1658DP** (Industrial - Plastic DIL package)
**SP1658DG** (Industrial - Ceramic DIL package)
**SP1658LC** (Industrial - LCC package)
**SP1658MP** (Industrial - Miniature plastic package)

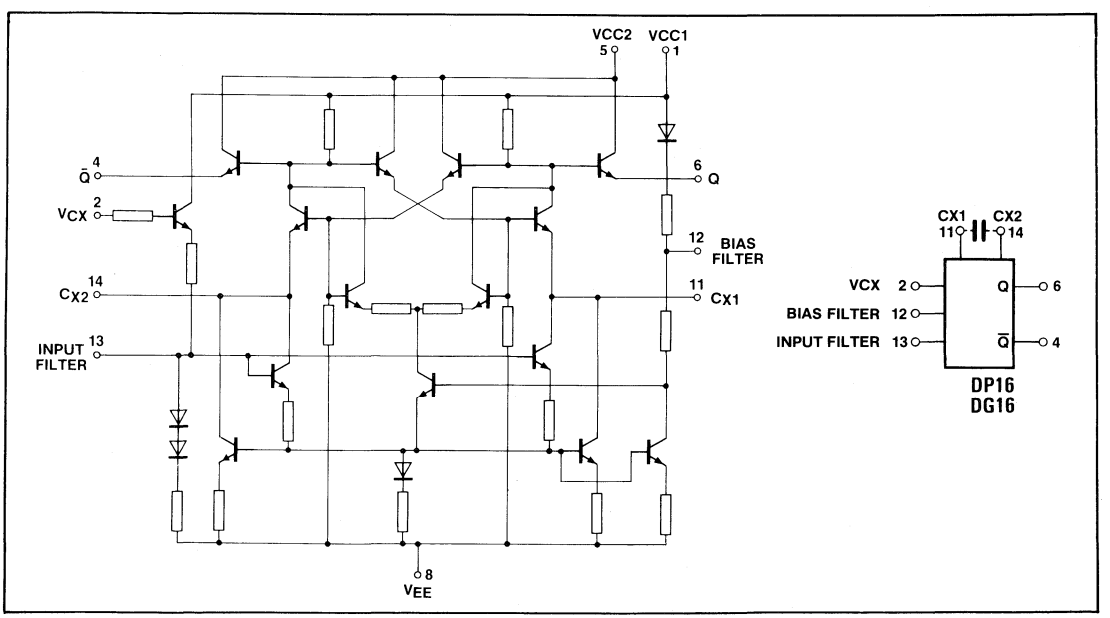



*Fig.2 Circuit diagram (DG, DP and MP pin numbers)*

## ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50Ω resistor to -2.0V.

| Test temp. | TEST VOLTAGE (V) $V_{CX1}$ | $V_{CX2}$ | $V_{CX3}$ | $V_{EE}$ |
|---|---|---|---|---|
| -30°C | 0.0 | -2.0 | -1.0 | -5.2 |
| +25°C | -0.0 | -2.0 | -1.0 | -5.2 |
| +85°C | -0.0 | -2.0 | -1.0 | -5.2 |

| Characteristic | Symbol | Pin under test | SP1658 Test Limits -30°C Min. | -30°C Max. | +25°C Min. | +25°C Typ. | +25°C Max. | +85°C Min. | +85°C Max. | Unit | TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{CX1}$ | $V_{CX2}$ | $V_{CX3}$ | $V_{EE}$ | $V_{CC}$ (GND) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | | | | | | | | | |
| Drain current | $I_E$ | 8* | - | - | - | - | 32 | - | - | mAdc | 2 | - | - | 8 | 1,5 |
| | | 8** | - | - | - | - | 32 | - | - | mAdc | 2 | - | - | 8 | 1,5 |
| Input current | $I_{INH}$ | 2* | - | - | - | - | 350 | - | - | μAdc | 2 | - | - | 8 | 1,5 |
| Input leakage current | $I_{INL}$ | 2* | - | - | -0.5 | - | - | - | - | μAdc | - | 2 | - | 8 | 1,5 |
| High output voltage $\overline{Q}$ | $V_{OH}$ | 4* | -1.045 | -0.875 | -0.960 | - | -0.810 | -0.890 | -0.700 | Vdc | - | - | 2 | 8 | 1,5 |
| Q | | 6** | -1.045 | -0.875 | -0.960 | - | -0.810 | -0.890 | -0.700 | Vdc | - | - | 2 | 8 | 1,5 |
| Low output voltage $\overline{Q}$ | $V_{OL}$ | 4** | -1.890 | -1.650 | -1.850 | - | -1.620 | -1.830 | -1.575 | Vdc | - | - | 2 | 8 | 1,5 |
| Q | | 6* | -1.890 | -1.650 | -1.850 | - | -1.620 | -1.830 | -1.575 | Vdc | - | - | 2 | 8 | 1,5 |
| AC characteristics (Fig.3) | | | | | | | | | | | $C_{X1}$ | $C_{X2}$ | $V_{CX}$ +2.0V | $V_{EE}$ -3.2V | $V_{CC}$ +2.0V |
| Tests shown for one output, but checked on both | | | | | | | | | | | | | | | |
| Rise time (10 % to 90 %) | $t_+$ | 6 | - | 3.6 | - | - | 3.5 | - | 3.8 | ns | - | 11,14 | 2 | 8 | 1,5 |
| Fall time (10 % to 90 %) | $t_-$ | 6 | - | 3.1 | - | - | 3.0 | - | 3.3 | ns | - | 11,14 | 2 | 8 | 1,5 |
| Oscillator frequency | $f_{osc1}$ | - | 130 | - | 130 | 155 | 190 | 110 | - | MHz | - | 11,14 | 2 | 8 | 1,5 |
| | $f_{osc2}$ | - | - | - | 78 | 90 | 120 | - | - | MHz | 11,14 | - | 2 | 8 | 1,5 |
| Tuning ratio test † | TR | - | - | - | 3.1 | 4.5 | - | - | - | - | 11,14 | - | - | 8 | 1,5 |

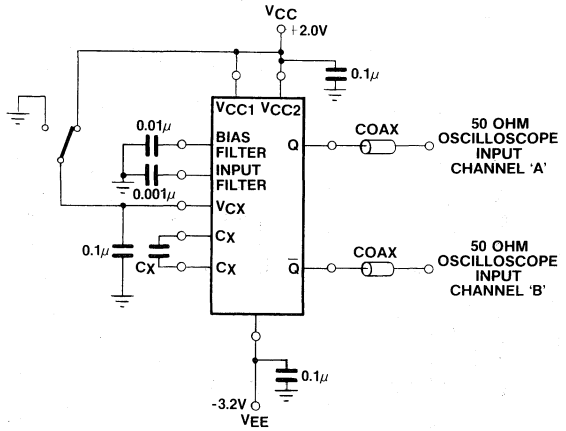
* Germanium diode (0.4 drop) forward biased from 11 to 14 (11 ——▶|—— 14)

** Germanium diode (0.4 drop) forward biased from 14 to 11 (11 ——|◀—— 14)

† $TR = \frac{\text{Output frequency at } V_{CX} = +2.0V}{\text{Output frequency at } V_{CX} = \text{Gnd}}$

CX1 = 10pF connected from pin 11 to pin 14

CX2 = 5pF connected from pin 11 to pin 14




The +2 and -3.2V supplies enable the output load to be connected to ground.

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be <1 inch from $TP_{in}$ to input pin and $TP_{out}$ to output pin.

Chip capacitors are advised for the input bias filters and supply decoupling.

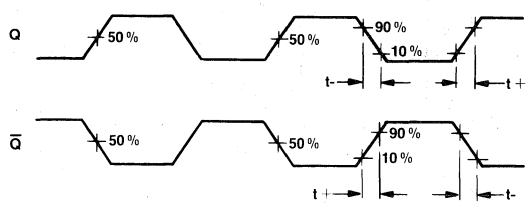



*Fig.3 Switching time test circuit and waveforms*

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply | \| $V_{CC}$ - $V_{CC}$\| 8V |
| Output source current | <40mA |
| $V_{CX}$ input | -2.5 to $V_{CC}$ |
| Storage temperature range | -65°C to +150°C (Ceramic and LC) |
| | -55°C to +150°C (Plastic) |
| Operating junction temperature DG | <175°C |
| Operating junction temperature DP | <150°C |

Thermal characteristics

| | |
|---|---|
| DG16 | $\theta_{JA}$ = 120°C/W |
| | $\theta_{JC}$ = 40°C/W |
| LC20 | $\theta_{JA}$ = 73°C/W |
| | $\theta_{JC}$ = 22°C/W |
| DP16 | $\theta_{JA}$ = 180°C/W |
| | $\theta_{JC}$ = 47°C/W |

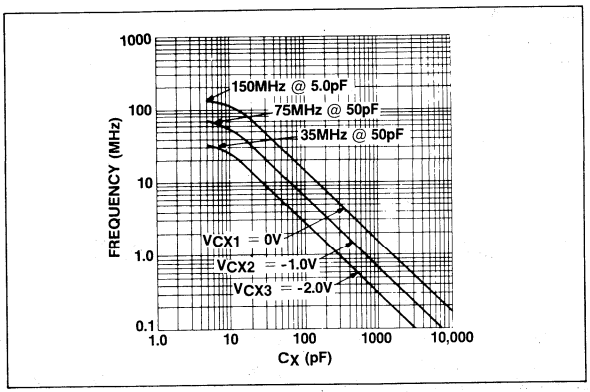



*Fig.4 Output frequency v. capacitance for three values of input voltage*

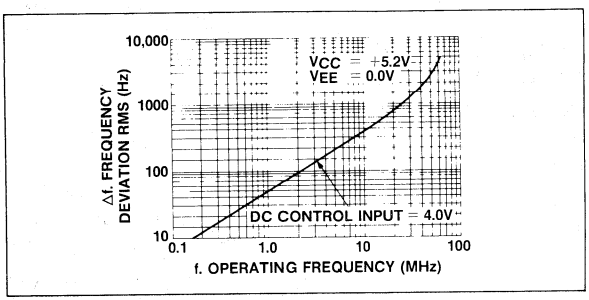



*Fig.5 RMS noise deviation v. operating frequency*

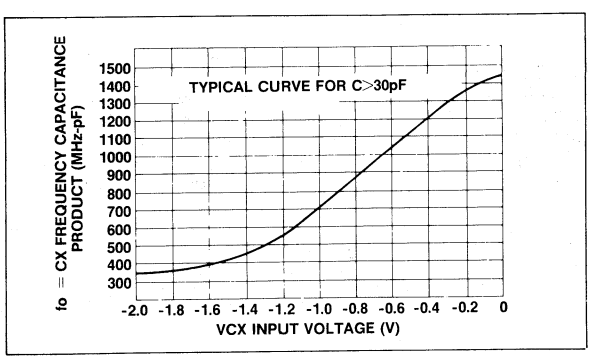



*Fig.6 Frequency-capacitance product v. control voltage $V_{CX}$*

1557-1.0

# SP16F60

## DUAL 4-INPUT OR/NOR GATE

SP16F60 provides simultaneous OR-NOR output functions with the capability of driving 50Ω lines. This device contains an internal bias reference voltage, ensuring that the threshold point is always in the centre of the transition region over the temperature range (—30°C to +85°C). Input pulldown resistors eliminate the need to tie unused inputs to $V_{EE}$.

### FEATURES

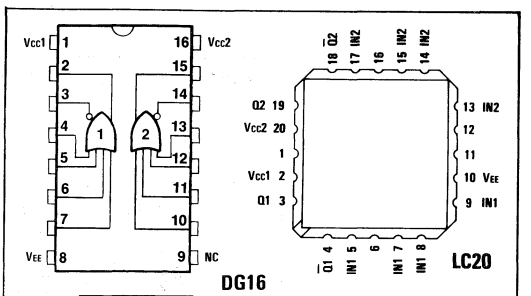
- Operating Temperature Range -30°C to +85°C
- Gate Switching Speed 550ps Typ.
- ECL III and ECL 10K Compatible
- 50Ω Line Driving Capability
- Operation With Unused I/Ps Open Circuit
- Low Supply Noise Generation
- Pin and Power Compatible With SP1660

### APPLICATIONS

- Data Communications
- Instrumentation
- PCM Transmission Systems
- Nucleonics

### ORDERING INFORMATION

**SP16F60DG** (Industrial - Ceramic DIL package)
**SP16F60BB DG** (GPS High Reliability, Level B, Ceramic DIL package)
**SP16F60LC** (Industrial - LCC package)
**SP16F60BA DG** (GPS High Reliability, Level A, Ceramic DIL package)




3 = 4 + 5 + 6 + 7
2 = 4 + 5 + 6 + 7

DC Input Loading Factor = 1
DC Output Loading Factor = 70
$t_{pd}$ = 0.9ns typ (510-ohm load)
= 1.1ns typ (50-ohm load)
$P_D$ = 120mW typ/pkg (No load)
Full Load Current, $I_L$ = -25mA dc max.

*Fig.1(a) Logic and pin connections (top view) DG package*
*Fig.1(b) Pin connections LC package*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $\|V_{CC} - V_{EE}\|$ 8V |
| Input voltages | 0V to $V_{EE}$ |
| Output source current | <40mA |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |

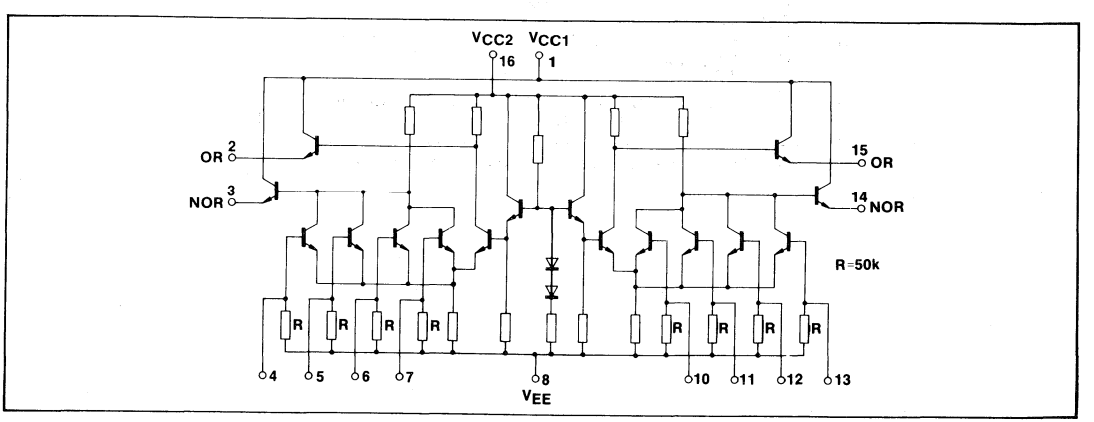



*Fig.2 Circuit diagram*

## ELECTRICAL CHARACTERISTICS

This ECL III circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The package should be housed in a suitable heat sink or a transverse air flow greater than 500 linear fpm should be maintained while the circuit is either in a test socket or mounted on a printed circuit board. Test procedures are shown for selected inputs and selected outputs. The other inputs and outputs are tested in a similar manner. Outputs are tested with a 50Ω resistor to -2.0V dc.

Thermal characterstics

DG16
$\theta_{JA}$ = 120°C/W
$\theta_{JC}$ = 40°C/W

LC20
$\theta_{JA}$ = 73°C/W
$\theta_{JC}$ = 22°C/W

| @ Test Temperature | TEST VOLTAGE VALUES (V) $V_{IH\ max}$ | $V_{IL\ min}$ | $V_{IHA\ min}$ | $V_{ILA\ max}$ | $V_{EE}$ |
|---|---|---|---|---|---|
| -30°C | -0.875 | -1.890 | -1.180 | -1.515 | -5.2 |
| +25°C | -0.810 | -1.850 | -1.095 | -1.485 | -5.2 |
| +85°C | -0.700 | -1.830 | -1.025 | -1.440 | -5.2 |

| Characteristic | Symbol | Pin Under Test | SP16F60 Test Limits -30°C Min | -30°C Max | +25°C Min | +25°C Max | +85°C Min | +85°C Max | Units | TEST VOLTAGE APPLIED TO PINS LISTED BELOW: $V_{IH\ max}$ | $V_{IL\ min}$ | $V_{IHA\ min}$ | $V_{ILA\ max}$ | $V_{EE}$ | $V_{CC}$ (Gnd) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power Supply Drain Current | $I_E$ | 8 | – | – | – | 28 | – | – | mA | – | – | – | – | 8 | 1,16 |
| Input Current | $I_{in\ H}$ | * | – | – | – | 350 | – | – | μA | * | – | – | – | 8 | 1,16 |
| | $I_{in\ L}$ | * | – | – | 0.5 | – | – | – | μA | – | * | – | – | 8 | 1,16 |
| NOR Logic 1 Output Voltage | $V_{OH}$ | 3 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | V | – | 4 | – | – | 8 | 1,16 |
| | | | | | | | | | | – | 5 | – | – | | |
| | | | | | | | | | | – | 6 | – | – | | |
| | | | | | | | | | | – | 7 | – | – | | |
| NOR Logic 0 Output Voltage | $V_{OL}$ | 3 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | V | 4 | – | – | – | 8 | 1,16 |
| | | | | | | | | | | 5 | – | – | – | | |
| | | | | | | | | | | 6 | – | – | – | | |
| | | | | | | | | | | 7 | – | – | – | | |
| OR Logic 1 Output Voltage | $V_{OH}$ | 2 | -1.045 | -0.875 | -0.960 | -0.810 | -0.890 | -0.700 | V | 4 | – | – | – | 8 | 1,16 |
| | | | | | | | | | | 5 | – | – | – | | |
| | | | | | | | | | | 6 | – | – | – | | |
| | | | | | | | | | | 7 | – | – | – | | |
| OR Logic 0 Output Voltage | $V_{OL}$ | 2 | -1.890 | -1.650 | -1.850 | -1.620 | -1.830 | -1.575 | V | – | 4 | – | – | 8 | 1,16 |
| | | | | | | | | | | – | 5 | – | – | | |
| | | | | | | | | | | – | 6 | – | – | | |
| | | | | | | | | | | – | 7 | – | – | | |
| NOR Logic 1 Threshold Voltage | $V_{OHA}$ | 3 | -1.065 | – | -0.980 | – | -0.910 | – | V | – | – | – | 4 | 8 | 1,16 |
| | | | | – | | – | | – | | – | – | – | 5 | | |
| | | | | – | | – | | – | | – | – | – | 6 | | |
| | | | | – | | – | | – | | – | – | – | 7 | | |
| NOR Logic 0 Threshold Voltage | $V_{OLA}$ | 3 | – | -1.630 | – | -1.600 | – | -1.555 | V | – | – | 4 | – | 8 | 1,16 |
| | | | – | | – | | – | | | – | – | 5 | – | | |
| | | | – | | – | | – | | | – | – | 6 | – | | |
| | | | – | | – | | – | | | – | – | 7 | – | | |
| OR Logic 1 Threshold Voltage | $V_{OHA}$ | 2 | -1.065 | – | -0.980 | – | -0.910 | – | V | – | – | 4 | – | 8 | 1,16 |
| | | | | – | | – | | – | | – | – | 5 | – | | |
| | | | | – | | – | | – | | – | – | 6 | – | | |
| | | | | – | | – | | – | | – | – | 7 | – | | |
| OR Logic 0 Threshold Voltage | $V_{OLA}$ | 2 | – | -1.630 | – | -1.600 | – | -1.555 | V | – | – | – | 4 | 8 | 1,16 |
| | | | – | | – | | – | | | – | – | – | 5 | | |
| | | | – | | – | | – | | | – | – | – | 6 | | |
| | | | – | | – | | – | | | – | – | – | 7 | | |
| Switching Times (50Ω Load) | | | Typ | Max | Typ | Max | Typ | Max | | Pulse In | Pulse Out | | | -3.2V | +2.0V |
| Propagation Delay | $t_{4+3-}$ | 3 | – | – | 0.55 | 0.8 | – | – | ns | 4 | 3 | – | – | 8 | 1,16 |
| | $t_{4-2-}$ | 2 | – | – | | | – | – | | | 2 | – | – | | |
| | $t_{4+2+}$ | 2 | – | – | | | – | – | | | 2 | – | – | | |
| | $t_{4-3+}$ | 3 | – | – | | | – | – | | | 3 | – | – | | |
| Rise Time 20% to 80% | $t_{3+}$ | 3 | | | 0.4 | 0.6 | – | – | ns | 4 | 3 | – | – | 8 | 1,16 |
| | $t_{2+}$ | 2 | | | 0.35 | 0.6 | – | – | ns | 4 | 2 | – | – | 8 | 1,16 |
| Fall Time 20% to 80% | $t_{3-}$ | 3 | | | 0.4 | 0.6 | – | – | ns | 4 | 3 | – | – | 8 | 1,16 |
| | $t_{2-}$ | 2 | | | 0.35 | 0.6 | – | – | ns | 4 | 2 | – | – | 8 | 1,16 |

* Individually test each input applying $V_{IH}$ or $V_{IL}$ to the input under test.

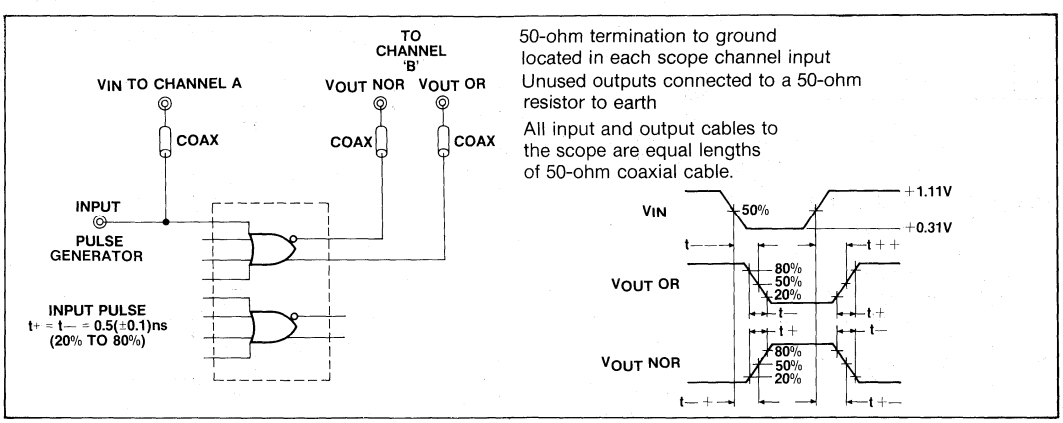



*Fig.3 Switching time test circuit and waveforms at +25° C*

# SP9131

## 520MHz ECL DUAL D FLIP-FLOP

The SP9131 Dual D type flip-flop is pin compatible with 10131, but has improved dynamic performance.

### FEATURES

- Guaranteed Operation at 520MHz
- Separate or Common Clock
- Independent Set and Reset Inputs
- Master Slave Operation
- -5.2V Supply
- Operating Temperature Range:
  -30°C to +85°C - Industrial
  -55°C to +125°C - Military
- ECL 10K Compatible
- Pin Compatible with MC10131/102131/105131/10H131 — But Faster

### ORDERING INFORMATION

**SP9131DG** (Industrial - Ceramic DIL package)
**SP9131BB DG** (Plessey High Reliability Ceramic DIL package)
**SP9131LC** (Industrial - LCC package)
**SP9131AC DG** (Military - Ceramic DIL package)

NOTE:
The AC version of this product conforms to MIL-STD-883C CLASS B screening and is covered by separate data which observes the change notification requirements of MIL-M-38510

### R-S TRUTH TABLE

| R | S | Qn + 1 |
|---|---|---|
| L | L | Qn |
| L | H | H |
| H | L | L |
| H | H | ND |

### CLOCKED TRUTH TABLE

| C | D | Qn + 1 |
|---|---|---|
| L | X | Qn |
| H | L | L |
| H | H | H |

X = Don't care
C = CE + CC
A clock H is a clock transition from a low to a high state.

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power supply voltage | $\lvert V_{CC} - V_{EE} \rvert$ 8V |
| Input voltages | 0V to $V_{EE}$ |
| Output source current | <40mA |
| Storage temperature range | -65°C to +150°C |
| Junction operating temperature | <175°C |

### THERMAL CHARACTERISTICS

| | |
|---|---|
| DG16 | $\theta_{JA}$ = 110°C/W |
| | $\theta_{JC}$ = 33°C/W |
| LC20 | $\theta_{JA}$ = 73°C/W |
| | $\theta_{JC}$ = 22°C/W |

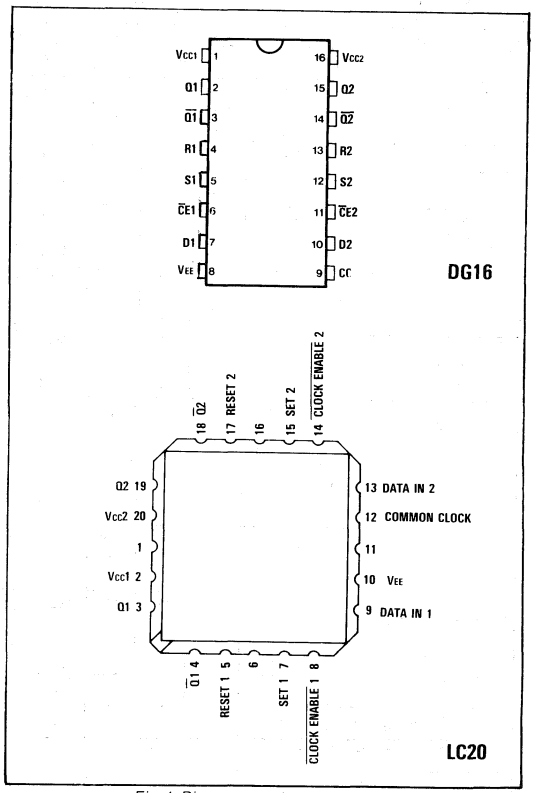



*Fig.1 Pin connections - top view*

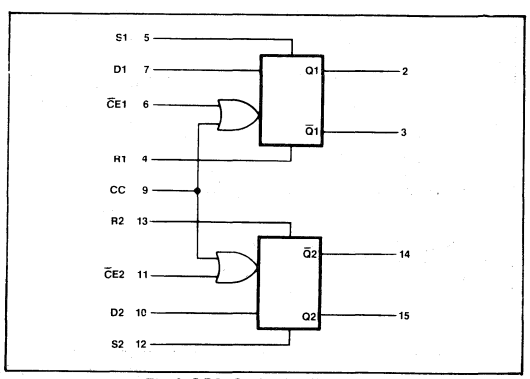
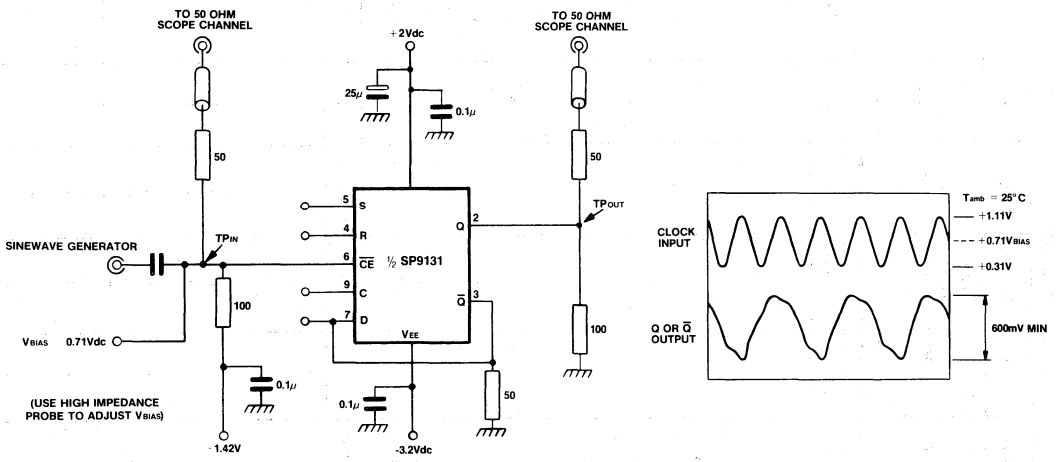



*Fig.2 SP9131 logic diagram*

## TEST CIRCUIT DETAILS

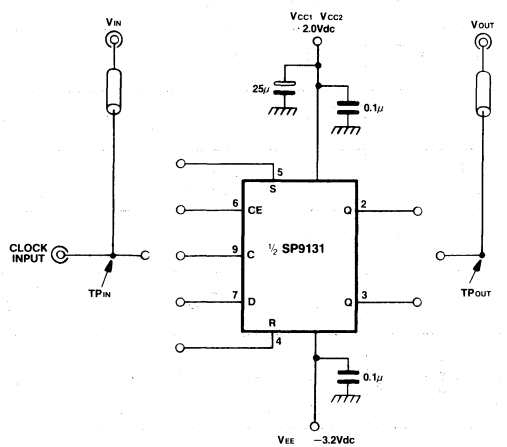


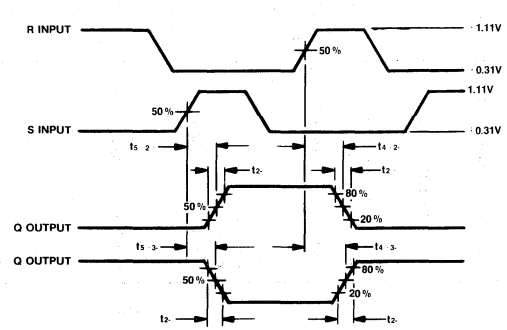

50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from $TP_{IN}$ to input pin and $TP_{OUT}$ to output pin.

The +2V and -3.2V supplies allow the output load to be connected to ground.

*Fig.3 Toggle frequency test circuit*

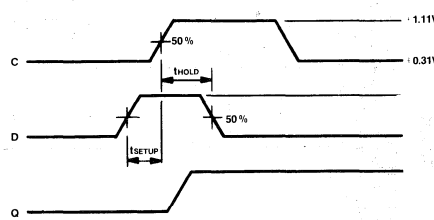



50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from $TP_{IN}$ to input pin and $TP_{OUT}$ to output pin.

INPUT PULSE
$t+ = t- = 1.0\text{nsec} \pm 0.2\text{nsec}$ (20 to 80%).




NOTE

$t_{setup}$ is the minimum time before the positive transition of the clock pulse (C) that information must be present at the data input (D).

$t_{hold}$ is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D).

*Fig.4 Switching time test circuit and waveforms at 25° C*

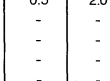
## ELECTRICAL CHARACTERISTICS

The SP9131 circuit has been designed to meet the DC specifications shown in the test table, after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to -2 volts. Test procedures are shown for only one input and one output. The other inputs and outputs are tested in the same manner.

| Test temp. | TEST VOLTAGES (V) $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{EE}$ |
|---|---|---|---|---|---|
| -30° C | -0.89 | -1.89 | -1.205 | -1.500 | -5.2 |
| +25° C | -0.81 | -1.85 | -1.105 | -1.475 | -5.2 |
| +85° C | -0.70 | -1.825 | -1.035 | -1.440 | -5.2 |

| Characteristic | Symbol | Pin under test | Test limits -30° C Min. | -30° C Max. | +25° C Min. | +25° C Typ. | +25° C Max. | +85° C Min. | +85° C Max. | Unit | VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH}$ Max. | $V_{IL}$ Min. | $V_{IHA}$ Min. | $V_{ILA}$ Max. | $V_{EE}$ | $V_{CC}$ (GND) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Power supply current | $I_E$ | 8 | - | 95 | - | 70 | 87 | - | 95 | mA | - | - | - | - | 8 | 1.16 |
| Input current | $I_{inH}$ | 4 | - | - | - | - | 600 | - | - | µA | 4 | - | - | - | 8 | 1.16 |
| | | 5 | - | - | - | - | 600 | - | - | | 5 | - | - | - | | |
| | | 6 | - | - | - | | 300 | - | - | | 6 | - | - | - | | |
| | | 7 | - | - | - | - | 300 | - | - | | 7 | - | - | - | | |
| | | 9 | - | - | - | - | 420 | - | - | | 9 | - | - | - | | |
| Input leakage current | $I_{inL}$ | 4,5 (Note 1) | - | - | 0.5 | - | - | - | - | µA | - | - | - | - | 8 | 1.16 |
| | | 6,7,9 (Note 1) | - | - | 0.5 | - | - | - | - | µA | - | - | - | - | 8 | 1.16 |
| Logic '1' output voltage | $V_{OH}$ | 2 | -1.06 | -0.89 | -0.96 | - | -0.81 | -0.89 | -0.70 | V | 5 | - | - | - | 8 | 1.16 |
| | | 2 (Note 2) | -1.06 | -0.89 | -0.96 | - | 0.81 | -0.89 | -0.70 | V | 7 | - | - | - | 8 | 1.16 |
| Logic '0' output voltage | $V_{OL}$ | 3 | -1.89 | -1.675 | -1.85 | - | -1.65 | -1.825 | -1.615 | V | 5 | - | - | - | 8 | 1.16 |
| | | 3 (Note 2) | -1.89 | -1.675 | -1.85 | - | -1.65 | -1.825 | -1.615 | V | 7 | - | - | - | 8 | 1.16 |
| Logic '1' threshold voltage | $V_{OHA}$ | 2 | -1.08 | - | -0.98 | - | - | -0.91 | - | V | - | - | 5 | - | 8 | 1.16 |
| | | 2 (Note 2) | -1.08 | - | -0.98 | - | - | -0.91 | - | V | - | - | 7 | 9 | 8 | 1.16 |
| Logic '0' threshold voltage | $V_{OLA}$ | 3 | - | -1.655 | - | - | -1.63 | - | -1.595 | V | - | - | 5 | - | 8 | 1.16 |
| | | 3 (Note 2) | - | -1.655 | - | - | -1.63 | - | -1.595 | V | - | - | 7 | 9 | 8 | 1.16 |
| **SWITCHING TIMES** | | | | | | | | | | | +1.11V | | Pulse in | Pulse out | -3.2V | +2.0V |
| Clock input propagation delay | $t_{9+2-}$ | 2 | 0.5 | 1.8 | 0.5 | 1.0 | 1.8 | 0.6 | 2.1 | ns | - | - | 9 | 2 | 8 | 1.16 |
| | $t_{9+2+}$ | 2 | - | - | | | | - | - | | 7 | - | 9 | 2 | | |
| | $t_{6+2+}$ | 2 | - | - | | | | - | - | | 7 | - | 6 | 2 | | |
| | $t_{6+2-}$ | 2 | - | - | | | | - | - | | - | - | 6 | 2 | | |
| Rise time (20 to 80 %) | $t_{2+}$ | 2 | 0.5 | 1.5 | 0.5 | 1.0 | 1.5 | 0.5 | 1.6 | | 7 | - | 9 | 2 | | |
| Fall time (20 to 80 %) | $t_{2-}$ | 2 | 0.4 | 1.4 | 0.4 | | 1.4 | 0.5 | 1.5 | | - | - | 9 | 2 | | |
| Set input propagation delay | $t_{5+2+}$ | 2 | 0.5 | 2.0 | 0.5 | 1.0 | 2.0 | 0.6 | 2.3 | ns | - | - | 5 | 2 | 8 | 1.16 |
| | $t_{12+15+}$ | 15 | - | - | | | | - | - | | 6 | - | 12 | 15 | | |
| | $t_{5+3-}$ | 3 | - | - | | | | - | - | | - | - | 5 | 3 | | |
| | $t_{12+14-}$ | 14 | - | - | | | | - | - | | 9 | - | 12 | 14 | | |
| Reset input propagation delay | $t_{4+2-}$ | 2 | - | - | | 1.0 | | - | - | ns | - | - | 4 | 2 | 8 | 1.16 |
| | $t_{13+15-}$ | 15 | - | - | | | | - | - | | 6 | - | 13 | 15 | | |
| | $t_{4+3-}$ | 3 | - | - | | | | - | - | | - | - | 4 | 3 | | |
| | $t_{13+14+}$ | 14 | - | - | | | | - | - | | 9 | - | 13 | 14 | | |
| Setup time | $t_{setup}$ | 7 | 1.0 | - | 1.0 | - | | 1.0 | - | ns | - | - | 6.7 | 2 | 8 | 1.16 |
| Hold time | $t_{hold}$ | 7 | 0.2 | - | 0.2 | - | | 0.2 | - | ns | - | - | 6.7 | 2 | 8 | 1.16 |
| Toggle frequency (max.) | $f_{Tog}$ | 2 | 520 | - | 520 | 600 | - | 500 | - | MHz | - | - | 6 | 2 | 8 | 1.16 |

NOTES
1. Individually test each input; apply $V_{IL}$ min to pin under test.
2. Output level to be measured after a clock pulse has been applied to the CE input (pin 6).



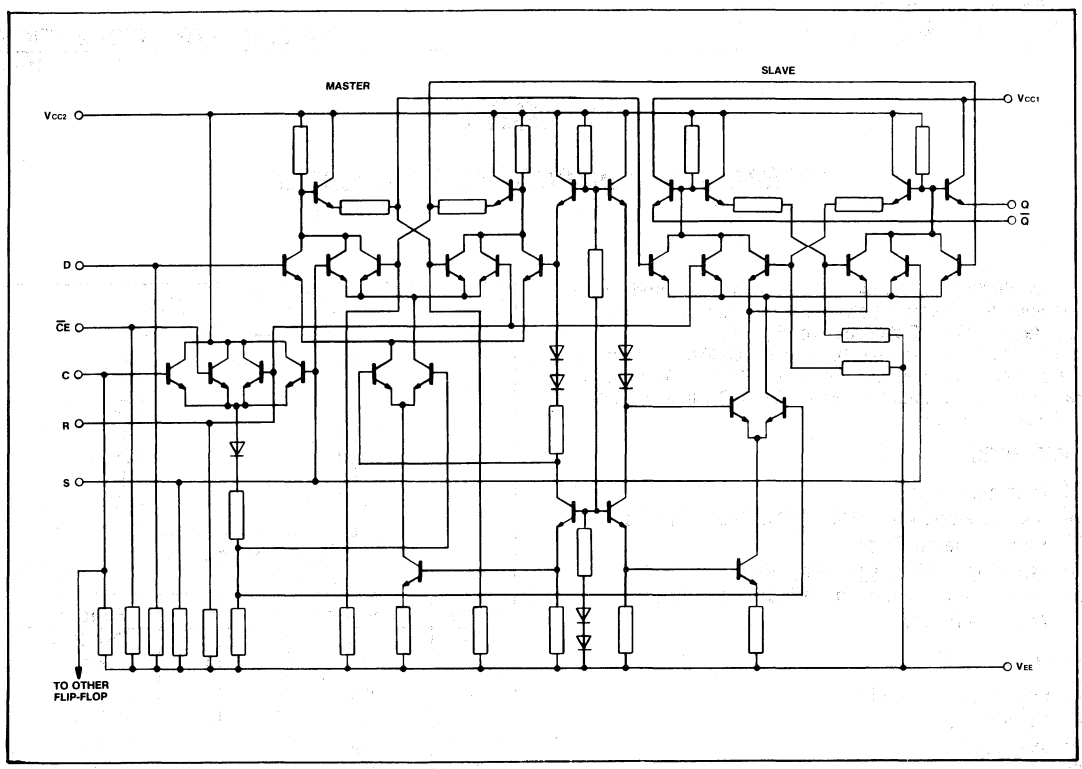



*Fig.5 Circuit schematic (½ of circuit shown)*

# SL9901

## 50MHz TRANSIMPEDANCE AMPLIFIER

The SL9901 is a monolithic silicon integrated circuit designed to interface between a detector diode and a decoder in a Fibre Optic Receiver System.

The device is also available as the SL9901AC, which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

### FEATURES

- High Sensitivity
- 50MHz Bandwidth (100 Mbit/s NRZ Data Rate)
- Wide Dynamic Range
- -40°C to +85°C Operating Range
- Usable in System with $10^{-9}$ BER at -36dBm Average Power

### APPLICATIONS

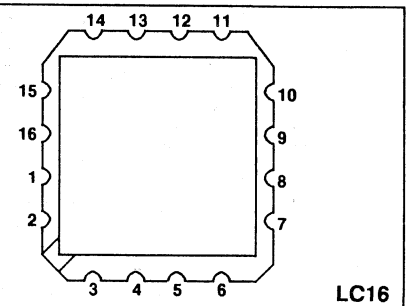
- Fibre Optic Data Links
- Nucleonics
- Instrumentation
- Current/Voltage Conversion

### ORDERING INFORMATION

**SL9901 B MP** (Industrial - miniature plastic surface mount package)
**SL9901 B LC** (Industrial - leadless chip carrier)
**SL9901 AC LC** (Military - leadless chip carrier, screened to MIL-STD-883C CLASS B)

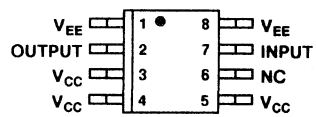
### ASSOCIATED PRODUCTS

**SP9960** 50M-Bit Manchester Biphase Encoder
**SP9921** 50M-Bit Manchester Biphase Decoder




LC16

| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | NC | 9 | OUTPUT |
| 2 | NC | 10 | NC |
| 3 | $V_{EE}$ | 11 | NC |
| 4 | $V_{EE}$ | 12 | $V_{CC}$ |
| 5 | $V_{EE}$ | 13 | $V_{CC}$ |
| 6 | $V_{EE}$ | 14 | $V_{CC}$ |
| 7 | NC | 15 | NC |
| 8 | NC | 16 | INPUT |




MP8

*Fig.1 Pin connections - top view*

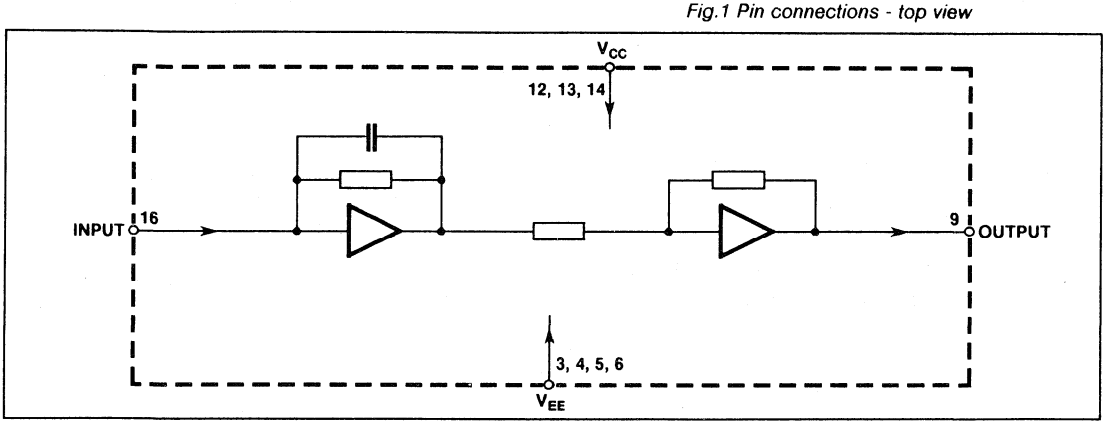



*Fig.2 Functional block diagram SL9901 (LC pinout)*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**
Supply voltage $V_{CC}$ = +4.50V to +5.50V. $T_{AMB}$ = -40°C to +85°C. Input current $I_I$ = 0.3μA to 30μA peak (see note 1). Output load $R_o$ = 200Ω minimum. Characteristic voltages are with respect to $V_{EE}$

| Characteristic | Symbol | Value | | Units | Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Supply current | $I_{CC}$ | 12 | 20 | mA | Outputs disabled |
| Input bias voltage | $V_{IB}$ | | 1.65 | V | $T_{AMB}$ = 25°C |
| Output bias voltage | $V_{OB}$ | 0.55 | 1.05 | V | $T_{AMB}$ = 25°C |
| Transimpedance gain | $G_T$ | 20 | 40 | kΩ | |
| Gain roll-off | $G_R$ | 6 | | dB/Oct | |
| 3dB bandwidth | $f_{3dB}$ | 50 | | MHz | 2.2pF on input See Fig. 3. |

NOTE 1. The device is guaranteed to operate at up to 84μA (peak), but above 30μA (peak) the output may be be clipped

## GUARANTEED CHARACTERISTICS

The following characteristics are guaranteed, but not tested, for the SL9901B at 25°C and over the full supply voltage range (+4.50V to +5.50V)

| Characteristic | Symbol | Value | | Units | Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Input noise current (RMS) | $I_N$ | | 4.0 | pA/√Hz | $C_{IN}$ = 2.2pF, $f$ = 10MHz |
| | | | 6.0 | pA/√Hz | $C_{IN}$ = 2.2pF, $f$ = 50MHz |
| Input bias variation | $dV_{IB}/dT$ | | 4.0 | mV/°C | |
| Input current at clipping | $I_{IC}$ | 30 | | μA | Peak current |
| Output impedance | $Z_O$ | | 100 | Ω | |
| 3dB Bandwidth | $f_{3dB}$ | 30 | | MHz | 10pF on input See Fig. 3. |

## ADDITIONAL INFORMATION

The following characteristics are typical for the SL9901 at +25°C, but not tested.

| Characteristic | Symbol | Value | Units | Conditions |
|---|---|---|---|---|
| Thermal resistance, chip-to-case | $\theta_{CC}$ | 40 | °C/W | |
| Thermal resistance, chip-to-ambient | $\theta_{CA}$ | 120 | °C/W | |
| Input impedance | $Z_I$ | 200 | Ω | |
| Pin capacitance | $C_P$ | 1-5 | pF | Pin to supplies |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | +7V |
| Input voltage (device sourcing current) | 0V |
| Input current (device sinking current) | 1mA |
| Output voltage (device sinking current) | 0V to $V_{CC}$ - 2V |
| Output current (device sourcing current) | 10mA |
| Storage temperature range | -65°C to +150°C |
| Maximum junction temperature | +175°C |

NOTE: For Currents in the range 10μA to 30μA (RMS) a DC offset is added to prevent the input from sourcing current. This gives a better approximation to normal use (see Fig. 4.)

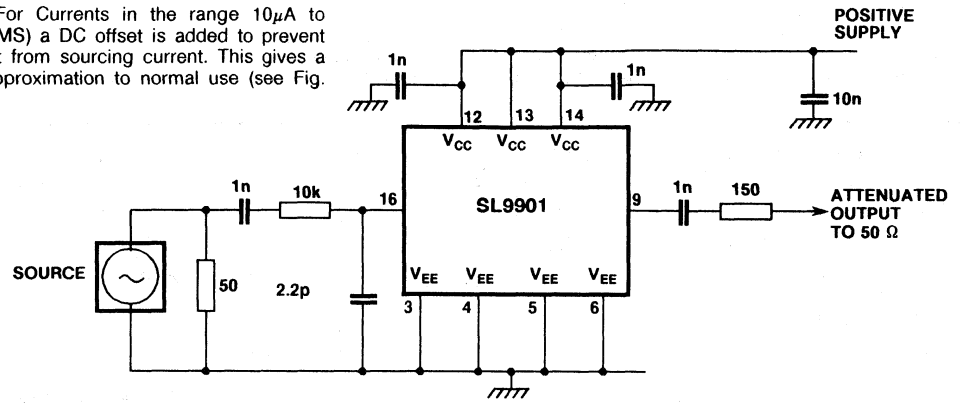



*Fig. 3 Test circuit (LC package)*

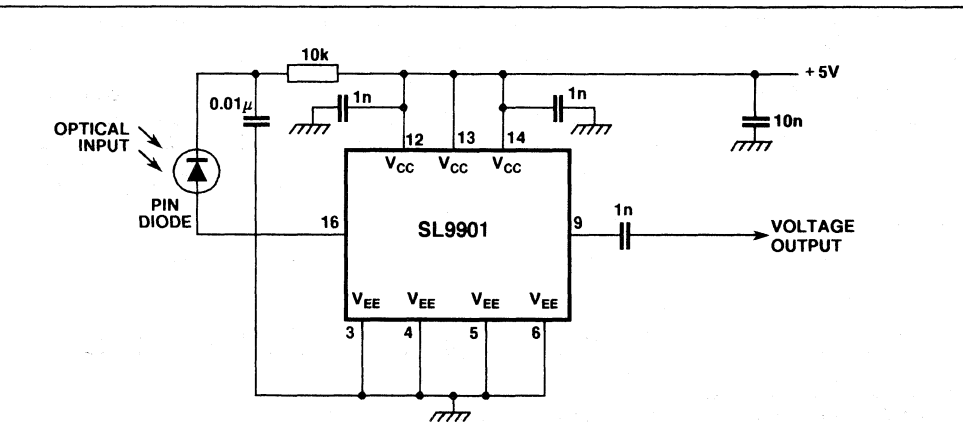



*Fig. 4 Typical application circuit (LC package)*

# SP9921

## 50 MBIT MANCHESTER BIPHASE DECODER

The SP9921 is a bipolar monolithic silicon integrated circuit for clock and data recovery from a Manchester biphase-mark encoded signal. It operates from a single 5V supply and has ECL outputs.

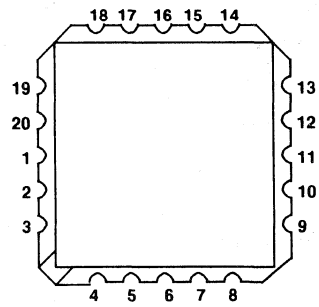
The device is also available as the SP9921AC, which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883C Class B. Data is available separately.

### FEATURES

- -40°C to +85°C Operating Temperature Range
- 50Mbit/s Clock and Data Rates.
- Single Supply Voltage
- Sensitive Differential Input
- ECL Outputs
- Input Signal Detection from Lock Detect Output
- No False Frequency Lock
- Correct Phase Lock on Random Data

### APPLICATIONS

- High Speed Serial Data Communications
- Fibre Optic Data Links
- Local Area Network (LAN) Interface




| Pin | Function | Pin | Function |
|---|---|---|---|
| 1 | RX – | 11 | RXD |
| 2 | NC | 12 | RXC |
| 3 | $V_{EE}$ | 13 | RXO |
| 4 | $V_{EE}$ | 14 | $V_{CC}$ |
| 5 | RECF | 15 | $V_{CC}$ |
| 6 | BD | 16 | NC |
| 7 | REFF | 17 | RCI |
| 8 | $V_{EE}$ | 18 | $V_{CC}$ |
| 9 | RCO | 19 | $V_{CC}$ |
| 10 | PLO | 20 | RX+ |

*Fig.1 Pin connections - top view*

### ORDERING INFORMATION

**SP9921 B LC** (Industrial - leadless chip carrier)
**SP9921 AC LC** (Military - leadless chip carrier, screened to MIL-STD-883C CLASS B)

### ASSOCIATED PRODUCTS

**SL9901** 50MHz Transimpedance Amplifier
**SP9960** 50M-Bit Manchester Biphase Encoder

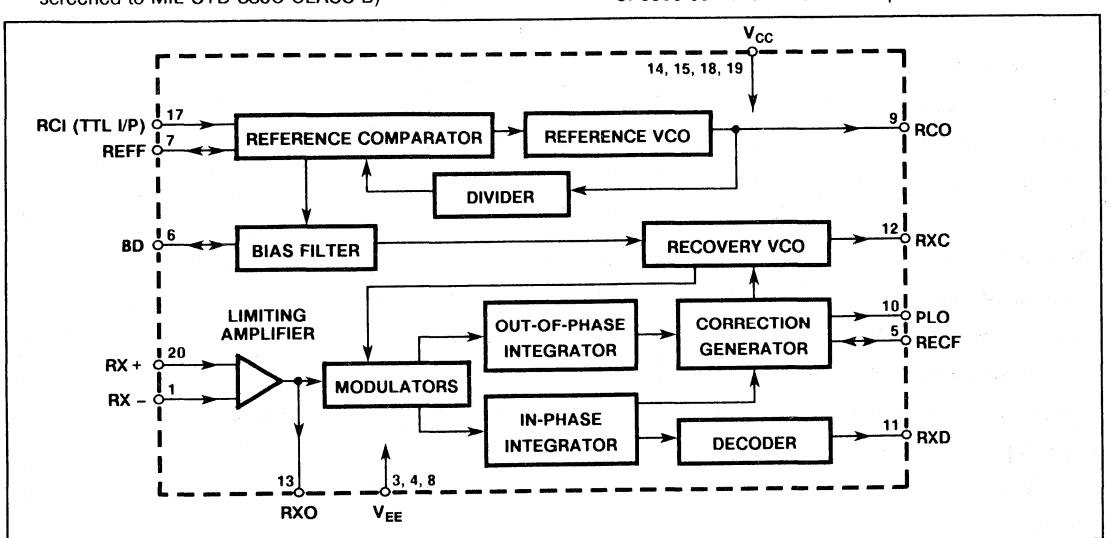



*Fig.2 Functional block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**

Supply voltage $V_{CC}$ = +4.50V to +5.50V, $T_{AMB}$ = −40°C to +85°C
Programming input low voltage $V_{ILP}$ = 0V to 0.4V. TTL input low voltage $V_{ILT}$ = 0.8V max, TTL input high voltage $V_{IHT}$ = 2.0V min. Differential receiver voltage $V_{RD}$ = 10mV to 2.00V peak to peak. Bit Error Rate BER = $10^{-9}$ max.

| Characteristic | Symbol | Value | | Units | Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Supply current | $I_{CC}$ | | 200 | mA | Output Unloaded |
| TTL input sink current | $I_T$ | | 10 | µA | $T_{AMB}$ = +25°C |
| | | | 30 | µA | $T_{AMB}$ = +25°C. |
| ECL output high voltage | $V_{OH}$ | $V_{CC}$-0.96 | $V_{CC}$-0.81 | V | $T_{AMB}$ = +25°C See note 1 |
| | | $V_{CC}$-0.89 | $V_{CC}$-0.70 | V | $T_{AMB}$ = +85°C See note 1 |
| | | $V_{CC}$-1.06 | $V_{CC}$-0.89 | V | $T_{AMB}$ = -40°C See note 1 |
| ECL output low voltage | $V_{OL}$ | $V_{CC}$-1.85 | $V_{CC}$-1.62 | V | $T_{AMB}$ = +25°C See note 1 |
| | | $V_{CC}$-1.82 | $V_{CC}$-1.61 | V | $T_{AMB}$ = +85°C See note 1 |
| | | $V_{CC}$-1.89 | $V_{CC}$-1.67 | V | $T_{AMB}$ = -40°C See note 1 |
| Receive offset voltage | $V_{RO}$ | | 5.0 | mV | |
| Minimum VCO frequency | $f$L | | 20 | MHz | |
| Maximum VCO frequency | $f$H | 50 | | MHz | |

NOTE 1. $[V_{RX}+] - [V_{RX}-] > 100mV$ to ensure a good ECL output on RXO output load as per Fig. 4b.

## GUARANTEED CHARACTERISTICS

The following characteristics are guaranteed, but not tested, for the SP9921 at +25°C and over the full supply voltage range (+4.50V to +5.50V). Voltages are with respect to the negative power supply ($V_{EE}$)

| Characteristic | Symbol | Value | | Units | Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| ECL output source current | $I_{SOURCE}$ | 1.2 | | mA | See Fig. 5. |
| RCI frequency | $f_R$ | 3.9 | 10.1 | MHz | |
| PCM clock high period | $t_{RH}$ | 20 | | ns | |
| PCM clock low period | $t_{RL}$ | 20 | | ns | |
| RCO rise or fall time | $t_{RRF}$ | | 4 | ns | $R_L$ = 1kΩ, Fig. 4a. |
| REFF source current pulse | $I_{RF+}$ | 100 | 350 | µA | |
| REFF sink current pulse | $I_{RF-}$ | 100 | 350 | µA | |
| Minimum half period | $t_{MIN}$ | $0.3t_B$ | | ns | See note 2 |
| Minimum half period | $t_{MAX}$ | | $0.7t_B$ | ns | See note 2 |
| Operating voltage (REFC) | $V_{OP}$ | $V_R$-0.33 | $V_R$+0.33 | V | See note 3 |
| Free-running voltage (REFC) | $V_{FR}$ | $V_R$-0.33 | $V_R$+0.33 | V | See note 3 |
| Free-running frequency offset (wrt $f_{RCO}$) | $\Delta_{FR}$ | -2.0 | +2.0 | % | Input grounded |
| Lock on range (wrt $f_{RCC}$) | $\Delta_L$ | -2.0 | +2.0 | % | Circuit as Fig.11 With C5 = 0 |

## GUARANTEED CHARACTERISTICS (continued)

| Characteristic | Symbol | Value | | Units | Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| RXC fall time | $t_{RXF}$ | | 4 | ns | $R_L$ = 1kΩ, Fig. 4a. |
| RXC rise time | $t_{RXR}$ | | 4 | ns | $R_L$ = 1kΩ, Fig. 4a. |
| Output delay | $t_{OD}$ | | 5 | ns | $R_L$ = 1kΩ, Fig. 4a. |

NOTES

2. $t_B$ typically = $1/f_{RCO}$ secs
3. $V_R$ typically = $V_{CC}$-1 volts

## ADDITIONAL INFORMATION

The following characteristics are typical for the SP9921B at +25°C, but not tested.

| Characteristic | Symbol | Value | Units | Conditions |
|---|---|---|---|---|
| Thermal resistance chip-to-case | $\theta_{CC}$ | 28 | °C/W | |
| Thermal resistance chip-to-ambient | $\theta_{CA}$ | 73 | °C/W | |
| Pin capacitance | $C_P$ | 3 | pF | Pin to supplies |
| ECL output sink current | $I_{SINK}$ | 2 | mA | See Fig. 5 |
| Receive bias voltage | $V_{RB}$ | $V_{CC}/2$ | V | |
| Receive input impedance | $Z_{RI}$ | 1000 | Ω | Differential input |
| RCI rise time | $t_{RR}$ | 20 | ns | |
| RCI fall time | $t_{RF}$ | 20 | ns | |
| $f$H temperature coefficient | $\Delta f$H | -0.2 | MHz/°C | |
| RCO frequency | $f_{RCO}$ | 18 | MHz | $V_{REFF}$ = 2.5V |
| | | 46 | MHz | $V_{REFF}$ = 3.0V |
| | | 54 | MHz | $V_{REFF}$ = 3.5V |
| Reference loop gain | $G_{REF}$ | 40 | MHz/V | $f_{RCO}$ = 20MHz |
| | | 100 | MHz/V | $f_{RCO}$ = 30MHz |
| | | 55 | MHz/V | $f_{RCO}$ = 40MHz |
| | | 20 | MHz/V | $f_{RCO}$ = 50MHz |
| Frequency - voltage ratio | OCF/V | 8.5 | MHz/V | $f_{RCO}$ = 50MHz |
| | | 9.5 | MHz/V | $f_{RCO}$ = 40MHz |
| | | 11.0 | MHz/V | $f_{RCO}$ = 30MHz |
| | | 6.5 | MHz/V | $f_{RCO}$ = 20MHz |

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | 7V |
| Input voltage | - 0.3V to $V_{CC}$ + 0.3V |
| Output voltage | 0V to $V_{CC}$ |
| Storage temperature range | - 55°C to + 150°C |
| Maximum junction temperature | + 175°C |

| PIN DESCRIPTIONS | | |
|---|---|---|
| **Symbol** | **Pin no** | **Description** |
| **REFF** | 7 | **Reference Filter (Current Output/Voltage Input)**. A series RC network should be connected between this pin and $V_{EE}$ to provide the filtering for the control of the reference VCO. |
| $V_{EE}$ | 8 | **Negative Power Supply** |
| **RCO** | 9 | **Reference Clock Out (ECL Output)**. This pin should output a clock which is frequency-locked to the reference clock input (RCI pin) but which is 5 times its frequency. |
| **PLO** | 10 | **Phase Lock Out (ECL Output)**. This pin goes low for any bits where the output of the in-phase integrator (data) fails to exceed the output of the out-of-phase integrator (error) by a set margin. |
| **RXD** | 11 | **Received Data** (ecl output). This pin outputs the decode received data. |
| **RXC** | 12 | **Received Clock (ECL Output)**. This pin outputs the recovered clock. |
| **RXO** | 13 | **Receive Out (ECL Output)**. This pin outputs the undecoded received data. |
| $V_{CC}$ | 14, 15 | **Positive Power Supply** |
| **NC** | 16, 2 | **No Connection** This pin should be left unconnected for normal operation. |
| **RCI** | 17 | **Receive Clock In (TTL Input)**. This is the input for the reference clock which sets the free-running frequency for the recovery VCO. Its frequency should be close to one fifth of the received data rate. |
| $V_{CC}$ | 18, 19 | **Positive Power Supply** |
| **RX +**<br>**RX –** | 20<br>1 | **Receive Plus and Minus (Analog Voltage Inputs)**. These are the differential inputs to the limiting receive amplifier. They are self-biasing and would normally be capacitively coupled. For a single-ended input the unused pin should be capacitively coupled to ground. |
| $V_{EE}$ | 3, 4 | **Negative Power Supply** |
| **RECF** | 5 | **Recovery Filter (Current Output/Voltage Input)**. A series RC network should be connected between this pin and ground to provide the filtering for the control of he recovery VCO. |
| **BD** | 6 | **Bias Decoupling (Decoupling Node)**. A capacitor should be connected between this pin and ground to eliminate noise on the bias voltage generated by the reference PLL and which sets the free-running frequency of the recovery VCO. |

## FUNCTIONAL DESCRIPTION

Fig. 2 shows the simplified block diagram of the device. It locks onto incoming data, recovers the clock and decodes the data making use of a reference clock input at one fifth of the data rate.

### Receive Path

Data is received at the differential input pins (RX+/-) of the limiting amplifier which outputs the digital received signal for monitoring at the amplifier output pin (RXO). This signal is fed into a modified Costas loop which outputs the recovered clock (RXC pin) and the decoded data (RXD pin).

Fig. 3 shows how the input signal is decoded. The Manchester biphase-mark code uses a transition at the centre of the bit to indicate a one and the absence of a transition to indicate a zero. In addition there is always a transition at the end of the bit.

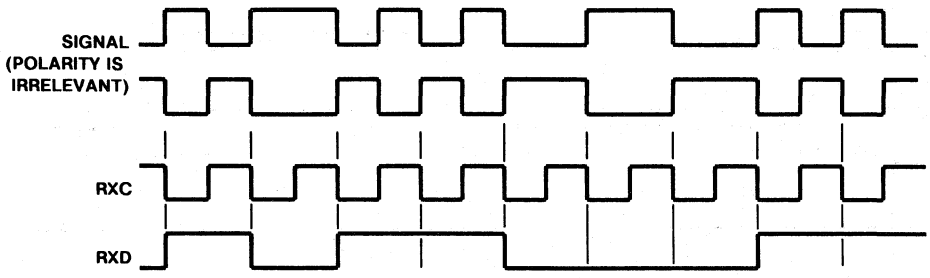
### Phase-Locking and Signal Recovery

The SP9921 can be used in systems operating over a wide range of data rates without false frequency lock. This is achieved using a reference VCO and a recovery VCO.

The reference VCO is phase-locked to the reference clock input (RCI pin). This generates an internal clock at 5 times the frequency of the reference clock input. The output of this VCO is output for monitoring on the reference clock output (RCO pin). Filtering of the bias control signal to the VCO is performed at the reference filter pin (REFF).

The bias control signal for the reference VCO is filtered at the bias decoupling pin (BD) and used to set the free-running frequency of the recovery VCO. The recovery VCO drivers the receive clock (RXC pin) and the modulators which in turn drive the integrators. The integrators analyse the components of the signal which are in phase and 90° out of phase and so obtain the recovered data and the correction signal for the modified Costas loop. The correction signal is filtered at the recovery filter pin (RECF).

The modified Costas loop also pulls the phase-lock output pin (PLO) low for any bits when the output of the in-phase integrator (data) does not exceed the output of the out-of-phase integrator (error) by a set margin. This can occur when there is a loss of data, if there is too much noise on the link (even if no data is corrupted) or if the Costas loop has difficulty locking.




NOTE: There is a delay of 3 clock cycles between the input signal and the decoded data output.

*Fig. 3 Biphase-Mark Decoding*

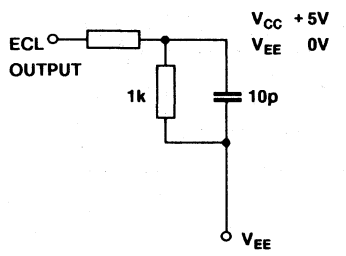



*Fig. 4a*

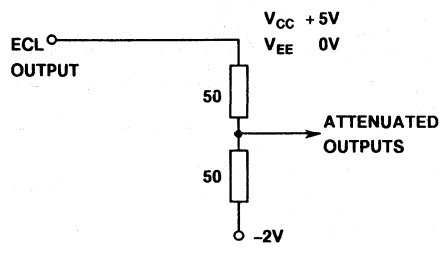



*Fig. 4b*

*Fig. 4 ECL Output test loading*

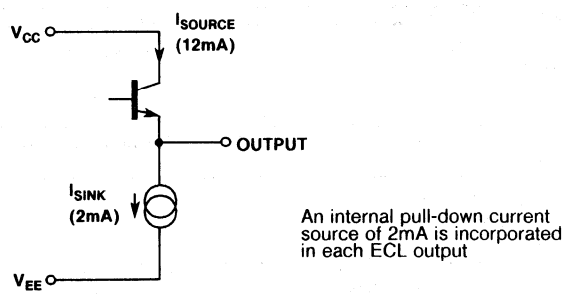



*Fig. 5 ECL output circuitry*

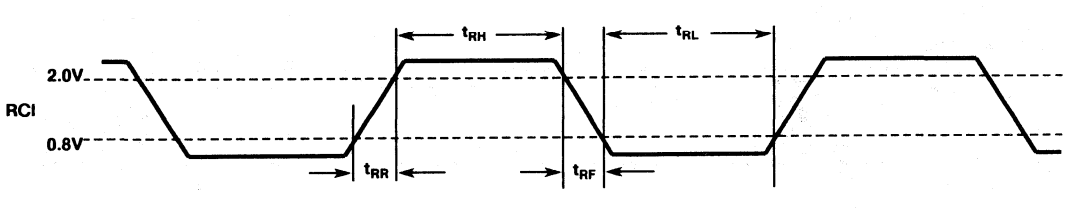



*Fig. 6 Timing - reference clock in*

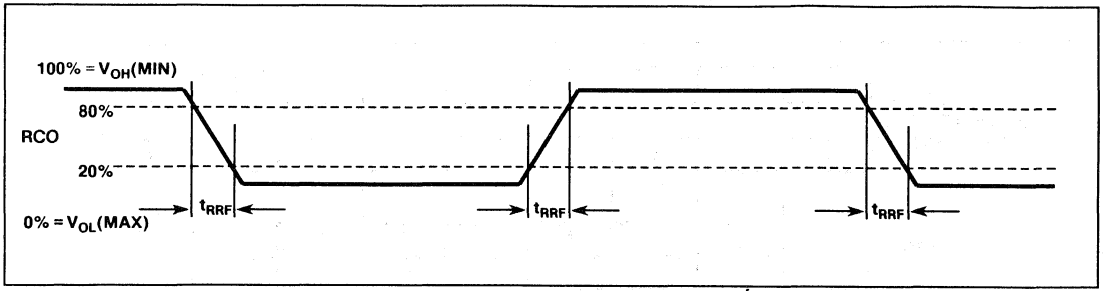



*Fig. 7 Timing - reference clock out*

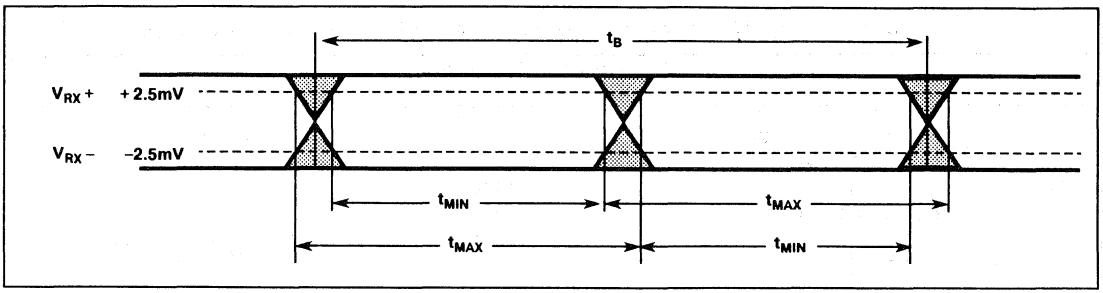



*Fig. 8 Timing - receive data*

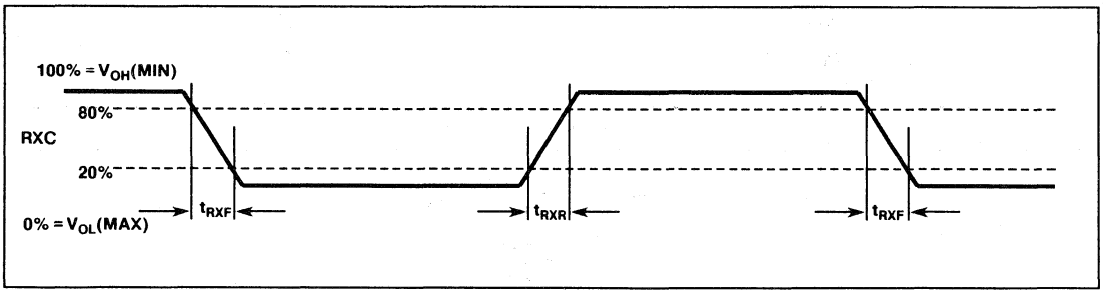



*Fig. 9 Timing receive clock*

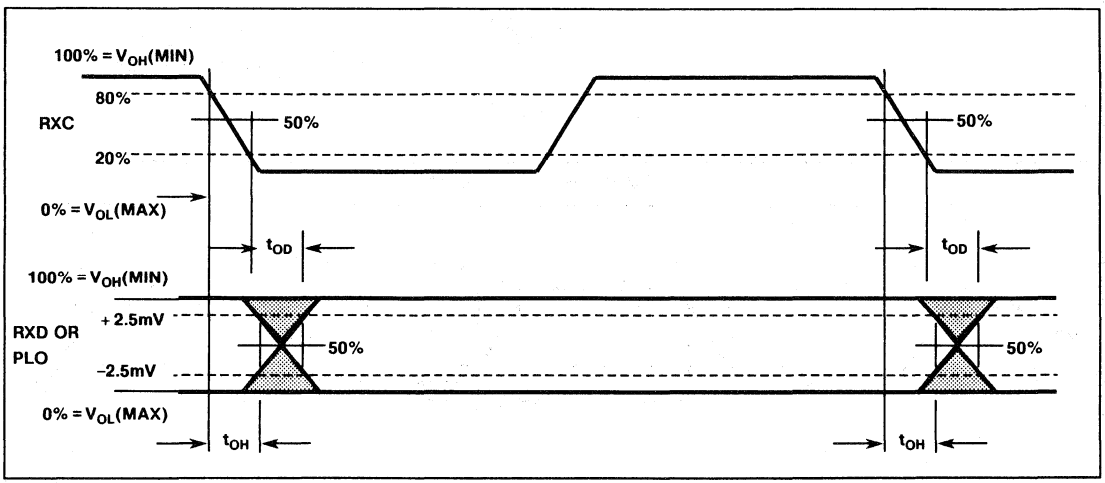
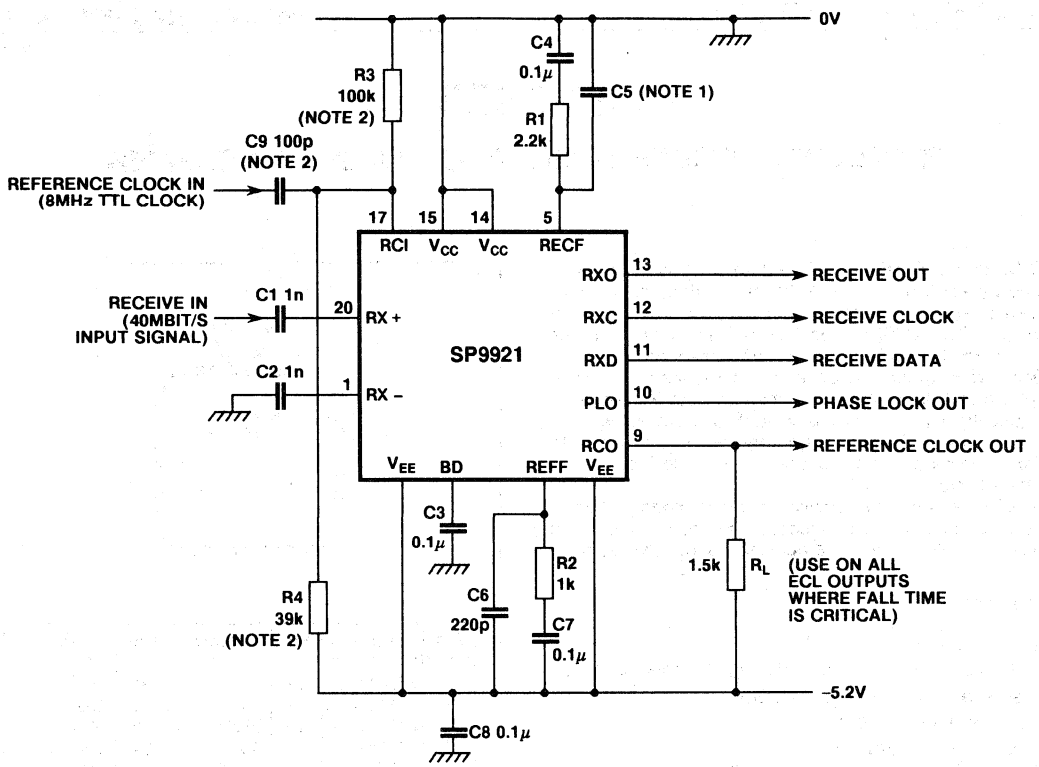



*Fig. 10 Timing - receive data and phase lock out*




1. C5 should be zero for most applications to maximise capture range, in applications where jitter is of paramount importance then a small value up to 47pF maybe used.
2. C9, R3 and R4 may be removed and the TTL reference clock connected directly to pin 17, provided that the TTL signal is referenced to $V_{EE}$

*Fig.11. Typical application circuit*

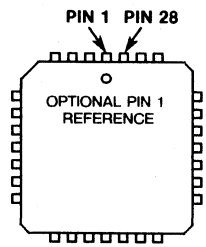
# SP9930

## FDDI CLOCK RECOVERY AND DE-SERIALISING RECEIVER

FDDI (Fibre Distributed Data Interface) is a standard defined by ANSI (American National Standard Institute) for a token passing ring network operating at a user rate of 100MB/s. The SP9930 receiver is one of two devices which service the 4B/5B codec to NRZI interface.

Only two external components are required to provide RC phase lock loop filtering. When no data is present at the input the internal VCO is locked to 5 times the local symbol clock. This arrangement gives an accurate 125MHz free running clock and a very short lock on time of less than 1 microsecond.

When data is input the device changes mode and locks to the data. Following clock recovery the data is converted from NRZI to NRZ before the parallel to serial conversion.




HG28

| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | RDATA $D_1$ | 11 | FLTR | 21 | SDI + |
| 2 | RDATA $D_2$ | 12 | $AV_{EE}$ | 22 | SDI |
| 3 | RDATA $D_3$ | 13 | ERROR | 23 | SDO |
| 4 | RDATA $D_4$ | 14 | $AV_{CC}$ | 24 | LSCLK |
| 5 | TGND | 15 | LTXD | 25 | MODE |
| 6 | DGND | 16 | LPBCK | 26 | RBYCLK |
| 7 | SRDATA | 17 | TEST | 27 | $DV_{CC}$ |
| 8 | EGND | 18 | RCVD- | 28 | RDATA $D_0$ |
| 9 | RBCLK | 19 | RCVD + | | |
| 10 | AGND | 20 | $DV_{EE}$ | | |

*Fig.1 Pin connections - top view*

### FEATURES

- FDDI Standard Compatible
- 125MHz Clock Guaranteed (Typ. 170MHz at 25°C)
- Receive bit Clock Jitter <2.3ns
- Lock on time <1.0μs
- +5.0V/ -5.2V Supplies
- Very Low External Component Requirement

### APPLICATIONS

- FDDI Communication System

### ORDERING INFORMATION

**SP9930 C HG** (Commercial - Quad Cerpac package)

### ASSOCIATED PRODUCTS

**SP9970** FDDI transmitter
**SP9944E** 200MBit/s data regenerator
**SL9901** 50MHz transimpedance amplifier
**SP9921** 50MBit/s Manchester biphase-mark Decoder
**SP9960** 50MBit/s Manchester biphase-mark Encoder

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | +5.5V |
| Supply voltage $V_{EE}$ | -5.75V |
| Operating temperature | 0°C to +70°C |
| Maximum junction temperature | +125°C |
| Storage temperature | -55°C to +150°C |

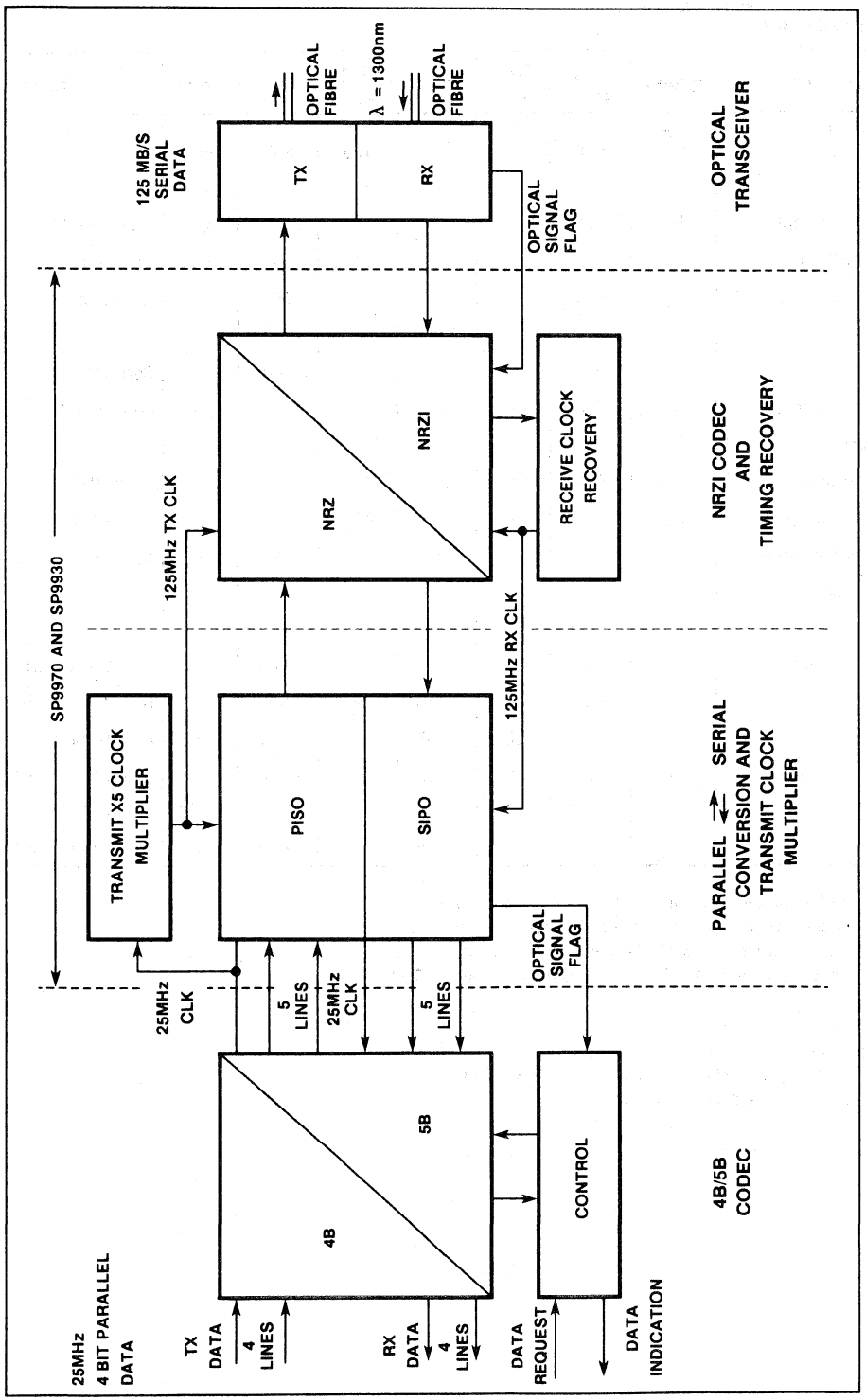



*Fig.2 FDDI physical layer (block diagram)*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**
$T_{AMB}$ = +25°C, $V_{CC}$ = +5V ±10%, $V_{EE}$ = -5.25V ±10%
Full temperature range = 0°C to +70°C

**DC CHARACTERISTICS**

| Characteristic | Symbol | Temp. (°C) | Test level | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Supply current | $I_{CC}$ | Full | 1 | | 25 | 50 | mA | |
| | $I_{EE}$ | Full | 1 | | 150 | 200 | mA | |
| **TTL Inputs** | | | | | | | | |
| Logic '1' current | $I_{IH}$ | Full | 1 | | 3 | 20 | µA | See Note 1 |
| Logic TEST pin | | Full | 1 | | 120 | 130 | µA | See Note 1 |
| Logic '0' current | $I_{IL}$ | Full | 1 | | | -600 | µA | See Note 1 |
| **ECL Inputs** | | | | | | | | |
| Logic '1' current | $I_{IH}$ | Full | 1 | | | 200 | µA | See Note 3 |
| Logic '0' current | $I_{IL}$ | Full | 1 | -0.01 | | 300 | µA | See Note 4 |
| **TTL Outputs** | | | | | | | | |
| Logic '1' voltage | $V_{OH}$ | Full | 1 | 2.4 | 2.9 | | V | $I_{OH}$ = -400µA |
| Logic '0' voltage | $V_{OL}$ | Full | 1 | | 0.35 | 0.525 | V | $I_{OL}$ = 4mA |
| Short circuit current | $I_{OS}$ | Full | 5 | -3.0 | | -40 | mA | $V_O$ = 0V |
| Output current | | | | | | | | |
| **ECL Outputs** | | | | | | | | |
| Logic '1' voltage | $V_{OH}$ | 0 | 4 | -1.17 | -0.9 | -0.84 | V | RL = 100Ω to -2V |
| | | +25 | 1 | -1.13 | -0.85 | -0.8 | V | RL = 100Ω to -2V |
| | | +70 | 4 | -1.07 | -0.8 | -0.72 | V | RL = 100Ω to -2V |
| Logic '0' voltage | $V_{OL}$ | 0 | 4 | -1.95 | -1.7 | -1.48 | V | RL = 100Ω to -2V |
| | | +25 | 1 | -1.95 | -1.7 | -1.48 | V | RL = 100Ω to -2V |
| | | +70 | 4 | -1.95 | -1.7 | -1.45 | V | RL = 100Ω to -2V |

NOTES
1. TTL input under test set to 2V all other TTL inputs set to 0.8V
2. TTL input under test set to 0.8V all other TTL inputs set to 2V
3. ECL input under test set to-0.81V all other ECL inputs set to -1.85V
4. ECL input under test set to -1.85V all other ECL inputs set to -0.81V

**TEST LEVELS**
Level 1 - 100% production tested
Level 4 - Parameter guaranteed by design and characteristics testing
Level 5 - Parameter is a typical vaue only

## AC CHARACTERISTICS

Guaranteed by design and AC characteristics testing.
Characteristics assume 125M/bit operation

| Characteristic | Symbol | Temp. (°C) | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **ECL Outputs** | | | | | | | |
| Rise times 20%-80% | $t_R$ | 0 | | 2 | 2.5 | ns | RL = 100Ω to -2V |
| | | 25 | | 2.7 | 3 | ns | RL = 100Ω to -2V |
| | | 70 | | 3 | 5 | ns | RL = 100Ω to -2V |
| Fall times 20%-80% | $t_F$ | 0 | | 2 | 2.5 | ns | RL = 100Ω to -2V |
| | | 25 | | 2.7 | 3 | ns | RL = 100Ω to -2V |
| | | 70 | | 3 | 5 | ns | RL = 100Ω to -2V |
| **TTL Outputs** | | | | | | | |
| Rise times 20%-80% | $t_R$ | 0 | | 5 | 12 | ns | |
| | | 25 | | 6 | 16 | ns | |
| | | 70 | | 7 | 19 | ns | |
| Fall times 10%-90% | $t_F$ | 0 | | 6 | 12 | ns | |
| | | 25 | | 6 | 12 | ns | |
| | | 70 | | 6 | 13 | ns | |
| **RBCLK** | | | | | | | |
| Duty cycle distortion | $D_{CD}$ | Full | -2.5 | -2 | +2.5 | ns | |
| Jitter p-p | $t_{CJ}$ | Full | -0.5 | 0.2 | +0.5 | ns | LSCLK to RBCLK |

### ELECTRICAL CHARACTERISTICS DEFINITIONS

Duty cycle distortion (DCD)
The maximum difference between the high time of this signal and the low time.
Jitter (tcj)
The maximum deviation of the rising edge of LSCLK to the rising edge of RBCLK.

| CONTROL INPUTS (TTL) | | | | FUNCTION | SRDATA (ECL) | RDATAn (TTL) | SDO (TTL) | MODE (TTL) |
|---|---|---|---|---|---|---|---|---|
| SDI (ECL) | | LPBACK (TTL) | TEST (TTL) | | | | | |
| + | - | | | | | | | |
| Hi | Lo | 1 | 0 | Normal operation | RCVD data | Decoded data from RCVD | 1 | 1 = locked 0 = unlocked |
| Lo | Hi | 1 | 0 | Fibre optic receive disabled | Lo | 0 | 0 on next LSCLK ↑ edge | 0 |
| X | X | 0 | 0 | Loopback mode | LPBCK data | Decoded data from LPBCK | 1 | 1 = locked 0 = unlocked |
| X | X | X | X | Test mode for manufacturer's use only | X | 1 | X | X |

*Table 1 Receiver function table*

## INTRODUCTION TO FDDI SYSTEMS

FDDI (Fibre Distributed Data Interface) is a standard defined by ANSI (American National Standard Institute) for a token passing ring network operating at a user rate of 100MB/s. The standard consists of 4 documents;

1. Physical Media Dependant (PMD)
2. Physical Layer Protocol (PHY)
3. Media Access Control (MAC)
4. Station Management (SMT)

These documents correspond closely with the OSI seven layer model, PMD and PHY are sublayers of the OSI physical layer. The MAC document implements some of the OSI Data link layer. Overall control of the PHY and MAC functions is provided by the SMT.

### Technical Overview (The Physical Layer)

Fig. 2 shows a block diagram of the Physical Layer, the first section is the 4B/5B codec, here the data is in symbols, four bits wide at a rate of 25MB/S. Each four bit code received, is converted into a 5 bit code according to a pre-defined table. This extra bit is added to prevent long runs of zeros, it also allows the addition of signalling words by the control section. A circuit incorporating the codec function is not yet available but it could be implemented in semi-custom CMOS, such as CLA60K series.

After conversion to a 5-bit word the data undergoes a parallel to serial conversion, this multiplies the transmission rate up to 125MB/s. In order to clock the data out at this rate the clock needs to be multiplied five times up to 125MHz, this is achieved with a phase locked loop in this chip set. Before transmission over the fibre the data is converted to a code called NRZI, in this code a '1' is represented by a transition and '0' as no transition. This coding maximises transistions without increasing the bandwidth of the signals, and when combined with the 4B/5B coding this system minimises the DC content of the signal. On the receive side the transitions within the NRZI code are used to recover the 125MHz clock.

FDDI specifies a fibre optic transmission medium of 62.5 μm core multimode fibre (this is the recommended core size; 50, 85 and 100μm cored fibres are allowed alternatives), a 1300nm LED source, and a maximum distance between nodes of 2km.

Up to 500 nodes and a total fibre length of 200km are supported by FDDI. A distance of up to 2km is supported by the present multimode interface, and work is in progress to modify the standard to allow a single mode interface for larger distances.

A further modified network called FDDI-II is proposed that uses 6MB/s time slots for isochronous data such as voice, low rate video and point to point data links. FDDI-II uses the same physical layer as FDDI-I.

## THE FDDI CHIPS

At present FDDI chips are available which support the 4B/5B to NRZI interface, this circuitry is contained in two 28 pin devices, a transmitter chip and a receiver chip Both chips operate on a supply of +5V/-5.2V. TTL and differential ECL interfaces are used for the 25MB/s and 125MB/s signals respectively, all control and alarm signals are TTL levels.

The ECL interfaces are 10KH compatible. Although the devices are designed to operate at a line rate of 125MB/s, performance up to 170MB/s can be expected at 25°C. Both transmitter and receiver have a loopback mode, serial data from the local transmitter is looped back to the local receiver. The devices are manufactured using a high speed bipolar process.

### The SP9930 Receiver

The receiver (device type SP9930) is powered from a +5V and -5.2V supply with currents of 40mA and 170mA respectively. Only two external components are required, a capacitor and a resistor, these provide the phase lock loop filtering.

A block diagram of the receiver is shown in Fig. 3. the serial data is input from the fibre optic receiver through a differential ECL input stage. When no data is present at the input, indicated by a low on Signal Detect Input (SDI), the internal VCO is locked to five times the local symbol clock (LSCLK). This arrangement gives an accurate 125MHz free running clock and a very short lock-on time of $< 1\mu s$. When the SDI pin is high the device changes mode and locks to the received data (RCVD), the MODE pin is used to indicate which mode the device is operating in.

While the VCO is locked to the RCVD its frequency is continuously monitored, if the frequency error exceeds ±1% the phase locked loop (PLL) changes back to the LSCLK mode.

Once a frequency accuracy of ±0.5%, relative to the LSCLK is achieved the PLL returns to the RCVD mode, provided SDI is high. Jitter on the receive bit clock should be <2.27ns pk-pk provided the RCVD jitter is <4.2ns pk-pk. External components are used to select the time constant of the PLL, and the error voltage from the comparator is available at an external pin (ERROR) through a buffer.

Following clock recovery the data is converted from NRZI to NRZ before the parallel to serial conversion. Parallel data is presented as five bit wide symbols at the RDATA outputs (TTL levels). The data bits transmitted will not necessarily appear on the same pins as they were transmitted, this is because the framing is performed in the 4B/5B decoder. A 25MHz Receive Byte Clock (RBYCLK) is provided, to allow data to be clocked into the following word alignment and decoding circuits.

A Signal Detect Output (SDO) is provided, this directly reflects the SDI input, except that it is clocked out on the next LSCLK positive edge after SDI changes.

## PHASE LOCKED LOOP CHARACTERISTICS

The receiver PLL is more complex than the transmitter as it is required to lock on to varying data patterns. Under worst conditions (Master Line State) 1 transistion occurs every 10 bits. However the device will still recover clock with only 1 transition in every 16 timeslots with the filter components shown in fig 4.

Unlike the transmitter the receiver PLL operates in two modes. In mode 0 the VCO is locked to five times the LSCLK input and in mode 1 the VCO is locked to the incoming data. As shown in table 1 the actual operating mode is indicated by the logic level at the mode output pin. While in mode 1 a frequency counter monitors the VCO frequency to check that it is five times the LSCLK frequency; if the error is more than ± 1% the PLL defaults back to mode 0 and this indicates that lock has been lost. Before switching back to mode 1 the VCO must achieve an accuracy of ± 0.5% when compared to five times the LSCLK input.

Note that the measurement period is 40 cycles of the LSCLK so that at 25MHz at least 1.6μs must be allowed before the PLL will switch back to mode 1.

Whenever the SDI flag is raised the PLL will automatically switch to mode 0 as this indicates there is no valid input signal. Conversely when the 'LP BACK' signal goes 'low' the device will default to mode '1', this allows loopback to be used regardless of the optical input signal condition.

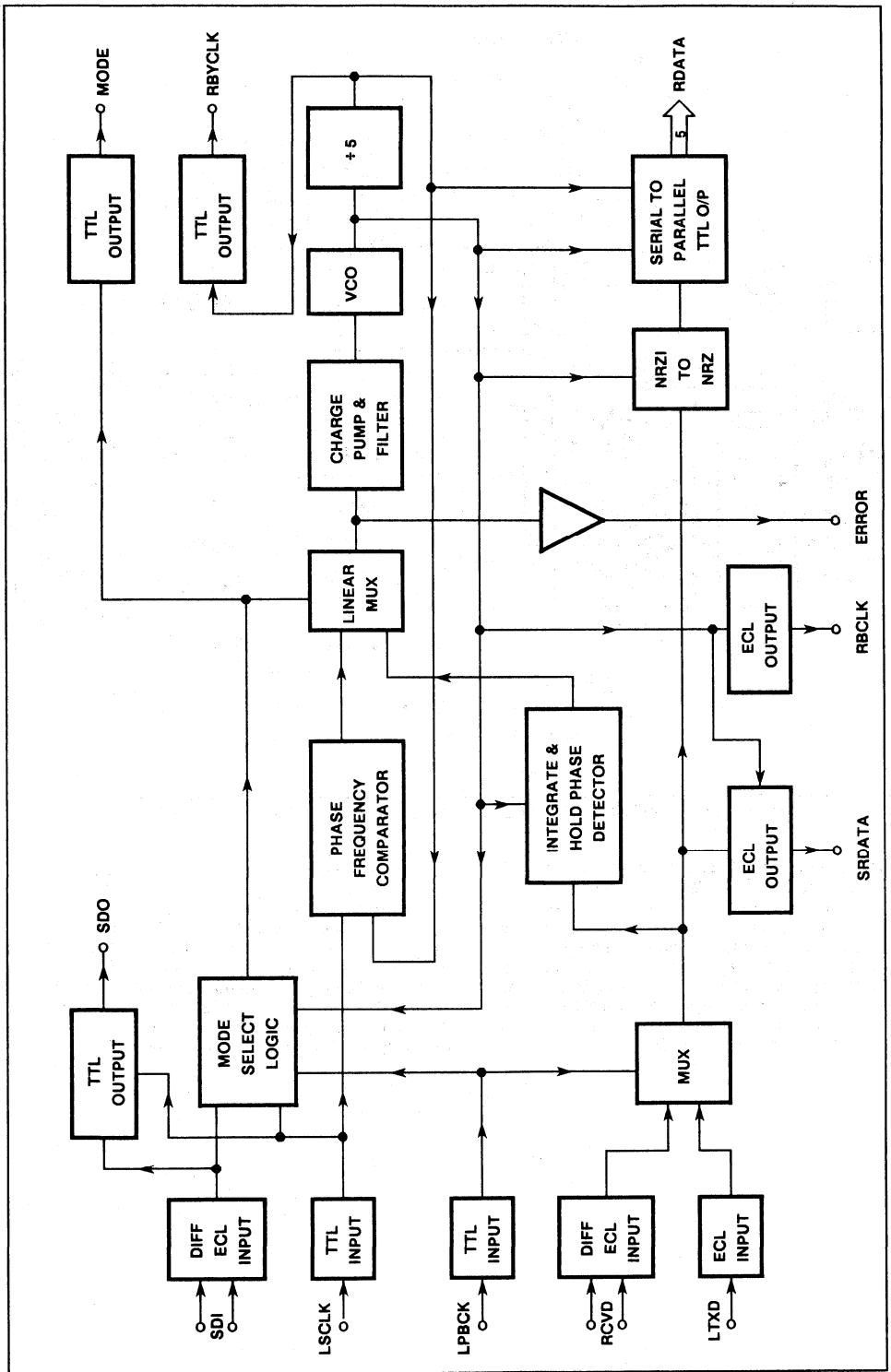



*Fig.3 SP9930 receiver block diagram*

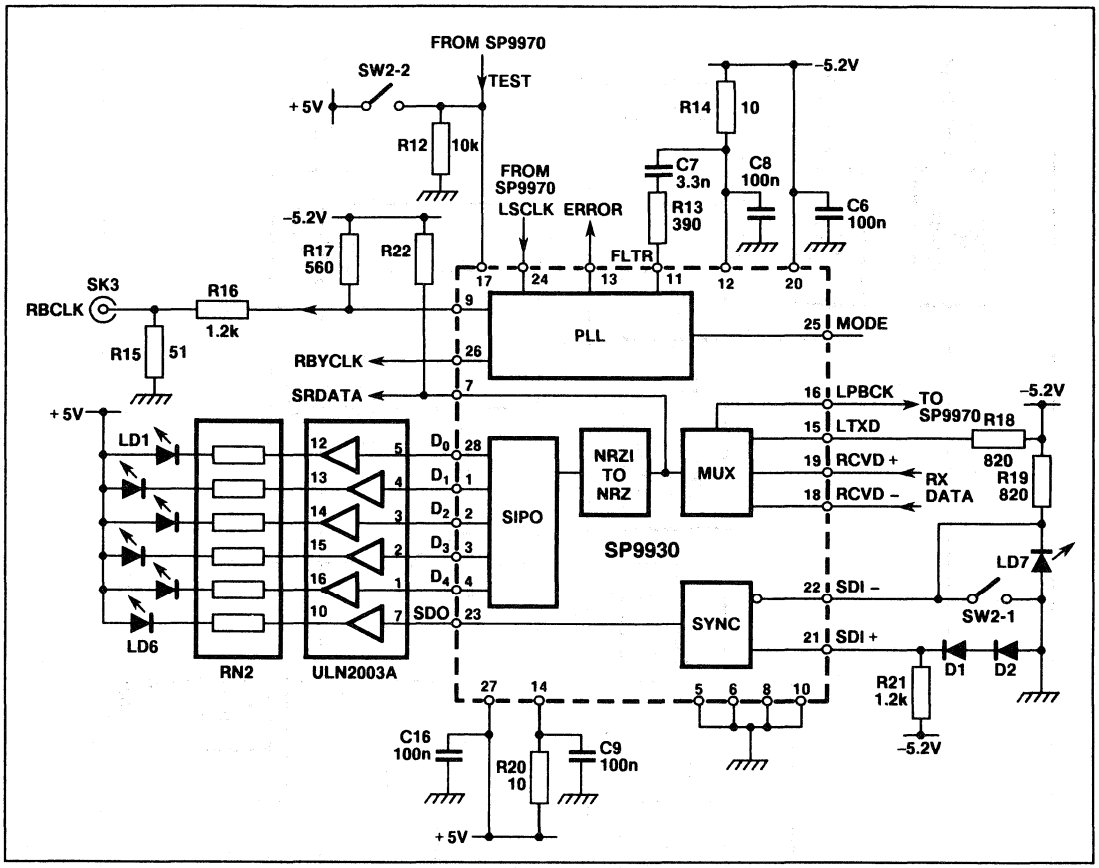



*Fig.4 SP9930 application circuit (see also Application Note AN66, page 4-233)*

Internally the PLL consists of a patented integrate and hold phase comparator driving a charge pump with an internal reservoir capacitor. The reservoir capacitor smoothes the current pulses from the charge pump and provides a relatively noise free voltage to control the VCO. A small resistor in series with the capacitor allows small instantaneous changes in frequency, increasing this resistor improves the capture time but adversely affects the jitter. In practice using the values shown in Fig. 4 will produce a capture time of $< 1\mu s$ and very low jitter.

Fig. 5. shows the VCO frequency against the control voltage at the FLTR pin; the control voltage goes positive for the higher frequencies. As shown by the graph the device has a wide range of operation from 60 to 175MHz. If the device is used at a non FDDI frequency the LSCLK must always be a fifth of the operating frequency ($\pm 0.25\%$), otherwise the frequency comparator will switch into mode 0. The reliability of operation at the frequency extremes is not guaranteed, jitter does increase at the low frequencies but at the higher frequencies it is minimal.

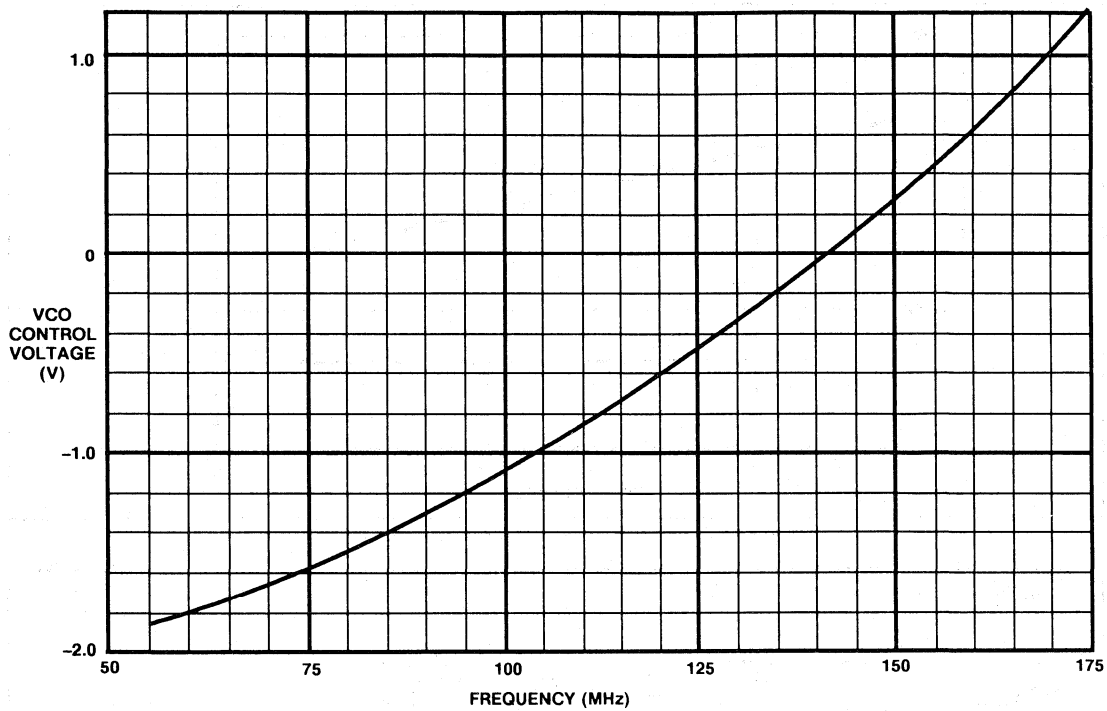



*Fig.5 Receiver VCO characteristic (typical)*

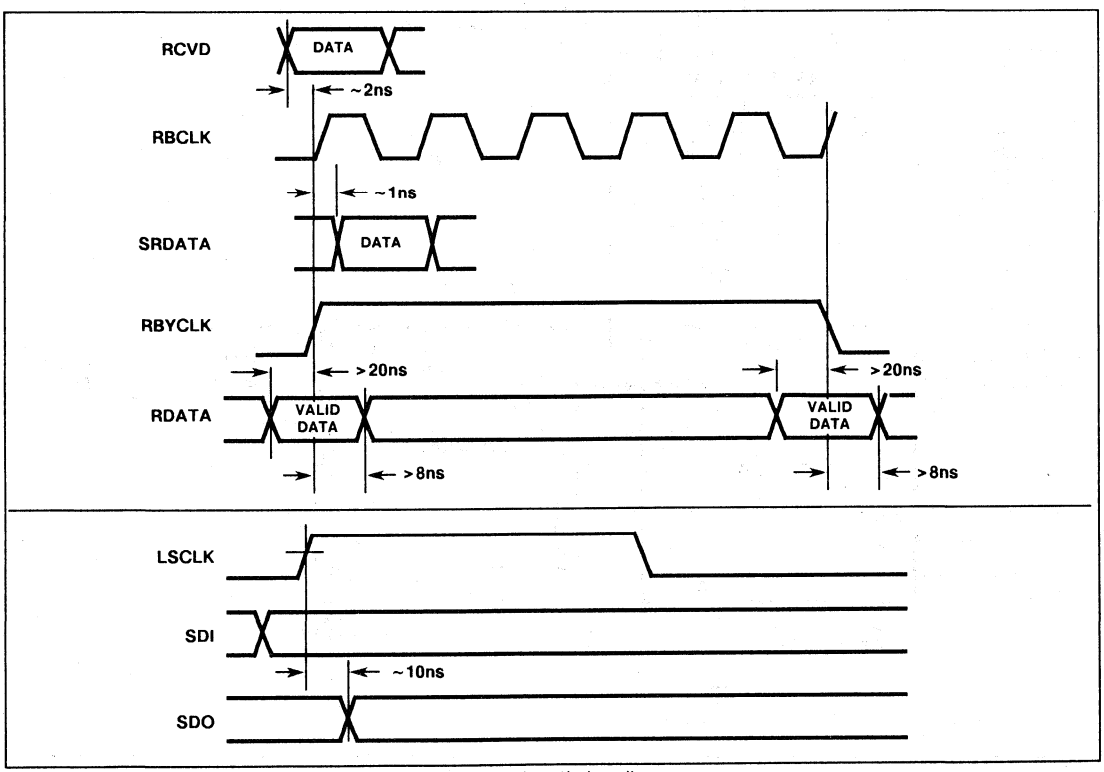



*Fig.6 Receiver timing diagram*

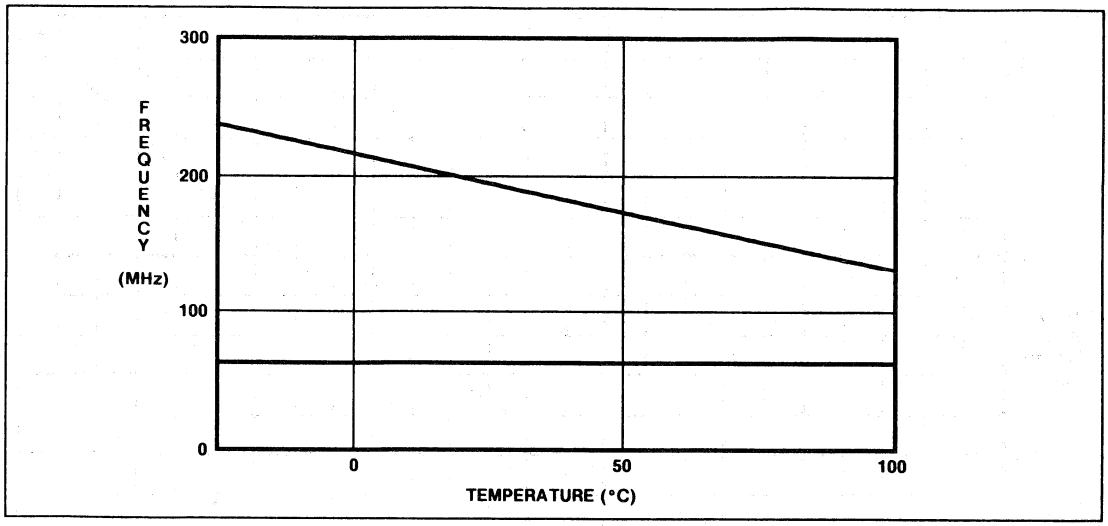



*Fig.7 Operating clock frequency for FDDI receiver*

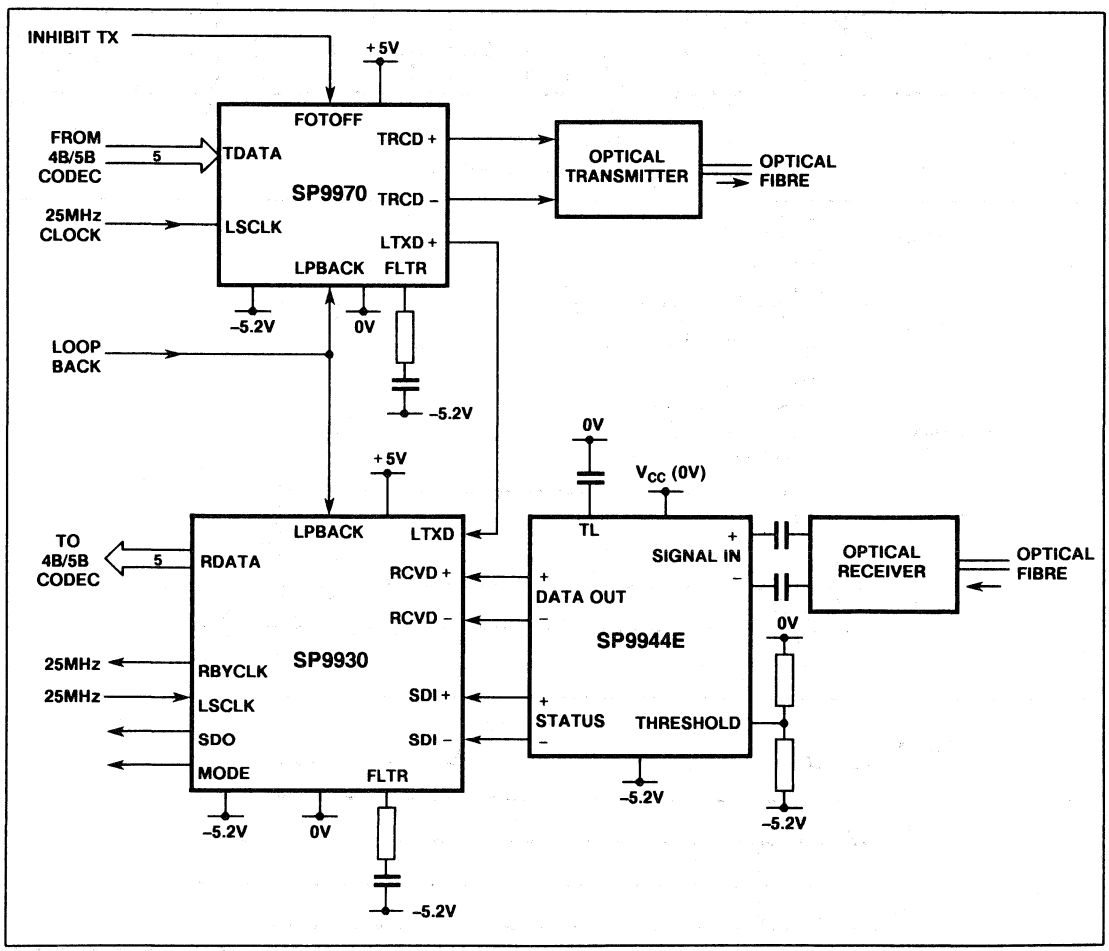


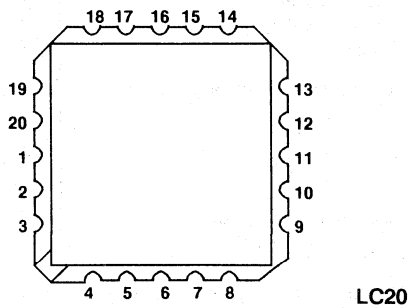

*Fig.8 Typical FDDI application circuit*

# SP9944E

## 200M-BIT/s DATA REGENERATOR

The SP9944E is a data regeneration circuit for use in fibre optic receivers at bit rates up to 220MB/s and can be used with receiver preamplifiers such as PIN-FET modules

Low level differential (or single-ended) input data is converted into ECL levels using high gain, high speed non-satutating limiting amplifiers which incorporate filtering at 125MHz. An internal peak detector and decision circuit is used to provide a STATUS flag when the received signal falls below an externally preset threshold.




| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | $V_{CC}$ | 8 | CAP 2 | 15 | TC |
| 2 | OUT + | 9 | IN + | 16 | $V_{EE}$ |
| 3 | OUT – | 10 | IN – | 17 | $V_{EE}$ |
| 4 | ECL $V_{CC}$ | 11 | $V_{EE}$ | 18 | STAT + |
| 5 | $V_{CC}$ | 12 | TL | 19 | STAT – |
| 6 | $V_{CC}$ | 13 | $V_{CC}$ | 20 | MONOUT |
| 7 | CAP 1 | 14 | EXT REF | | |

*Fig.1 Pin connections - top view*

### FEATURES

- Differential Input / Outputs
- Status Output with Programmable Threshold and Hysteresis
- High Speed (220 MB/s)
- Static Protection
- Gold Backed Die (Naked Die)

### APPLICATIONS

- Fibre Optic Receivers
- LANs (FDDI Compatible)

### ORDERING INFORMATION

**SP9944E C LC** (Commercial - LCC package)
**SP9944E NA 1C** (Naked die)

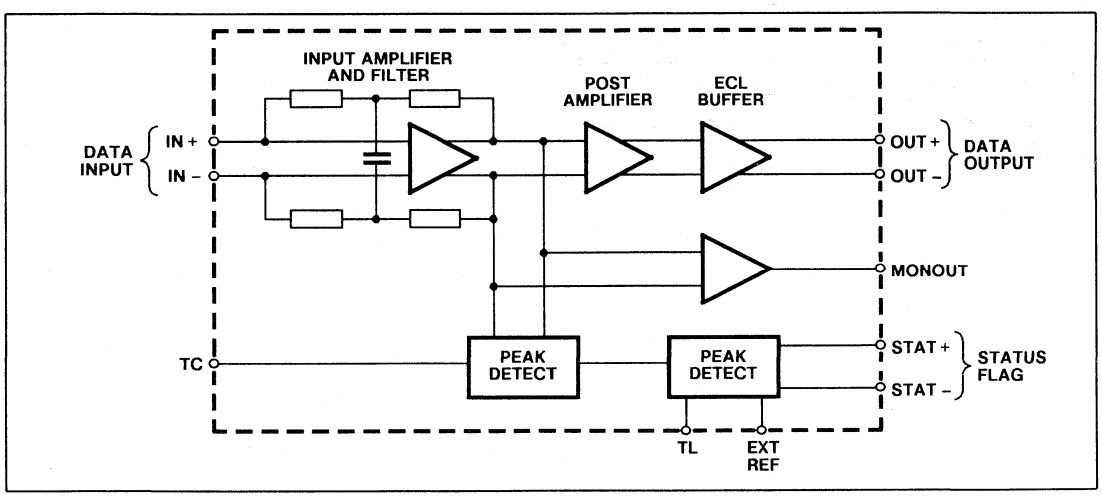



*Fig.2 Functional block diagram*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated):**

$T_{AMB}$ = 0°C to +70°C; $V_{EE}$ = –4.75V to –5.45V; $V_{CC}$ = 0V (ground); input voltage (differential or single-ended) = 1mV to 1000mV p-p; output load (to –2V) = 50Ω (typ.); external reference voltage = –1.2V to –1.4V. Voltages are with respect to $V_{CC}$ (ground). Typical figures are for design aid only: they are not guaranteed and not subject to production testing.

### STATIC CHARACTERISTICS

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply current | $I_{EE}$ | | 80 | 100 | mA | Outputs open circuit |
| IN+ bias voltage | $V_{IB}$ | | – 2.3 | | V | |
| Input impedance: IN+, IN–, TL | $Z_I$ | | 1 | | kΩ | To $V_{EE}$ |
| TC output voltage | $V_{TC}$ | – 0.5 | | – 1.4 | V | Peak detect |
| TL input voltage | $V_{TL}$ | – 0.75 | | – 1.25 | V | Set status threshold |
| Status detection range (note 1) | $V_{IST}$ | 6 | | 50 | mV | P-P differential or single-ended input |
| Status threshold (note 1) | $V_{IST1}$ | | 12 | | mV | $V_{TL}$ = 1.00V p-p, differential or single-ended input |
| ECL output voltage low | $V_{OL}$ | | – 1.8 | | V | |
| ECL output voltage high | $V_{OH}$ | | – 0.9 | | V | |

NOTE

1. $V_{IST1}$ is the switching threshold with no hysteresis. When using a hysteresis setting, the switching points will be equally spaced either side of this threshold point.

### DYNAMIC CHARACTERISTICS

| Characteristic | Symbol | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Output delay | $t_{OD}$ | | 1 | 2 | ns | 50mV p-p input |
| Filter 3dB point | $f_{3dB}$ | | 125 | | MHz | |

## ABSOLUTE MAXIMUM RATINGS

Exceeding these ratings may cause damage. Functional operation under these conditions is not implied.

| | |
|---|---|
| Negative supply voltage, $V_{EE}$ | 0.5 to – 8V |
| Input voltage, $V_I$ | $V_{EE}$ – 0.5V to 0.5V |
| Output voltage, $V_O$ | $V_{EE}$ – 0.5V to 0.5V |
| Output current (source), $I_O$ | 40mA |
| Storage temperature, $T_{ST}$ | – 55°C to + 150°C |
| Junction temperature, $T_J$ | – 55°C to + 175°C |

## FUNCTIONAL DESCRIPTION

The primary function of the SP9944E is amplification and regeneration of the input signal to ECL10KH levels. This is achieved using two high speed, non-saturating limiting amplifiers with a total gain of 75dB and an ECL buffer. The input will accept signals between 1 and 500 mV pk-pk. Filtering is incorporated in the front end amplifier with a 3dB point at 125MHz and a roll-off of 6dB/octave. DC feedback is used to stabilise the bias point of the input amplifier, an external capacitor is used between pins CAP1 and CAP2 to decouple the AC content of this feedback. The inputs must be capacitively coupled; the lower frequency limit is determined by the value of the input impedance and the AC coupling capacitors. The MONOUT pin provides for observation of the input signal at the output of the first amplifier. The gain between MONOUT and the input pins is 32dB.

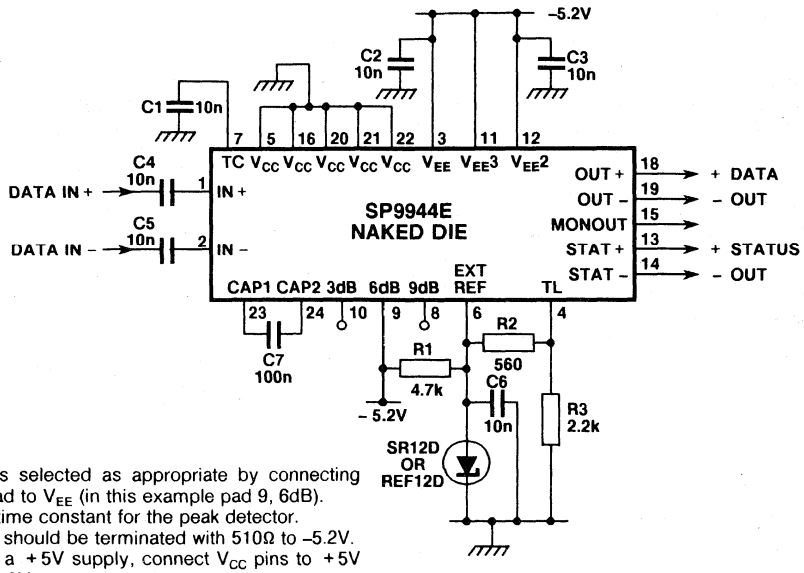
A secondary but very useful facility on the SP9944E are the differential STAT ± (status) outputs. These provide an output flag when the input signal falls below a preset level.

A hysteresis of 3dB, 6dB or 9dB (see note below) can be incorporated on the status flag; it can be user-defined on the naked die variant but is preset to 6dB in manufacture on the packaged device. A peak detector follows the peak amplitude of the input signal, this is fed to a comparator which provides the status output. The time constant of the peak detector is determined by the capacitor connected to the TC pin. Two resistors are used to set the detection threshold anywhere between 1 and 25mV, this can correspond to an optical power level between –32dBm and –41dBm.

NOTE. The electrical hysteresis figures given above should be divided by 2 to obtain the optical hysteresis in dB.

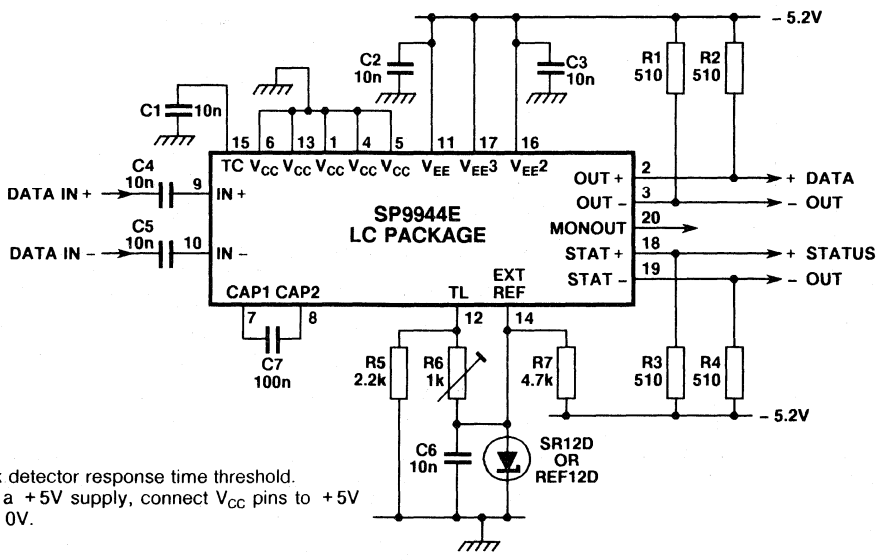
## PIN DESCRIPTION

| Symbol | Pad No | Pin No | Pin Name and Description |
|---|---|---|---|
| IN+<br>IN- | 1,2 | 9,10 | Positive and Negative Differential Data Input. These inputs are self biasing and should be capacitively coupled to the signal source. When using with a single ended source the unused input should be coupled to ground through a 10nF capacitor. |
| $V_{EE}$ | 3,11,12 | 11,16,17 | Negative Supply, connect to -5.2V and decouple to ground with a 10nF capacitor when using a -5.2V. Connect to 0V when using a +5V supply. |
| TL | 4 | 12 | Set Threshold Level for the STATus flag output. This can be set with two resistors: one to $V_{EE}$ and the other to $V_{CC}$. This voltage should be between -0.75V and -1.25V with respect to $V_{CC}$. |
| $V_{CC}$ | 5,16,21,22 | 1,5,6,13 | Positive Supply. Connect to 0V when using a -5.2V supply. Connect to +5V and decouple to ground with a 10nF capacitor when using a +5V supply. |
| TC | 7 | 15 | Time Constant. This sets the response time of the internal peak detector. For most applications a 10nF capacitor to $V_{EE}$ is recommended. |
| 9dB | 8 | - | When connected to $V_{EE}$, the hysteresis of the status detector threshold is 9dB electrical (4.5dB optical). When the signal goes below a preset threshold and the STAT output switches low, it is necessary for the signal to increase by 9dB before the STAT output reverts to the high state. When all hysteresis pads are left open-circuit there is no hysteresis. Available on naked die only. |
| 6dB | 9 | - | As above except hysteresis is set to 6dB (electrical) with this pad at $V_{EE}$. |
| 3dB | 10 | - | As above except hysteresis is set at 3dB (electrical) with this pad at $V_{EE}$. |
| EXT REF | 6 | 14 | An External Voltage Reference (ideally, a bandgap reference) of –1.2V to –1.4V should be connected to this pin. This voltage is used as a reference by the internal comparator.<br>See Application Circuits, Figs. 3 and 4. |
| STAT+<br>STAT- | 13<br>14 | 18<br>19 | Positive and Negative Status flag. This is a differential ECL output. |
| MONOUT | 15 | 20 | This output can be used to monitor the internal signal at the output of the input amplifier (after filtering). A total amplifier gain of 32dB buffers this signal. |
| OUT+<br>OUT- | 18<br>19 | 2<br>3 | Positive and Negative Data Output This is the signal from the IN ± pins regenerated into a differential ECL output. |
| ECL $V_{CC}$ | 20 | 4 | Positive Supply for the ECL output buffers. Connect to 0V when using a -5.2V supply, connect to +5V and decouple to ground with a 10nF capacitor when using +5V supply. |
| CAP1<br>CAP2 | 23<br>24 | 7<br>8 | These connections are used for the DC compensation capacitor which eliminates any DC offset at the input stage. A 100nF capacitor must be connected between these pins. |




NOTES
1. Hysteresis is selected as appropriate by connecting the relevant pad to $V_{EE}$ (in this example pad 9, 6dB).
2. C1 sets the time constant for the peak detector.
3. ECL outputs should be terminated with 510Ω to -5.2V.
4. When using a +5V supply, connect $V_{CC}$ pins to +5V and $V_{EE}$ pins to 0V.
5. R1 and R2 set STATUS to 25mV p-p.

*Fig.3 Typical application circuit (naked die hybrid)*




NOTES
1. C1 sets peak detector response time threshold.
2. When using a +5V supply, connect $V_{CC}$ pins to +5V and $V_{EE}$ pins to 0V.

*Fig.4 Typical application circuit (packaged device)*

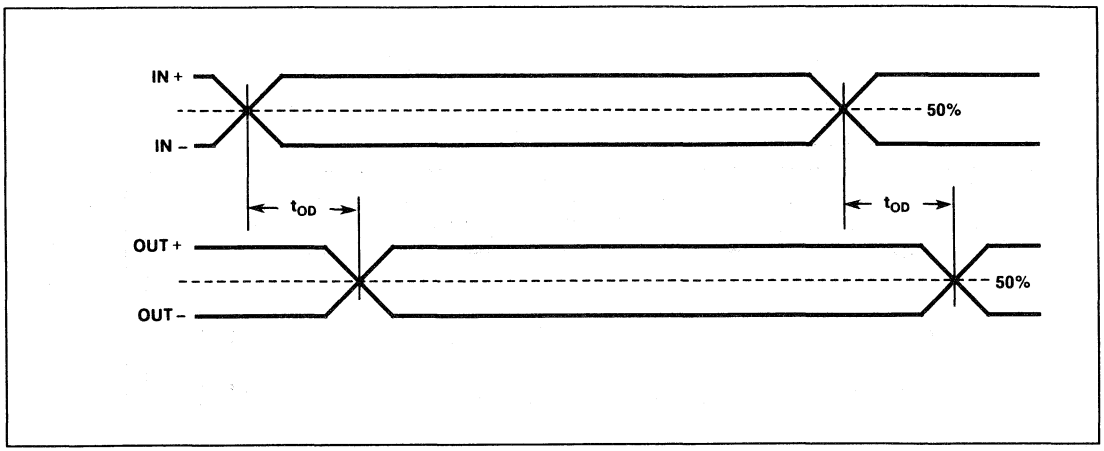



*Fig. 5 Digital switching characteristics*

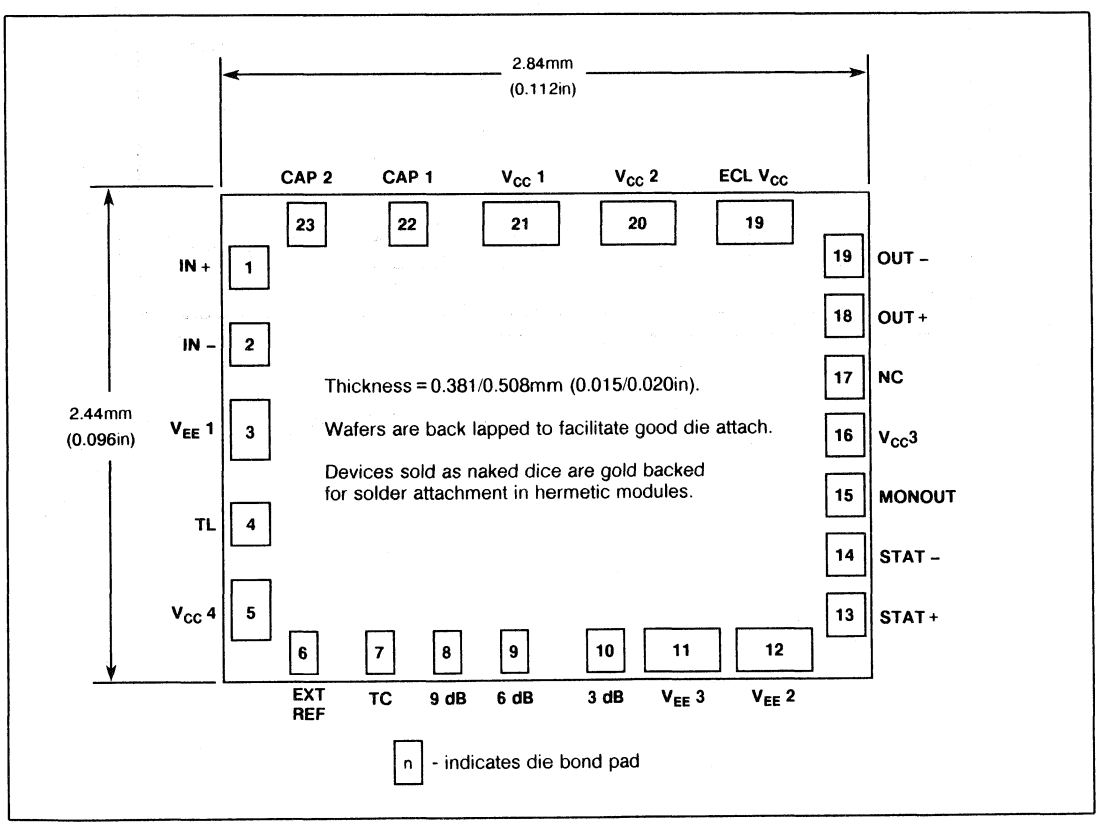



*Fig. 6 Die diagram*

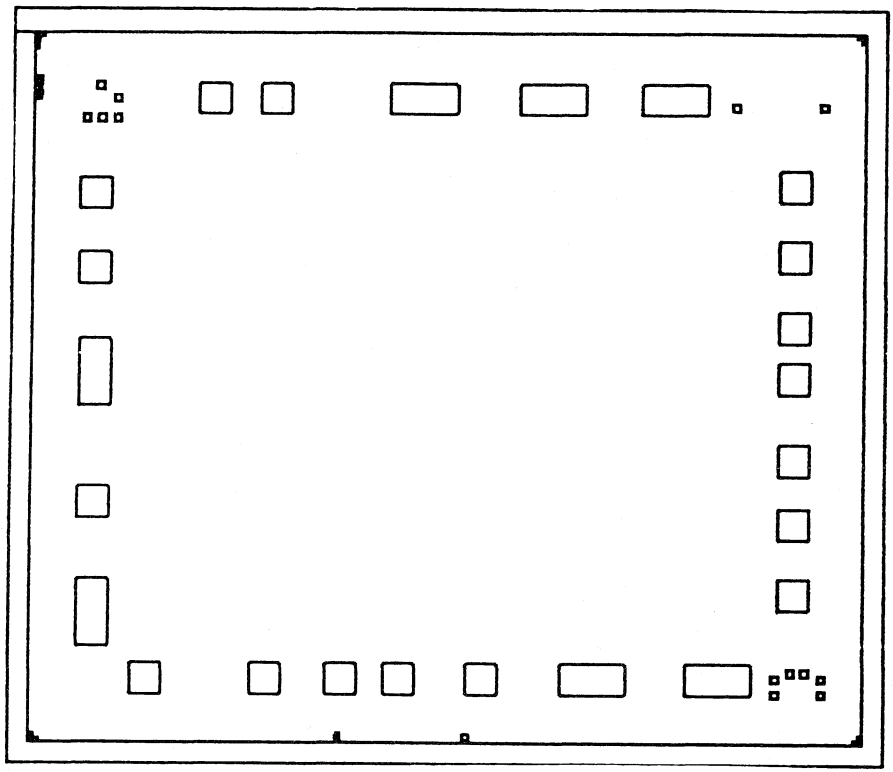


*Fig.7 SP9944E naked die pad map. (Scale: 1mm = 25μm)*

# SP9960

## 50M-BIT MANCHESTER BIPHASE-MARK ENCODER AND LED DRIVER

The SP9960 is a Manchester biphase-mark encoder and LED driver, designed for use in fibre-optic links at up to 50Mbits/s. It encodes TTL or ECL data and outputs the result as a current at either the large or small LED driver output. The LED driver and the current output are selected.

The device is also available as the SP9960AC, which has guaranteed operation over the full Military Temperature Range and is screened to MIL-STD-883 Class B. Data is available separately.

### FEATURES

- -40°C to +85°C Operating Temperature Range
- 50Mbit/s Operation Clock and Data Rates
- TTL or ECL Inputs
- Choice of LED drivers - Large or Small
- Choice of LED Drive Currents
- LED Driver Enable Voltage
- Single Supply Voltage

### APPLICATIONS

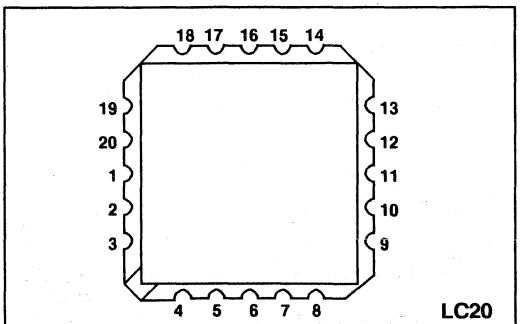
- Fibre Optic Data Link
- Local area Network (LAN) Interface
- Coaxial/Twisted Pair Devices

### ORDERING INFORMATION

**SP9960 B LC** (Industrial - leadless chip carrier)
**SP9960 AC LC** (Military - leadless chip carrier, screened to MIL-STD-883C CLASS B)

### ASSOCIATED PRODUCTS

**SL9901** 50MHz Transimpedance Amplifier
**SP9921** 50M-Bit Manchester Biphase Decoder




| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | NC | 8 | EDI | 15 | LD |
| 2 | $V_{EE}$ | 9 | NC | 16 | NC |
| 3 | $V_{EE}$:10 | 10 | $V_{CC}$ | 17 | $V_{EE}$:80 |
| 4 | TDI | 11 | DL | 18 | $V_{EE}$:45 |
| 5 | TCI | 12 | DL | 19 | $V_{EE}$:LD |
| 6 | NC | 13 | SD | 20 | ODE |
| 7 | ECI | 14 | NC | | |

*Fig.1 Pin connections - Top view*

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage | +7V |
| Input voltage | -3.0V to +0.3V |
| Storage temperature range | -65°C to +175°C |
| Maximum junction temperature | +175°C |

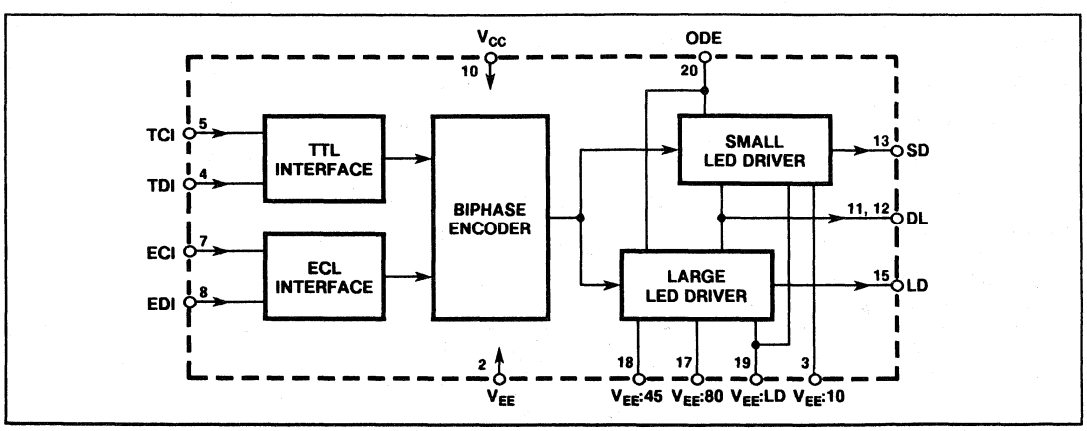



*Fig.2 Functional block diagram*

## ELECTRICAL CHARACTERISTICS (Voltages are with respect to the negative power supply ($V_{EE}$)

**Test conditions (unless otherwise stated)**

Supply voltage $V_{CC}$ = +4.5V to +5.50V, $T_{AMB}$ = -40°C to +85°C (see note 1),
Programming input low voltage $V_{ODEL}$ = 0V to 0.4V; Programming input high voltage $V_{ODEH}$ = 2V to $V_{CC}$; TTL input low voltage $V_{ILT}$ = 0.84V Max; TTL input high voltage $V_{ILT}$ = 2.0V min; ECL input low voltage $V_{ILE}$ = $V_{CC}$ -1.65V max; ECL input high voltage $V_{IHE}$ = $V_{CC}$ -0.96V min. (see note 2).

| Parameter | Symbol | Value | | Units | Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Supply current | $I_{CC}$ | | 70 | mA | Output disabled |
| TTL input current | $I_T$ | | 130 | μA | $V_{IHT} = V_{CC}$ |
| ECL input current | $I_E$ | | 300 | μA | $V_{IHE} = V_{CC}$ |
| Small driver ON current (sink) (note 3) | $I_{SD}$ | 12<br>20 | 18<br>30 | mA<br>mA | $1V < (V_{EE}:10) < V_{CC}$, default.<br>$V_{EE}:10 = V_{EE}$ |
| Large driver ON current (sink) (note 3) | $I_{LD}$ | 35<br>72<br>102<br>140 | 55<br>108<br>148<br>200 | mA<br>mA<br>mA<br>mA | $1V < (V_{EE}:45/80) < V_{CC}$, default.<br>$V_{EE}:45 = V_{EE}$<br>$V_{EE}:80 = V_{EE}$<br>$V_{EE}:45 = V_{EE}$, $V_{EE}:80 = V_{EE}$ |
| Operating clock frequency | $f_C$ | 50 | | MHz | |

NOTES

1 The maximum temperature depends on the selected LED drive current. The limits are found by derating the limit of the chip temperature (given in Absolute Maximum Ratings) by the temperature difference due to the power dissipation and the thermal resistance to case or ambient (given in the Additional Information table).

2. $T_{AMB}$ = +25C.

3. The maximum power dissipation depends on the selected output drive current. It is always less than the product of the supply voltage and the sum of maximum drive current (either $I_{SD}$ or $I_{LD}$) and the maximum current with driver disabled ($I_{CC}$)

## GUARANTEED CHARACTERISTICS

The following characteristics are guaranteed, but not tested, for the SP9960B at +25°C and over the full supply voltage range (+4.50V to +5.50V); refer to Figs. 5 to 7.

| Parameter | Symbol | Value | | Units | Conditions |
|---|---|---|---|---|---|
| | | Min | Max | | |
| Programming input (ODE) current low | $I_{ODEL}$ | | 2.0 | mA | $V_{ODE} = 0V$ |
| Driver OFF leakage (sink) | $I_L$ | | 100 | μA | $0V < V_{ODE} < 0.4V$ |
| Clock high period | $t_{CH}$ | 5 | | ns | |
| Clock low period | $t_{CL}$ | 5 | | ns | |
| Input data setup time | $t_{IS}$ | 5 | | ns | |
| Input data hold time | $t_{IH}$ | 0 | | ns | |
| Output data hold time | $t_{OH}$ | 0 | | ns | |
| Output data delay | $t_{OD}$ | | 30 | ns | |
| Output rise & fall time | $t_{ORF}$ | | 2 | ns | $I_{LED}$ = 80mA, 10Ω to $V_{CC}$ |
| 1st half cycle period | $t1_{CP}$ | $t_{CL-2}$ | | ns | |
| 2nd half cycle period | $t2_{CP}$ | $t_{CL-2}$ | | ns | |

## ADDITIONAL INFORMATION

The following parameters are typical for the SP9960 at +25°C but not tested.

| Characteristic | Symbol | Value | Units | Conditions |
|---|---|---|---|---|
| Thermal resistance, chip-to-case | $\theta_{CC}$ | 28 | °C/W | |
| Thermal resistance, chip-to-ambient | $\theta_{CA}$ | 73 | °C/W | |
| Pin capacitance | $C_P$ | 3 | pF | Pin to supplies |

## FUNCTIONAL DESCRIPTION

Fig. 2 shows the simplified block diagram of the device. Data arriving at a data input (TDI or EDI pin) is sampled by the positive edge of the appropriate clock (TCI or ECI pin), encoded into a biphase-mark signal, and output as a current at the chosen LED driver (SD or LD pin).

If TTL inputs are to be used (TDI and TCI pins) then the ECL inputs (EDI and ECI) should be left unconnected and vice versa.

### Biphase Mark Encoding

Fig. 3 shows how the biphase-mark encoding scheme works. The input data is sampled by the positive edge of the clock. If the data is high (logic '1') then the driver switches to its opposite state i.e., OFF if it was previously ON, or ON if it was previously OFF. If the data is low (logic '0') then the driver does not switch to its opposite state on the positive clock edge.

Regardless of the sampled input data, the driver always switches to its opposite state on the negative edges of the clock.

This form of encoding ensures a high number of transitions in the signal which simplifies the task of clock recovery at a remote detector. Since the data is encoded in terms of transitions, rather than as absolute levels, the signal can be given a net inversion without corrupting the information carried.

### LED Drivers

There are two LED driver outputs, the small driver (SD, pin 13) and the large driver (LD, pin 15). The driver used is chosen by $V_{EE}$:LD (pin 19) which should be tied to $V_{EE}$ (pin 2) to select the large driver and left unconnected to select the small driver., as shown in Table 1.

Typical LED output currents for the small driver are 15mA or 25mA and for the large driver 45mA, 90mA, 125mA or 170mA, determined by the supply connections to the $V_{EE}$:10, $V_{EE}$:45 and $V_{EE}$:80 pins, as shown in Table 1.

When the LED driver is OFF then current is switched to the dummy load pins (DL) which are normally connected to the positive supply. This reduces the ringing which could otherwise occur on switching relatively large currents. The drivers are disabled by pulling the ODE pin low. They are enabled if the ODE pin is left unconnected.

| LED output selectors (ODE = O/C) | | | | LED current (mA typ) | |
|---|---|---|---|---|---|
| $V_{EE}$:LD (19) | $V_{EE}$:10 (3) | $V_{EE}$:45 (18) | $V_{EE}$:80 (17) | SD (13) | LD (15) |
| O/C | O/C | X | X | 15 | – |
| O/C | $V_{EE}$ | X | X | 25 | – |
| $V_{EE}$ | X | O/C | O/C | – | 45 |
| $V_{EE}$ | X | $V_{EE}$ | O/C | – | 90 |
| $V_{EE}$ | X | O/C | $V_{EE}$ | – | 125 |
| $V_{EE}$ | X | $V_{EE}$ | $V_{EE}$ | – | 170 |

*Table 1*

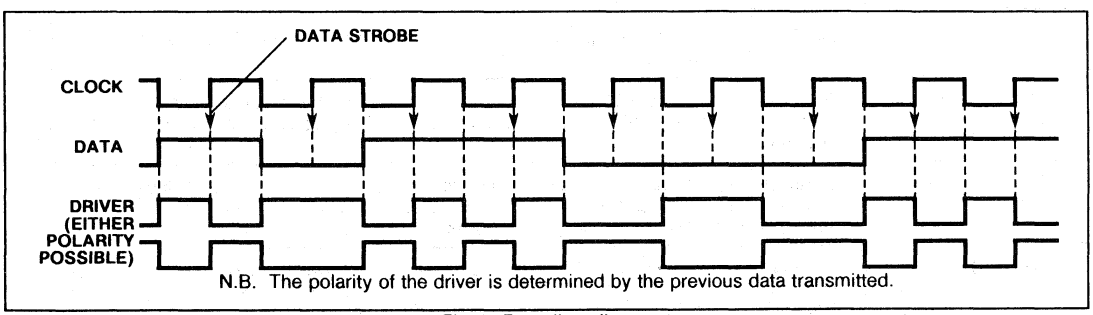



*Fig. 3 Encoding alignment*

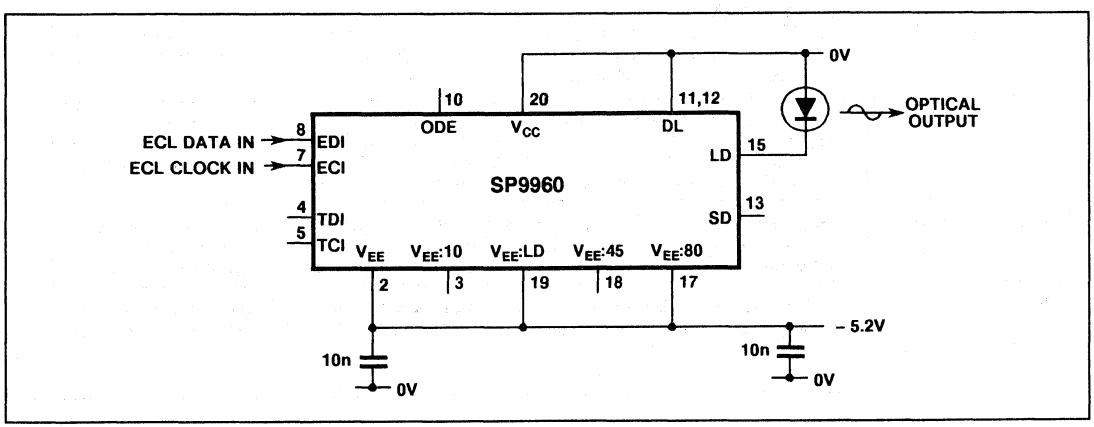



*Fig. 4 Typical ECL application circuit - large driver at 125 mA (typical) selected*

*N.B. For TTL applications the TTL inputs TDI and TCI should be used, VCC should be + 5V and $V_{EE}$ should be 0V.*

## PIN DESCRIPTIONS

| Symbol | LCC Pin No | Pin Name and Description |
|---|---|---|
| $V_{EE}$ | 2 | **Negative Supply (Power Input).** This pin is normally tied to 0V for TTL operation or to -5.2 V for ECL operation. |
| $V_{EE}$: 10 | 3 | **10mA Negative Supply (Power Input).** This pin should be tied to the negative supply (VEE) to increase the current sink at the small current LED output driver (SD pin) by 10mA if the small driver is selected. It should be left unconnected otherwise. |
| TDI | 4 | **TTL Data Input (TTL Input with Internal Pull-Down).** TTL data is strobed in at this pin by the positive edges of the TTL Clock input (TCI pin). This pin should be left unconnected if the TTL inputs are not to be used. See notes given in this table on $V_{CC}$ and $V_{EE}$. |
| TCI | 5 | **TTL Clock Input (TTL Input with Internal Pull-Down).** The rising edges of this clock is used to strobe the TTL data input (TTI pin). This pin should be left unconnected if the TTL inputs are not to be used. See notes on $V_{CC}$ and $V_{EE}$. |
| ECI | 7 | **ECL Clock Input (ECL Input with Internal Pull-down).** The rising edge of this clock is used to strrobe the ECL data input (EDI pin). This pin should be left unconnected if the ECL inputs are not to be used. See notes on $V_{CC}$ and $V_{EE}$. |
| EDI | 8 | **ECL Data Input (ECL Input with Internal Pull-down).** ECL data is strobed in at this pin by the positive edges of the EC clock input (ECL pin). This should be left unconnected if the ECL inputs are not to be used. See notes given in this table on $V_{CC}$ and $V_{EE}$. |
| $V_{CC}$ | 10 | **Positive Supply (Power Input).** This pin is normally tied to 5V for TTL operation or to 0 V for ECL operation. |
| DL | 11,12 | **Dummy Load (Current Sink Output).** Current is switched between these pins and the selected LED drivers (SD or LD) to reduce ringing. They should be connected to the positive supply ($V_{CC}$). |
| SD | 13 | **Small Driver (Current Sink Output).** This is the small current LED output driver. Data supplied at the clock and data pins is encoded and output as a current at this pin if the large driver negative supply pin ($V_{EE}$:LD) is left unconnected. |
| LD | 15 | **Large Driver (Current Sink Output).** This is the large current LED output driver. Data supplied at the clock and data pins is encoded and output as a current at this pin if the latge driver negative supply pin ($V_{EE}$:LD) is tied to the negative supply ($V_{EE}$). |
| $V_{EE}$: 80 | 17 | **80mA Negative Supply (Power Input).** This pin may be used in conjunction with the $V_{EE}$:45 pin. It should be tied to the negative supply ($V_{EE}$) to increase the current sink at the large current LED output driver (LD pin) by 80mA (typically) if the large driver is selected. It should be left unconnected otherwise. |
| $V_{EE}$: 45 | 18 | **45mA Negative Supply (Power Input).** This pin may be used in conjunction with the $V_{EE}$:80 pin. It should be tied to the negative supply ($V_{EE}$) to increase the current sink at the large current LED output driver (LD pin) by 45mA (typically) if the large driver is selected. It should be left unconnected otherwise. |
| $V_{EE}$: LD | 19 | **Large Driver Negative Supply (Power Input).** This pin should be tied to the negative supply ($V_{EE}$) if the large current LED output driver (LD pin) is to be used. It should be left unconnected if the small current LED output driver (SD pin) is to be used. |
| ODE | 20 | **Output Driver Enable (Programming Input with Internal Pull-up).** This pin should be left unconnected for normal operation. If it is low then the LED output driver is disabled. |

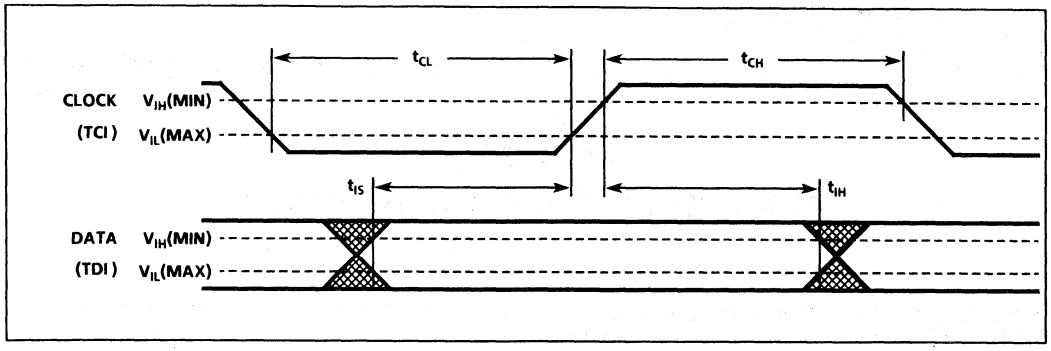



*Fig. 5 Digital Switching Characteristics - TTL Input*

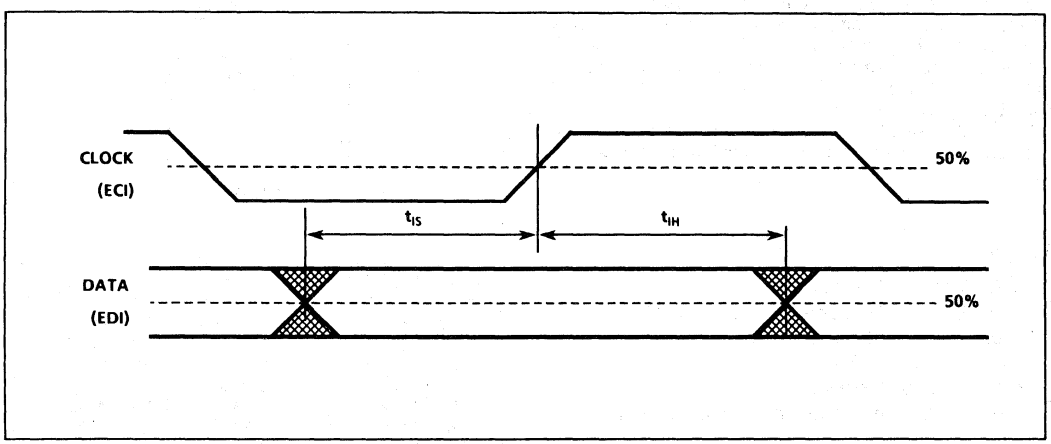



*Fig. 6 Digital Switching Characteristics - ECL Input*

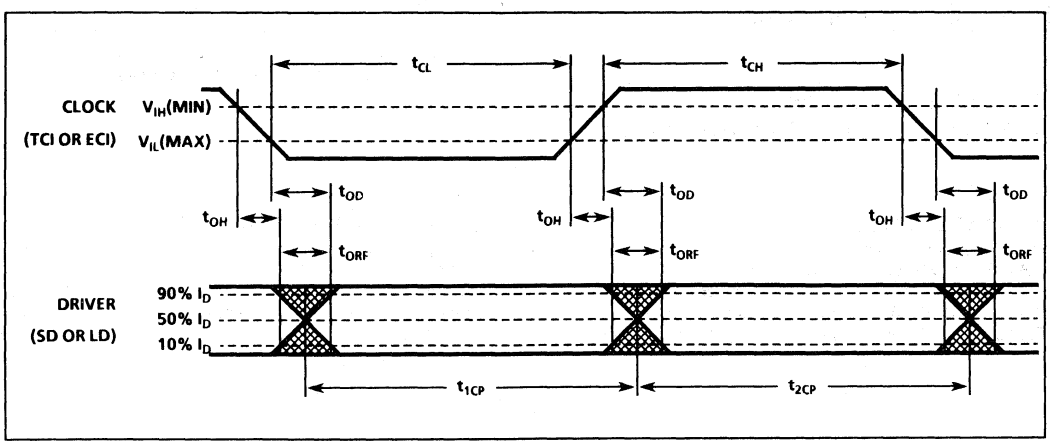



*Fig. 7 Digital Switching Characteristics - Output*

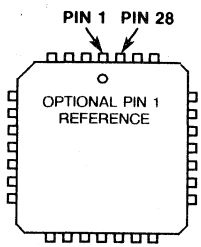
# SP9970

## FDDI PARALLEL TO SERIAL LINE DRIVER

FDDI (Fibre Distributed Data Interface) is a standard defined by ANSI (American National Standard Institute) for a token passing ring network operating at a user rate of 100MB/s. The SP9930 receiver is one of two devices which service the 4B/5B codec to NRZI interface.

Only two external components are required to provide RC phase lock loop filtering. An on-chip PLL is used to multiply the local symbol clock by 5. This provides a transmit bit clock of 125MHz and a differential ECL O/P allows the signal to be monitored.

A parallel to serial converter changes the I/P data into a serial data stream of 125MB/s before it is encoded as NRZI.




HG28

| Pin | Function | Pin | Function | Pin | Function |
|---|---|---|---|---|---|
| 1 | NC | 11 | TRCD – | 21 | $DV_{CC}$ |
| 2 | TBCLK + | 12 | NC | 22 | LSCLK |
| 3 | TBCLK – | 13 | LTXD + | 23 | FOTOFF |
| 4 | NC | 14 | LTXD – | 24 | $DV_{EE}$ |
| 5 | AGND | 15 | LPBCK | 25 | $AV_{EE}$ |
| 6 | DGND | 16 | TDATA $D_4$ | 26 | FLTR |
| 7 | EGND | 17 | TDATA $D_3$ | 27 | $AV_{CC}$ |
| 8 | NC | 18 | TDATA $D_2$ | 28 | TEST |
| 9 | TRCD + | 19 | TDATA $D_1$ | | |
| 10 | NC | 20 | TDATA $D_0$ | | |

*Fig.1 Pin connections - top view*

### FEATURES

- FDDI Standard Compatible
- 125MHz Clock Guaranteed (Typ. 170MHz at 25°C)
- Receive Bit Clock Jitter <2.3ns
- Lock on time <1.0μs
- +5.0V/ –5.2V Supplies
- Very Low External Component Requirement

### APPLICATIONS

- FDDI Communication System

### ORDERING INFORMATION

**SP9970 C HG** (Commercial - Quad Cerpac package)

### ASSOCIATED PRODUCTS

**SP9930** FDDI Receiver
**SP9944E** 200MBit/s data regenerator
**SL9901** 50MHz transimpedance amplifier
**SP9921** 50MBit/s Manchester biphase-mark Decoder
**SP9960** 50MBit/s Manchester biphase-mark Encoder

### ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Supply voltage $V_{CC}$ | +5.5V |
| Supply voltage $V_{EE}$ | -5.75V |
| Operating temperature | 0°C to +70°C |
| Maximum junction temperature | +125°C |
| Storage temperature | -55°C to +150°C |

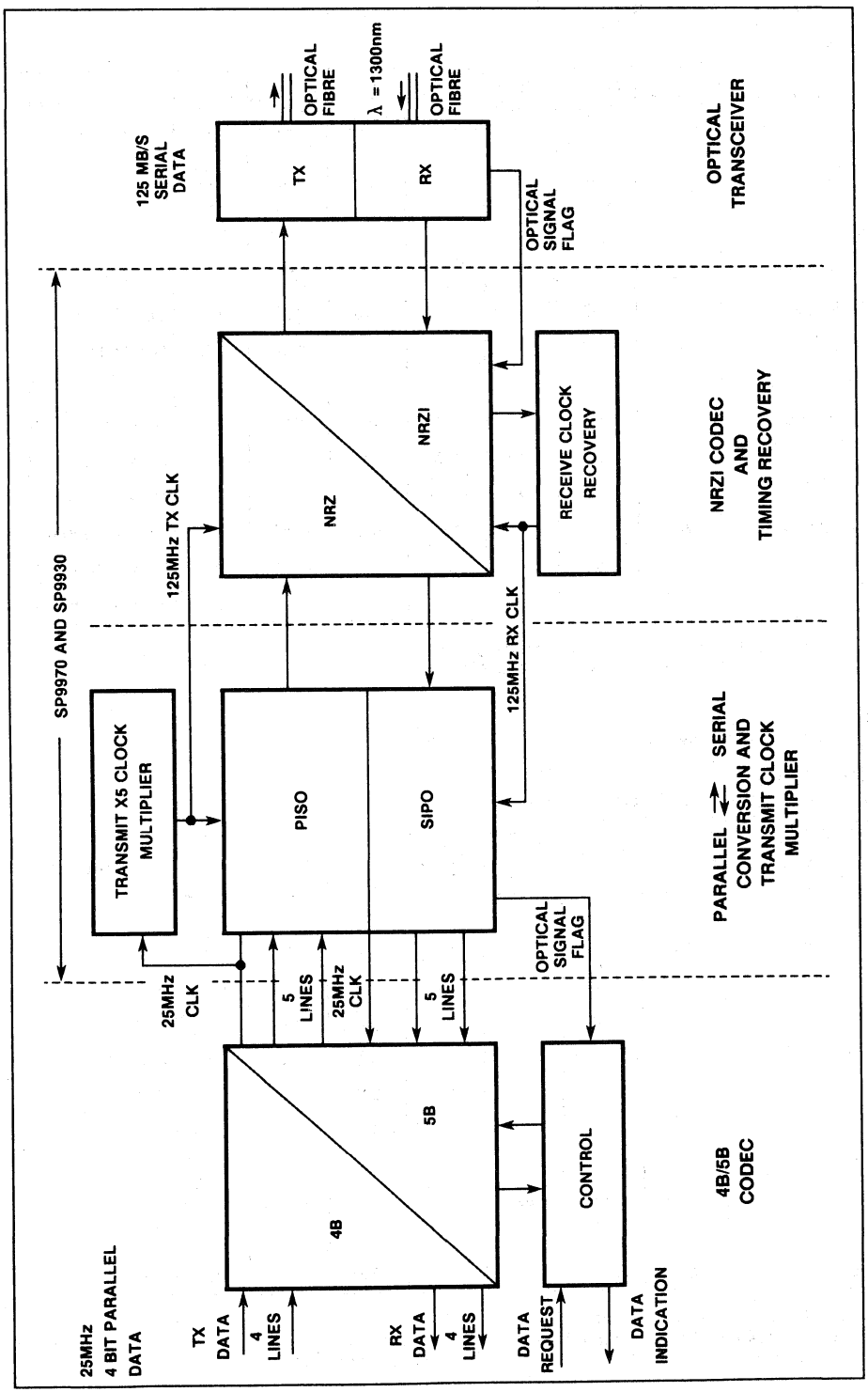



*Fig.2 FDDI physical layer (block diagram)*

## ELECTRICAL CHARACTERISTICS

**Test conditions (unless otherwise stated)**
$T_{amb}$ = 25°C, $V_{CC}$ = +5V ±10%, $V_{EE}$ = -5.25V ±10%
Full temperature range = 0°C to +70°C

**DC CHARACTERISTICS**

| Characteristic | Symbol | Temp. (°C) | Test level | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| **Power Supply** | | | | | | | | |
| Supply current | $I_{CC}$ | Full | 1 | | 13 | 20 | mA | |
| | $I_{EE}$ | Full | 1 | | 70 | 150 | mA | |
| **TTL Inputs** | | | | | | | | |
| Logic '1' current | $I_{IH}$ | Full | 1 | | 4 | 20 | µA | See Note 1 |
| Logic TEST pin | | Full | 1 | | 110 | 130 | µA | See Note 1 |
| Logic '0' current | $I_{IL}$ | Full | 1 | | | -600 | µA | See Note 1 |
| **ECL OUTPUTS** | | | | | | | | |
| Logic '1' voltage | $V_{OH}$ | 0 | 4 | -1.02 | -0.9 | -0.84 | V | RL = 100Ω to -2V |
| | | 25 | 1 | -1.00 | -0.85 | -0.8 | V | RL = 100Ω to -2V |
| | | 70 | 4 | -1.92 | -0.8 | -0.72 | V | RL = 100Ω to -2V |
| Logic '0' voltage | $V_{OL}$ | 0 | 4 | -1.95 | -1.7 | -1.63 | V | RL = 100Ω to -2V |
| | | 25 | 1 | -1.95 | -1.7 | -1.63 | V | RL = 100Ω to -2V |
| | | 70 | 4 | -1.95 | -1.7 | -1.6 | V | RL = 100Ω to -2V |

NOTES
1. TTL input under test set to 2V all other TTL inputs set to 0.8V
2. TTL input under test set to 0.8V all other TTL inputs set to 2V

**TEST LEVELS**
Level 1 - 100% production tested
Level 4 - Parameter guaranteed by design and characteristics testing

**AC CHARACTERISTICS**
Guaranteed by design and AC characteristics testing.
Characteristics assume 125Mbit operation

| Characteristic | Symbol | Temp. (°C) | Value | | | Units | Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| **ECL Outputs** | | | | | | | |
| Rise times 20%-80% | $T_R$ | 0 | | 1.0 | 2.5 | ns | RL = 100Ω to -2V |
| | | 25 | | 1.5 | 3.0 | ns | RL = 100Ω to -2V |
| | | 70 | | 2.5 | 5.0 | ns | RL = 100Ω to -2V |
| Fall times 20%-80% | $T_F$ | 0 | | 1.0 | 2.5 | ns | RL = 100Ω to -2V |
| | | 25 | | 1.5 | 3.0 | ns | RL = 100Ω to -2V |
| | | 70 | | 2.5 | 5.0 | ns | RL = 100Ω to -2V |
| **TCR Outputs** | | | | | | | |
| Duty cycle distortion | DCD | Full | -0.8 | 0.3 | +0.8 | ns | |
| **TBCLK** | | | | | | | |
| Jitter p-p | $t_{CJ}$ | Full | 0 | 0.2 | 0.5 | ns | LSCLK to RBCLK |

**ELECTRICAL CHARACTERISTICS DEFINITIONS**
**Duty cycle distortion (DCD):** The maximum difference between the high time of this signal and the low time.
**Jitter ($t_{CJ}$):** The maximum deviation of the rising edge of LSCLK to the rising edge of RBCLK.

| CONTROL INPUTS (TTL) | | | FUNCTION | DATA OUTPUTS (ECL) | | | |
|---|---|---|---|---|---|---|---|
| | | | | TRCD | | LTXD | |
| FOTOFF | LPBCK | TEST | | + | − | + | − |
| 1 | 1 | 0 | Normal operation | Coded data | | Lo | Hi |
| 0 | 1 | 0 | Fibre optic transmit disabled | Lo | Hi | As above | |
| 1 | 0 | 0 | Loopback mode | Coded data | | Coded data | |
| 0 | 0 | 0 | Loopback mode | Lo | Hi | Coded data | |
| X | X | 1 | Test mode for manufacturer's use only | X | | X | |

*Table 1 Transmitter function*

## INTRODUCTION TO FDDI SYSTEMS

FDDI (Fibre Distributed Data Interface) is a standard defined by ANSI (American National Standard Institute) for a token passing ring network operating at a user rate of 100MB/s. The standard consists of 4 documents;

1. Physical Media Dependant (PMD)
2. Physical Layer Protocol (PHY)
3. Media Access Control (MAC)
4. Station Management (SMT)

These documents correspond closely with the OSI seven layer model, PMD and PHY are sublayers of the OSI physical layer. The MAC document implements some of the OSI Data link layer. Overall control of the PHY and MAC functions is provided by the SMT.

### Technical Overview (The Physical Layer)

Fig. 2 shows a block diagram of the Physical Layer, the first section is the 4B/5B codec, here the data is in symbols, four bits wide at a rate of 25MB/S. Each four bit code received, is converted into a 5 bit code according to a pre-defined table. This extra bit is added to prevent long runs of zeros, it also allows the addition of signalling words by the control section. A circuit incorporating the codec function is not yet available but it could be implemented in semi-custom CMOS, such as CLA60K series.

After conversion to a 5-bit word the data undergoes a parallel to serial conversion, this multiplies the transmission rate up to 125MB/s. In order to clock the data out at this rate the clock needs to be multiplied five times up to 125MHz, this is achieved with a phase locked loop in this chip set. Before transmission over the fibre the data is converted to a code called NRZI, in this code a '1' is represented by a transition and '0' as no transition. This coding maximises transistions without increasing the bandwidth of the signals, and when combined with the 4B/5B coding this system minimises the DC content of the signal. On the receive side the transitions within the NRZI code are used to recover the 125MHz clock.

FDDI specifies a fibre optic transmission medium of 62.5 μm core multimode fibre (this is the recommended core size; 50, 85 and 100μm cored fibres are allowed alternatives), a 1300nm LED source, and a maximum distance between nodes of 2km.

Up to 500 nodes and a total fibre length of 200km are supported by FDDI. A distance of up to 2km is supported by the present multimode interface, and work is in progress to modify the standard to allow a single mode interface for larger distances.

A further modified network called FDDI-II is proposed that uses 6MB/s time slots for isochronous data such as voice, low rate video and point to point data links. FDDI-II uses the same physical layer as FDDI-I.

## THE FDDI CHIPS

At present FDDI chips are available which support the 4B/5B to NRZI interface, this circuitry is contained in two 28 pin packages, a transmitter chip and a receiver chip Both chips operate on a supply of +5V/-5.2V. TTL and differential ECL interfaces are used for the 25MB/s and 125MB/s signals respectively, all control and alarm signals are TTL levels.

The ECL interfaces are 10KH compatible. Although the devices are designed to operate at a line rate of 125MB/s, performance up to 170MB/s can be expected at 25°C. Both transmitter and receiver have a loopback mode, serial data from the local transmitter is looped back to the local receiver. The devices are manufactured using a high speed bipolar process.

### The SP9970 Transmitter

The SP9970 transmitter is the simpler of the two devices and takes a supply of approximately 30mA and 80 mA on the +5V and -5.2V supplies respectively. Only two external components are required: a capacitor and resistor which provide the phase lock loop filter. Fig. 3 shows the block diagram of the transmitter.

An on-chip phase locked loop consisting of a phase frequency comparator, charge pump and a VCO is used to multiply the local symbol clock (LSCLK) by five. This provides a transmit bit clock (TBCLK) of 125MHz and a differential ECL output allows monitoring of this signal.

A parallel-to-serial converter changes the input data into a serial data stream of 125MB/s. No framing signal is added, as the 4B/5B code is constructed such that the bit sequence can be recovered in the 5B/4B decoder in the receiver. Immediately after conversion to serial form the data is encoded as NRZI (Non Return to Zero Invert on Ones), i.e., a transition occurs if the input is at a logic '1' but no change if it is at a logic '0'. Use of this code minimises the DC component and therefore allows the signal to be AC coupled as is common practice on high rate fibre optic receivers. With the 4B/5B code no more than nine zeros occur and this only in the 'Master Line' state. TDATA 4 is transmitted first and TDATA 0 last.

Differential ECL output buffers are provided for the Transmit coded data (TRCD) and loopback transmit data (LTXD); these minimise noise and DC level problems. When the FOTOFF control signal is at a logic '0' the TRRD buffer is forced to a known state (see Table 1). This control signal is normally used to switch off the optical transmitter. The NRZI data is also connected to the loopback buffer output (LTXD), which is enabled when LPBACK is at a logic '0'. If disabled the LTXD output is forced to a known state. (see Table 1).

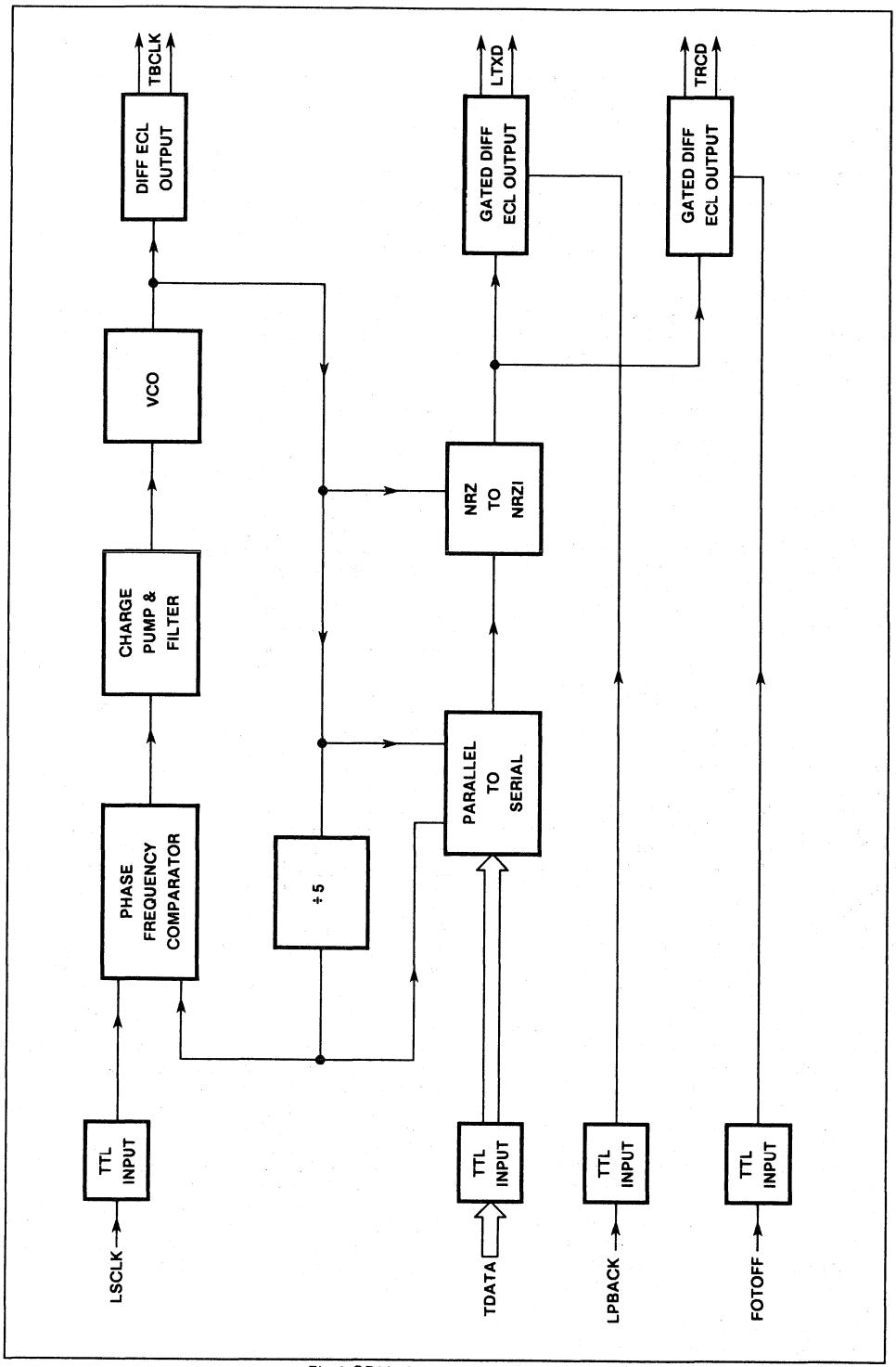



*Fig.3 SP9970 transmitter block diagram*

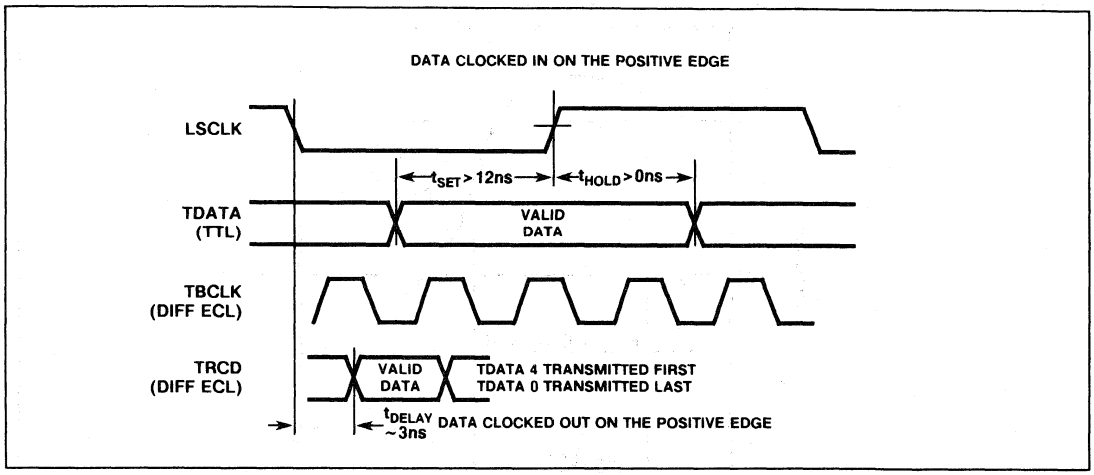



*Fig.4 Transmitter timing diagram*

**Transmitter Phased Locked Loop Characteristics**

The transmitter PLL uses the 25MHz LSCLK as the reference and provides a 125MHz TBCLK locked to five times this reference. Although not normally used, the TBCLK is provided as a differential O/P. Internally, the PLL comprises a phase frequency comparator, a charge pump and a VCO. (see Fig. 3). The phase frequency comparator outputs correction pulses which are converted to current pulses by the charge pump. These current pulses are used to charge an internal reservoir capacitor through a resistor, and allows small instantaneous changes inthe VCO frequency, aiding the capture time and improving supply noise rejection. Fig. 4 shows the alignment of the TBCLK with the LSCLK. Refer to Fig. 7 for the recommended PLL filter components. Fig. 5 shows the VCO frequency against the control voltage on the FLTR pin and shows that the device has a reasonably linear characteristic. Typically, the device will operate between 50 and 170MHz and can therefore be used for applications other than FDDI, Jitter is likely to increase at the extremes of operating frequency.

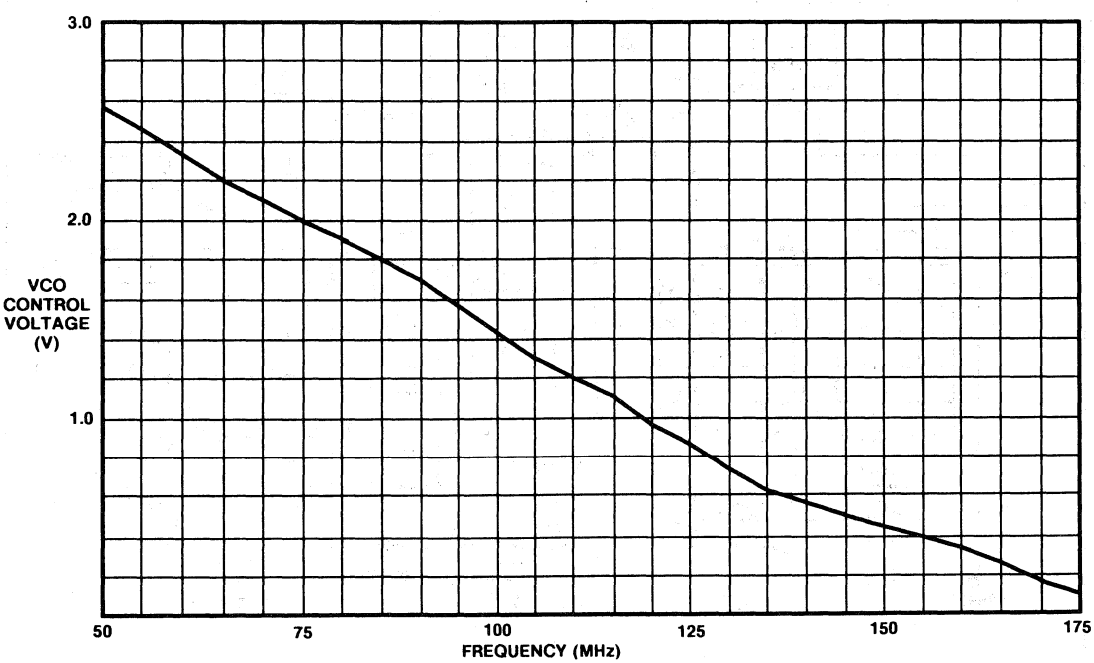



*Fig.5 Transmitter VCO characteristic (typical)*

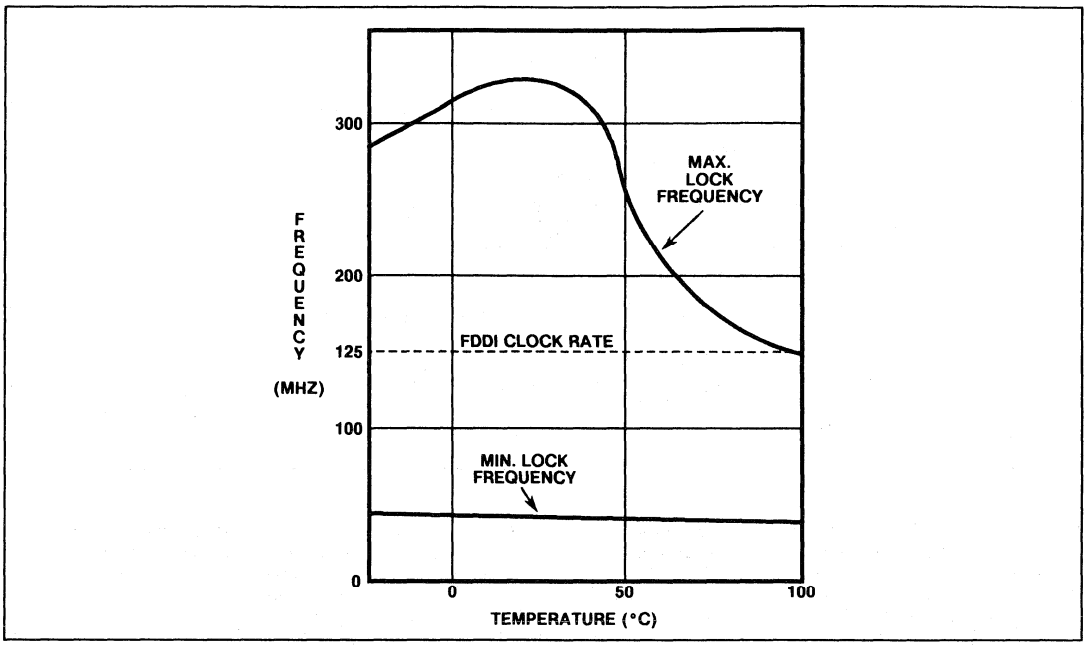



*Fig. 6 Operating clock frequency range for FDDI transmitter*

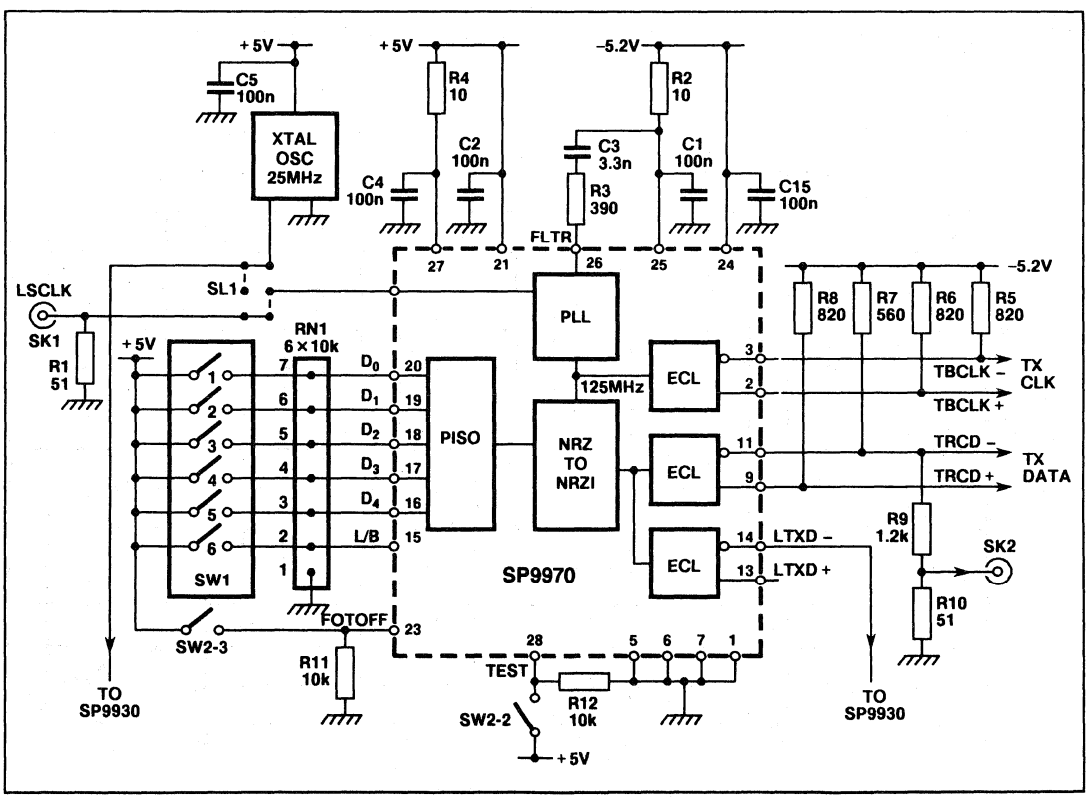



*Fig.7 SP9970 application circuit (see also Application Note AN66, page 4-233)*

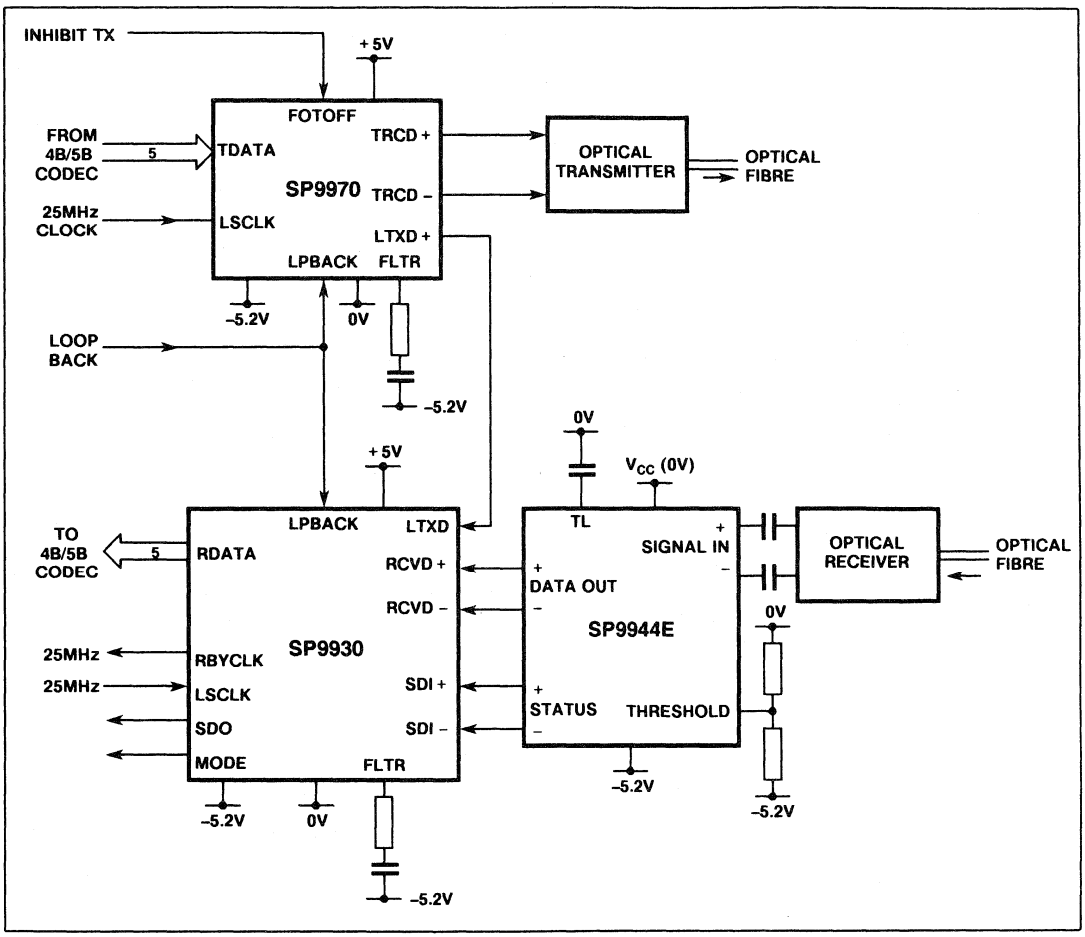



*Fig.8 Typical FDDI application circuit*

# Section 4

## Application Notes

# Digital to Analog Converters

**1. A digital to analog converter (DAC) is a device which converts a digital data input into a corresponding analog output. This output usually takes the form of a voltage or current.**

## 1.1 Ideal output characteristics

If a unipolar voltage output and normal binary coding are assumed, then the ideal transfer function of a linear DAC may be written as:

$V_{out} = V_{FS} \ (B_1.2^{-1} + B_2.2^{-2} + B_3.2^{-3} + ..... + B_n.2^{-n})$

where $B_1$ is the most significant bit input (MSB) and $B_n$ is the least significant bit input (LSB). Bits 1 to n can each assume a value of '1' or '0'. The number of bit inputs a DAC possesses is known as the **resolution** of the converter.

The smallest increment of output voltage is that contributed by the LSB and is equal to $V_{FS}.2^{-n}$.

The terms 'MSB', 'LSB' etc., are frequently used interchangeably to describe either the digital input or the corresponding analogue output.

The maximum output from a DAC is known as full-scale output ($V_{FSO}$).

It occurs when all inputs are '1' and is equal to $V_{FS}\left(\frac{(2^n - 1)}{2^n}\right)$. For example the maximum output of a 3-bit DAC is $\frac{7}{8}\ V_{FS}$.

The transfer function graph of an ideal 3-bit DAC is shown in Fig. 1. For each of the 8 input codes there exists a discrete analogue output level,

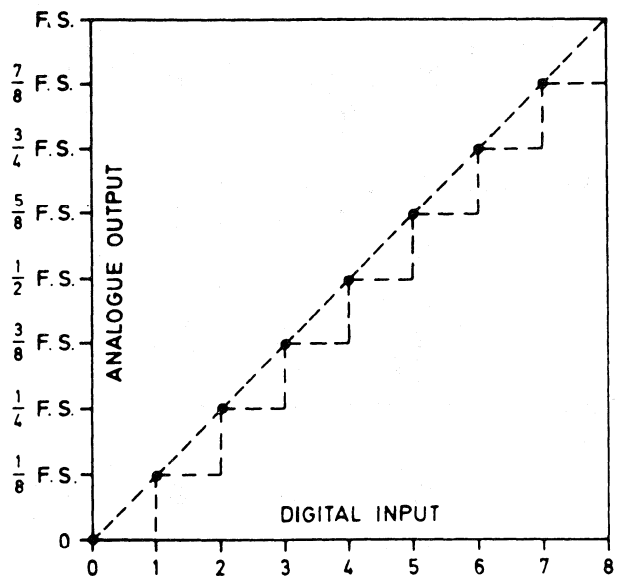



**Fig. 1 Transfer characteristics of ideal 3-bit DAC**

represented by a point on the graph. It should be emphasised that the transfer characteristic is not a continuous function and it is, therefore, not strictly correct to join the points with a continuous line, since this would imply that non-integral input codes and corresponding levels existed. However, a straight line is often drawn between zero and full-scale to represent the 'ideal' transfer function on which all the points should lie.

Similarly, if the input code of a DAC is incremented using, say a binary counter and clock generator, then the analogue output will be a staircase waveform. DAC transfer functions are frequently drawn as a staircase, since this is a convenient way of illustrating various errors that may occur in a DAC. However, such a graph is, strictly speaking, a plot of analogue output v time rather than output v input code.

## 1.2 Practical DAC circuits

Fig.2 shows an example of a 3-bit DAC circuit based on a voltage-switching R-2R ladder network, a technique widely used in Plessey converters.

Each 2R element is connected either to 0V or $V_{FS}$ ($V_{REF}$) by transistor switches. Binary weighted voltages are produced at the output of the R-2R ladder, the value being proportional to the digital input number.

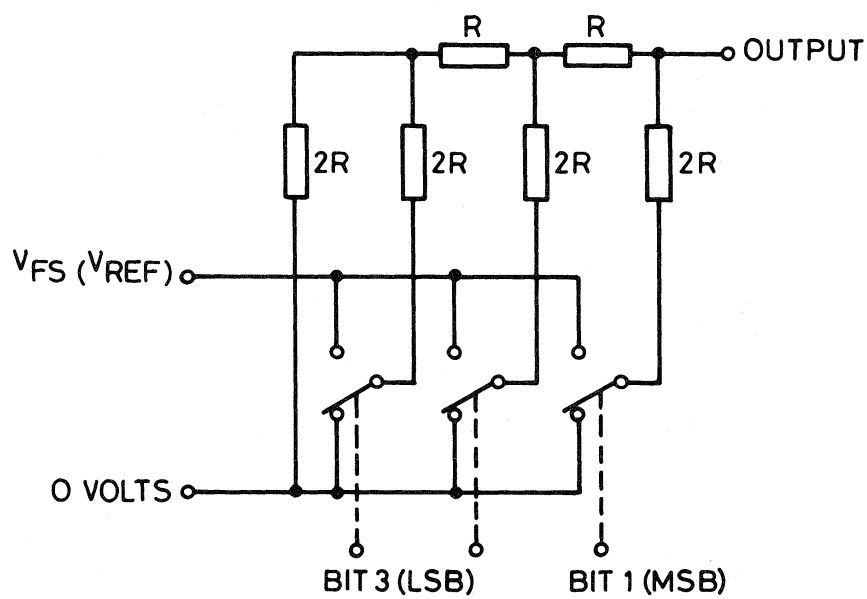



**Fig. 2 3-bit voltage switching DAC**

For example, it is fairly easy to see that if bit 1 is '1' and bit 2 and 3 are '0' then an output of $V_{FS}/2$ is produced. This is because the resistance of the ladder looking from the output through the first R is 2R, which forms a 2:1 attenuator with the 2R in series with the MSB switch. Output voltages for other input codes can similarly by calculated, and it can be seen that the ladder may be extended to any number of bits.

## 1.3 D-A parameters and definitions

### 1.3.1 Converter errors

The ideal DAC assumes that all the resistors are perfectly matched and that the switches have zero resistance. In a practical converter this will not be the case and various errors will occur in the output.

### 1.3.2 Monotonicity

When the input code of a DAC is increased in 1 LSB steps the analogue output of the DAC should also increase, staircase fashion. If the output always increases in this manner then the DAC is said to be monotonic, i.e. the output is a single-valued function of the input. If, due to errors in the bit weighting, the output of the DAC decreases at any step, as shown in Fig. 3, then the DAC is said to be non-monotonic.

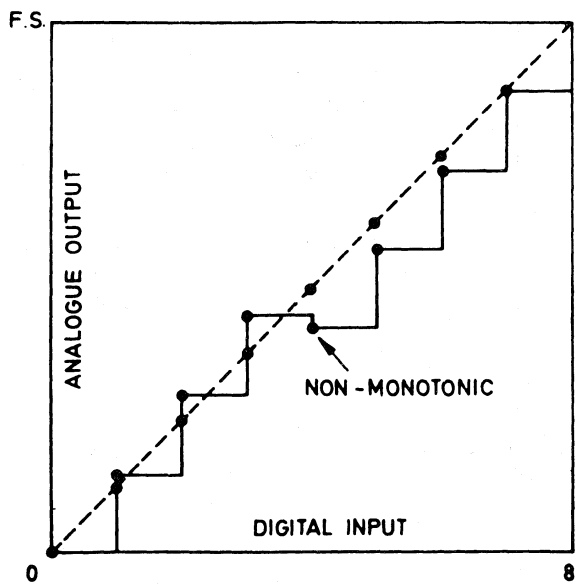



Fig. 3 Non-monotonic DAC

### 1.3.3 Offset (zero error)

Assuming unipolar operation and normal binary coding, when the input code is zero then the DAC outputs should also be zero. However, due to package lead resistances and offset voltages in the switches this will not be the case, and a small output offset may exist. This has the effect of shifting the transfer function so that it no longer passes through zero, as shown in Fig. 4.

### 1.3.4 Gain error

If the reference voltage of a DAC is exactly the nominal value then the transfer characteristics of the converter should follow the ideal straight line. However, due to imperfections in the converter the transfer function may diverge from this line, as shown in Fig. 4. This error is known as gain error and is the difference between the slope of the actual transfer characteristic and the slope of the ideal transfer characteristic.

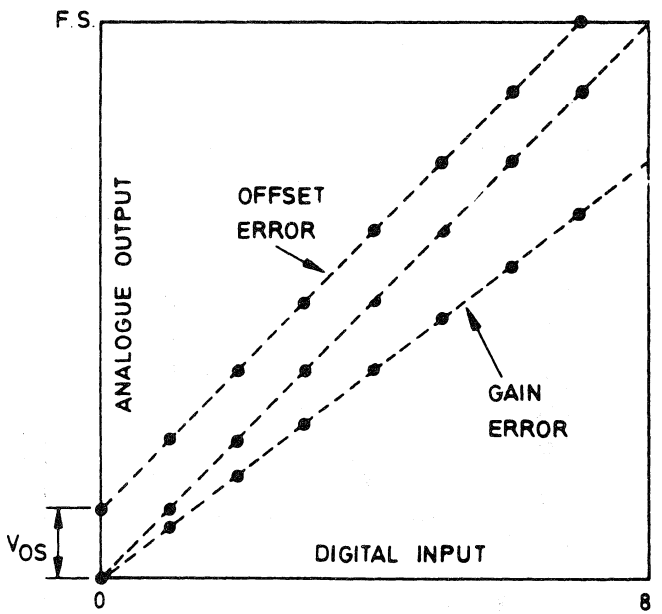



**Fig. 4 Illustrating offset and gain errors**

### 1.3.5 Linearity errors

Offset and gain errors may be trimmed out so that the end points of the transfer characteristics lie at zero and $V_{FSO}$. However, even when this has been done, some or all of the intermediate points may not lie on the 'ideal' line. These errors, which cannot be trimmed out, are known as linearity errors.

### 1.3.8 Resolution

As stated earlier, the resolution of a DAC is simply the number of bit inputs that a DAC possesses, which indicates the smallest analogue increment that the converter can produce as a fraction of $V_{FS}$. e.g. 8 bits = 1 part in $2^8$(256). Resolution implies nothing about the accuracy of a DAC, which is defined by linearity and other errors.

### 1.3.9 Useful resolution

If an n bit DAC has a differential non-linearity of say −1.5LSB then it is non-monotonic. However, if the LSB input is made permanently '0' then the DAC becomes an n − 1 bit device with an LSB equal to twice the original LSB. The differential non-linearity error thus becomes −0.75(new)LSB and the device is monotonic at a resolution of n − 1 bits. This is illustrated in Fig. 6, which shows the transfer characteristic of a 3-bit DAC that has a useful resolution of 2 bits.

Due to manufacturing tolerances a proportion of n-bit converters will have only n - 1 or n - 2 bit useful resolution. In applications not requiring n - bit useful resolution these reduced resoution versions offer a significant price advantage. The useful resolution of Plessey DACs is guaranteed over their full operating temperature range.

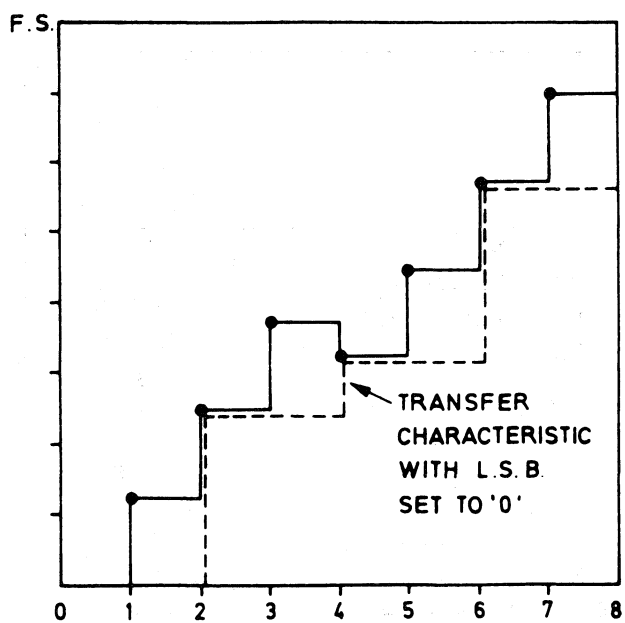



**Fig. 6 Non-monotonic 3-bit DAC with a useful resolution of 2 bits**

### 1.3.6 Non-linearity (linearity error)

This is the maximum amount, given either as a percentage of full-scale or a fraction of an LSB, by which any point on the transfer characteristic deviates from the ideal straight line passing through zero and $V_{FSO}$. Non-linearity is illustrated in Fig. 5. A linearity error within the range $\pm$ ½LSB assures monotonic operation. Note however that the converse is not true and a DAC may still be monotonic with large linearity errors, which is also shown by Fig. 5.

### 1.3.7 Differential non-linearity

This is the maximum difference, specified as a fraction of an LSB, between the actual and ideal size of any one LSB analogue increment. This can be seen as an error in the step height of a DAC staircase. A positive value of differential non-linearity means that the step height is larger than nominal, whilst a negative value means that it is smaller than nominal. If it is more negative than −1LSB then the DAC is non-monotonic. However, positive differential non-linearity may assume any value and a DAC can still be monotonic, as shown in Fig. 5.

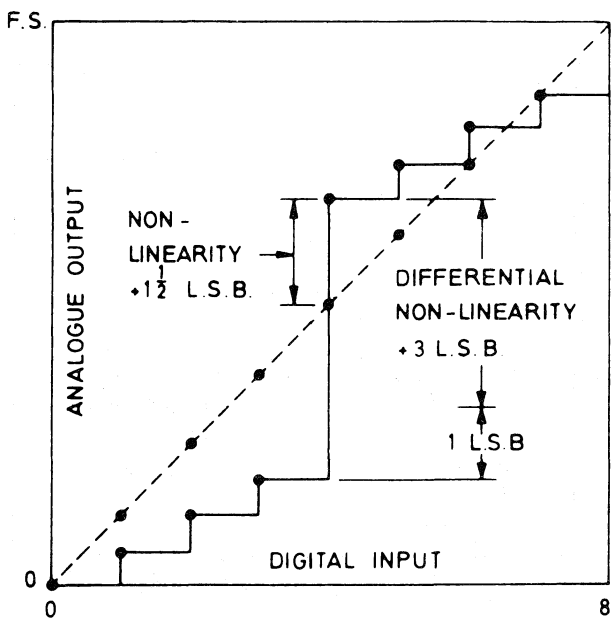



**Fig. 5 Illustrating linearity errors**

### 1.3.10 Settling time

Settling time is the time taken after a transition of the input code for the output of a DAC to settle to within ± ½LSB of its final value. This varies depending on which bits are being changed. It may be specified for a change of 1LSB which generally gives the most optimistic (fastest) figure. More conservative figures are given by the most major transition (where the MSB changes in one direction and all other bits change in the opposite direction, e.g. 01111111 to 10000000 or vice versa) or by a change from all bits off to all bits on (00000000 to 11111111) or vice versa.

## 1.4 Bipolar operation

The discussion so far has been concerned only with DACs producing a single polarity (usually positive) output voltage. In some applications a bipolar (both positive and negative) output range may be required.

This can be achieved by adding a negative offset of $\frac{V_{REF}}{2}$ to the analogue output, as shown in Fig. 7. For all input codes where the MSB is '0' the output voltage is then negative, and for output codes where the MSB is '1' the output voltage is positive. Where the input coding is normally binary but the output voltage is offset by $\frac{-V_{REF}}{2}$ then the input code is referred to as offset binary.

The transfer function of a 3-bit DAC with offset binary coding is shown in Fig. 8.

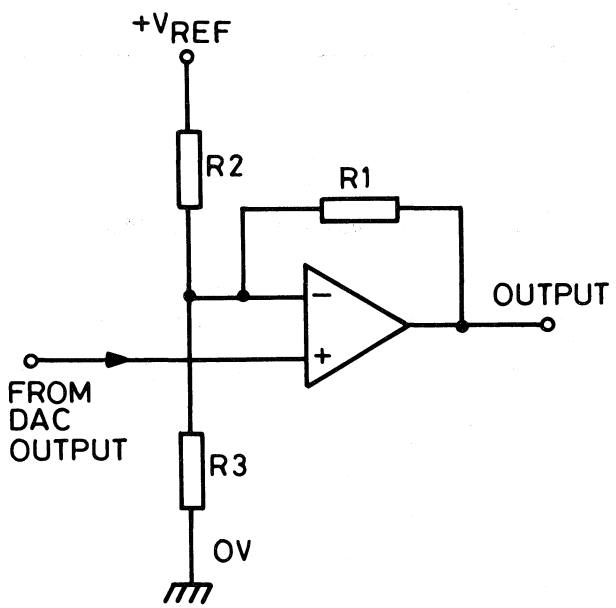



**Fig. 7 Bipolar operation of a DAC**

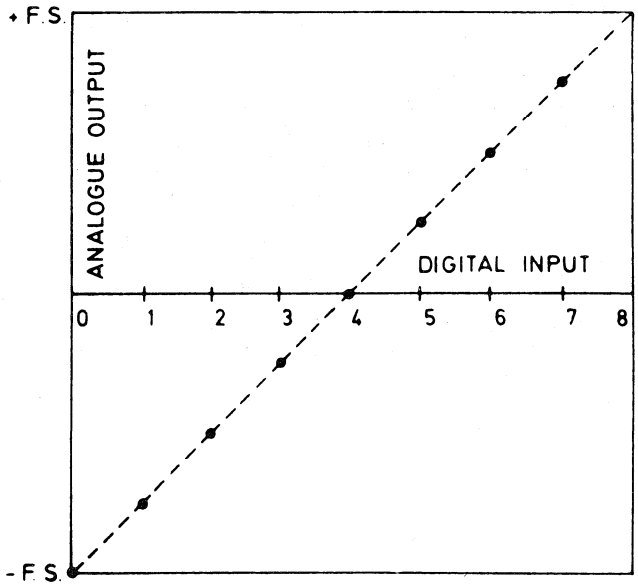



Fig. 8 Bipolar operation of a 3-bit DAC

# Analog to Digital Converters

**2. An analogue to digital converter (ADC) is a device which converts an analogue input into a corresponding digital output code.**

## 2.1 Ideal output characteristics

Assuming a unipolar input voltage and binary coded output the transfer function of an ideal n-bit ADC is given by:

$$V_{FS}\ (B_1.2^{-1} + B_2.2^{-2} + .... + B_n.2^{-n}) = V_{in} \pm \tfrac{1}{2}LSB.$$

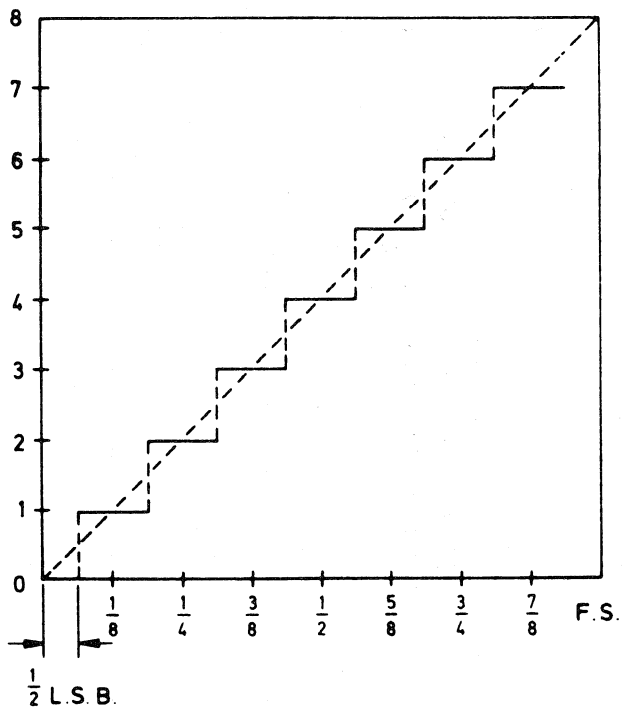



**Fig. 9 Ideal 3-bit ADC transfer characteristic**

The transfer function of an ideal 3-bit ADC is shown in Fig. 9. In this case there are 8 digital output codes corresponding to the 8 input codes of a DAC. However, unlike the analogue output of a DAC, the analogue input of an ADC can vary continuously, which means that each digital output code, with the exception of 0 and 7, exists over an analogue increment of 1LSB. The zero of an ADC is usually trimmed so that the transitions between codes occur $\pm \tfrac{1}{2}$LSB on either side of the nominal analogue input for a particular code. For example, the nominal input for output code 2 is ¼ $V_{FS}$. The transition from 1 to 2 occurs at $\frac{3}{16}$ $V_{FS}$ and the transition from 2 to 3 occurs at $\frac{5}{16}$ $V_{FS}$.

As with a DAC, an 'ideal' straight line may be drawn through the transfer characteristic of an ADC.

## 2.2 Practical A-D conversion methods

There are many methods of performing an analogue to digital conversion; all of these methods are used in the current range of A-D converters.

### 2.2.1 Parallel (flash) conversion

In an n-bit parallel converter (Fig. 10) a resistor ladder is used to generate $2^n - 1$ voltage levels from 1LSB to $(2^n - 1) \times$ LSB which are fed to the reference inputs of $2^n - 1$ voltage comparators. The analogue input signal is fed to the second input of each comparator, and is thus compared simultaneously with each of the $2^n - 1$ voltage levels. At the point in the comparator chain where the reference voltage exceeds the input voltage the comparator outputs will change over from low to high. The comparator outputs are encoded into whatever digital output coding is required.

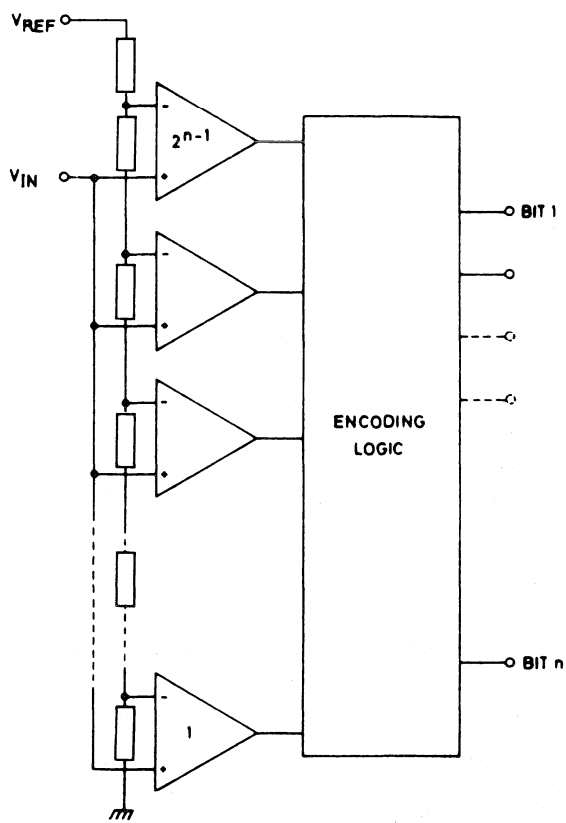



Fig. 10 Parallel A-D converter

Since the only delays involved in the conversion are the propagation delay of one comparator plus the logic propagation delays, parallel converters are very fast and may perform in excess of 10 million conversions per second. However, due to the large number of comparators required (63 for a 6-bit converter, 255 for an 8-bit converter) they are expensive to produce. Applications include digital video systems, digital storage oscilloscopes and radar data processing.

### 2.2.2 Staircase and comparator

In this type of ADC the input code of a DAC is incremented by a binary counter to give a staircase waveform, as shown in Fig. 11. This is compared with the analogue input and when the staircase exceeds the analogue voltage the comparator output changes state and stops the clock. The count reached by the binary counter is thus the ADC output code. This method of A-D conversion is relatively simple and cheap, but is also relatively slow, requiring $2^n - 1$ clock pulses for a full-scale conversion, where n is the number of bits. This conversion method is used in the ZN425 series of dual-purpose D-A/A-D converters.

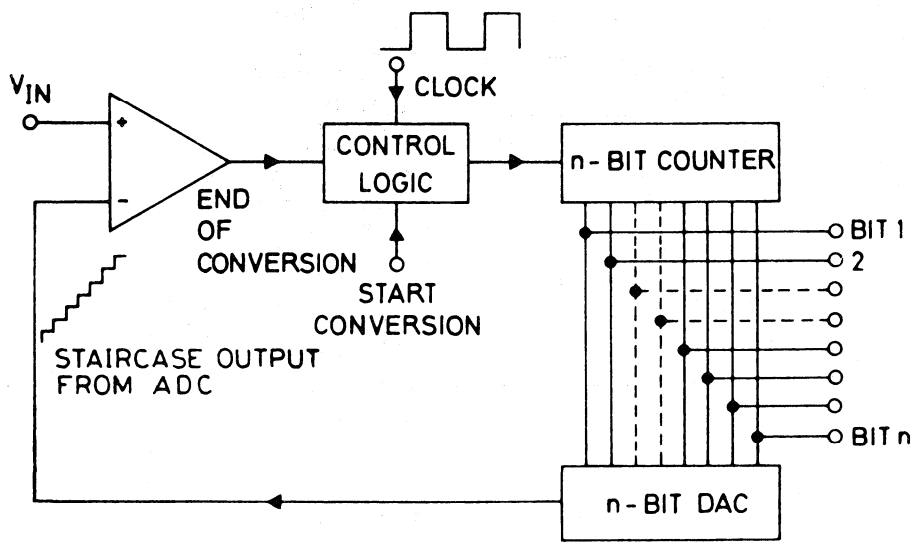



**Fig. 11 Staircase (ramp) and compare ADC**

### 2.2.3 Tracking converters

As its name implies, a tracking converter can follow changing analogue inputs. The principle operation is similar to that of the staircase and compare type of converter, but it uses an up/down counter and a window comparator, as shown in Fig. 12. When the DAC output is less than the analogue input the comparator instructs the counter to count up and the DAC output thus increases. If the DAC output is greater than the analogue input the comparator causes the counter to count down, thus decreasing the DAC output. When the DAC output is equal to the analogue input $\pm$ ½LSB, the input is within the 'window' of the comparator and the counter is stopped. This is illustrated in Fig. 13. A tracking converter has speed advantages over a staircase and compare type, since the counter of the latter type can only count up, and must therefore be reset between conversions. In the case of a tracking converter, once it has performed an initial conversion starting from zero, any subsequent conversions require only that number of clock pulses necessary to track any increase or decrease in input voltage.

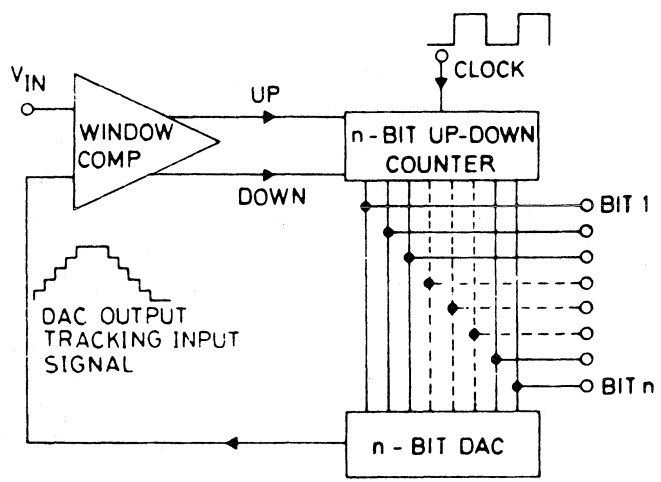



**Fig. 12 Tracking ADC**

As an extreme example consider an analogue input that changes from $V_{FSO}$ to ($V_{FSO}$ – 1LSB). The staircase and compare converter will require $2^n - 1$ clock pulses for the first conversion and $2^n - 2$ clock pulses for the second conversion. The tracking converter on the other hand, will require $2^n - 1$ clock pulses for the first conversion but only one clock pulse for the second conversion. This is illustrated in Fig. 14.

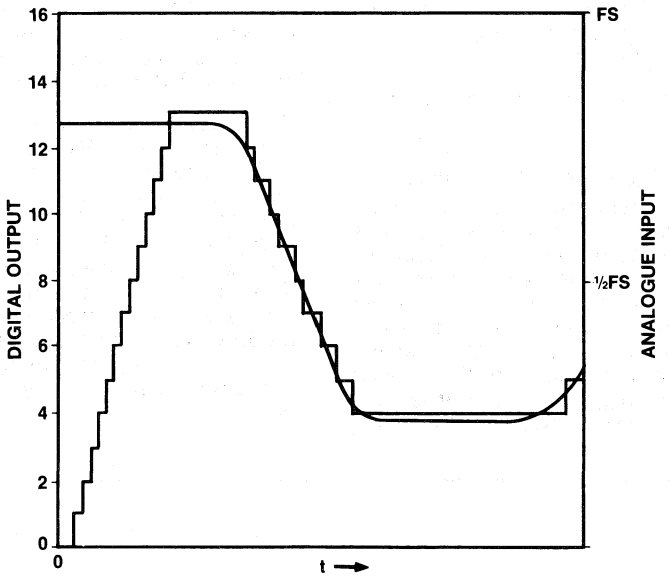



Fig.13 Operation of tracking ADC

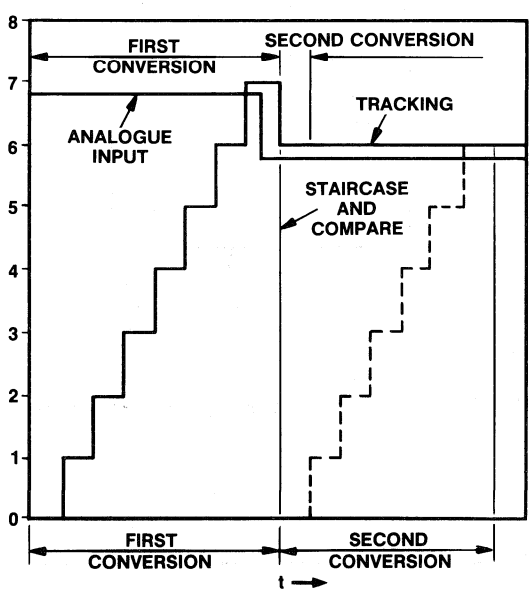



Fig.14 Comparison of ramp and compare and tracking ADC

In general it can be said that a tracking converter will follow signals whose rate of change is less than $\pm$ 1LSB $\times$ clock frequency. If this condition is met there is no need to use a sample-and-hold circuit on the analogue input.

A tracking technique is used in the ZN433 series of converters.

### 2.2.4 Successive approximation converters

The operation of a staircase and compare ADC is analogous to weighing, say an 11 gramme weight, on a balance by adding one gramme weights until the scale tips, which is clearly a very slow method. A faster procedure, known as successive approximation, uses weights of 16, 8, 4 2 and 1 grammes. The 16 gramme weight is tried first and is discarded because it tips the scale. The 8 gramme weight is tried next, and is left on the pan. Next the 4 gramme weight is tried and discarded, and the 2 and 1 gramme weights are tried and retained. The final result is the sum of the weights remaining on the scale pan, and the operation has taken 5 'cycles' as opposed to 11 'cycles' for the staircase and compare method.

The principle of a successive approximation ADC is identical. The MSB of a DAC is first set to '1' and the output is compared to the analogue input. If it is greater than the input the MSB is reset to '0', otherwise it is left at '1'. The next bit is then set to '1' and the DAC output is again compared to the analogue input. Again it is either reset or left at '1' depending on the result of the comparison. This procedure is repeated for every bit down to the LSB, and the final code to the DAC is the output code of the ADC. A successive approximation cycle is illustrated in Fig. 15.

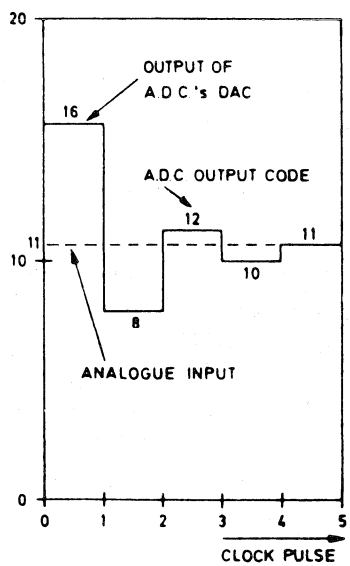



Fig. 15 Operation of a successive approximation ADC

The successive approximation technique is used in most of the Plessey data converters that operate below video speeds.

### 2.2.5 Dual-slope converters

Dual-slope integration is one of the slowest methods of A-D conversion, but it offers high resolution at a modest cost.

A block diagram of a dual-slope converter is shown in Fig. 16. It operates in the following manner: Switch S1 is closed by the control logic, S4 is opened and the input voltage is integrated for n clock periods, where n is usually the maximum count of the counter. At the end of this time the integrator output voltage, $V_O$, is $\frac{-V_{in}\, n\, T_c}{RC}$ where $T_c$ is the clock period. This is shown in Fig. 17.

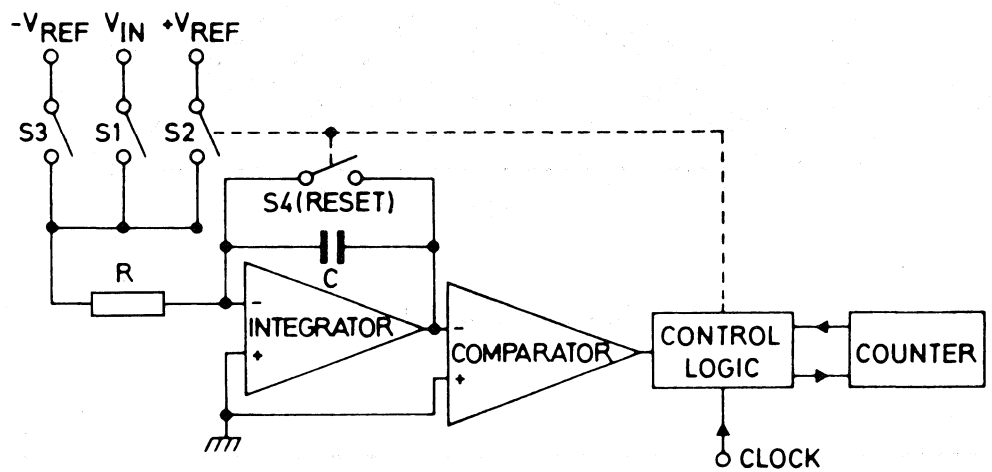



**Fig. 16 Dual-slope ADC**

During this period the polarity of the input signal is detected by the comparator. At the end of the integration period S1 is opened and, depending on the polarity of $V_{in}$, either S2 or S3 is closed to connect the integrator to a reference voltage of opposite polarity to $V_{in}$. The counter is now allowed to count from zero until the integrator output reaches 0V, when the comparator output changes state and the counter is stopped. Since the integration is over the same voltage range ($V_O$), $V_O = \frac{-V_{REF} \times T_c}{RC}$, where X is the count reached by the time the integrator output

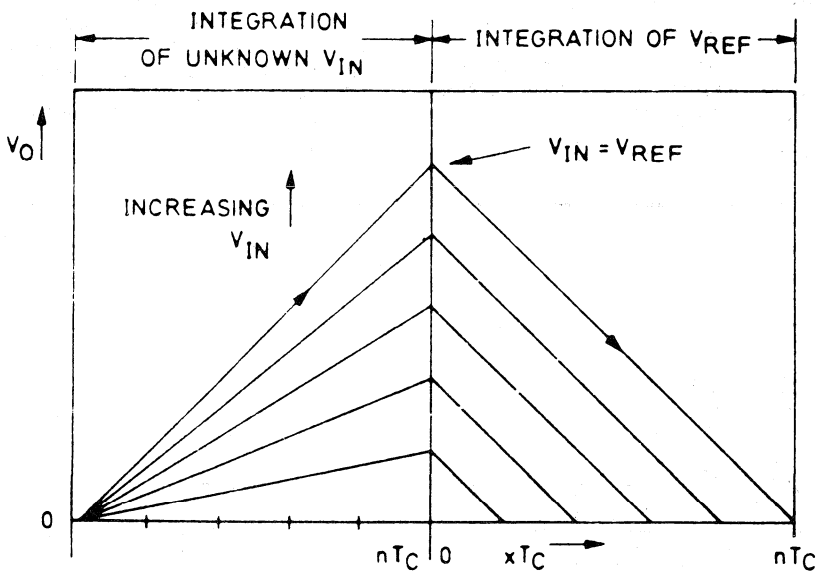



**Fig. 17 Operation of dual-slope ADC**

crosses zero. Thus

$$\frac{V_{in.}\ n\ T_c}{RC} = \frac{V_{REF}\ X\ T_c}{RC}$$

$$\text{or } X = \frac{V_{in.}\ n}{V_{REF}}$$

Since n and $V_{REF}$ are both fixed the output count is proportional to the input voltage. Since both the first and second integrations occur under identical conditions the converter is unaffected by any long term variations in $T_c$, R or C, as demonstrated by the disappearance of these terms from the final equation. The only factors affecting the accuracy of the converter are (1) the stability of $V_{REF}$ (2) the stability of the 'on' resistance of S1 to S3 and (3) drift in the integrator and comparator op-amps. These affects can be minimised by careful design.

Dual-slope converters are generally used where high resolution and low cost are more important than speed, for example in digital voltmeters.

The ZNA216 is a DVM logic sub-system containing the clock, counter and all control logic necessary for dual-slope converter or DVM.

## 2.3 A-D parameters and definitions

### 2.3.1. A-D converter errors

Like DACs, practical ADCs are subject to a number of error sources, and since most ADCs contain a reference DAC, many of these error sources are the same for both types of converter.

### 2.3.2 Quantising error (uncertainty)

Quantising error is an ADC specification that has no counterpart in DAC specifications. For each input code of a DAC there is a unique analogue output level, but for any ADC output code there is a 1LSB range of analogue input levels. It is thus not possible to tell from the output code the precise value of the analogue level, there being a quantising error or uncertainty of ± ½LSB. Since all ADCs have this inherent quantising error the parameter is frequently not quoted in specifications.

### 2.3.3 Missing codes

Missing codes are perhaps best explained by considering the operation of a staircase and compare type 3-bit ADC which has a non-monotonic DAC, as shown in Fig. 18. The reference DAC exhibits non-monotonicity at input code 4, i.e. step 4 of the staircase decreases. There is thus no way in which the counter can be stopped at this code. If the analogue input is less than the DAC output for code 3 then the comparator will stop the counter before 4 is reached. If the analogue input is greater than output 3 it must also be greater than output 4, so the comparator will not change state at code 4.

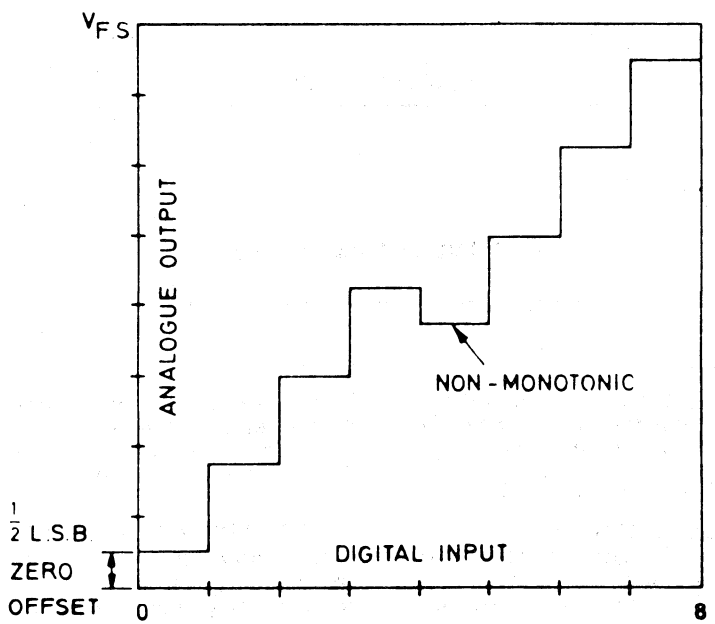



**Fig. 18 Non-monotonic DAC used in an ADC**

Output code 4 will thus never appear and is known as a 'missing' code. The transfer function of an ADC with a missing code is shown in Fig. 19.

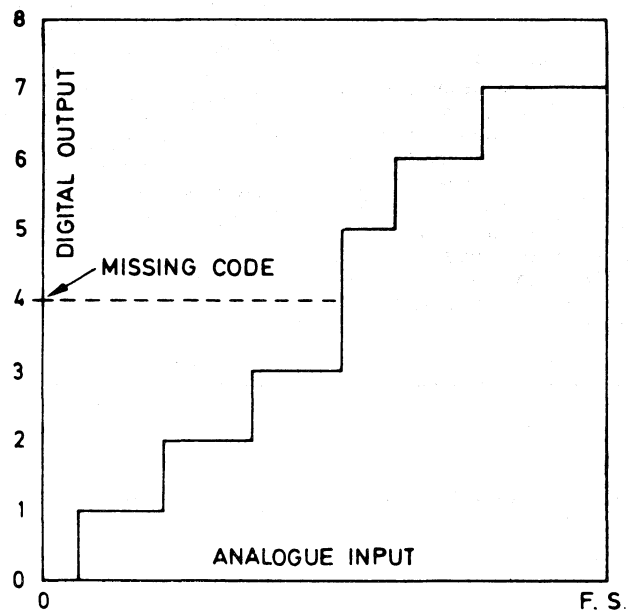



**Fig. 19 ADC with missing code**

### 2.3.4 Zero transition

As explained earlier, the zero of an ADC is usually trimmed so that the output transition from 0 to 1 occurs at an input level corresponding to ½LSB, i.e. $\frac{1}{2}\frac{V_{FS}}{2^n}$. However, as supplied the reference DAC of an ADC I.C. will not have the ½LSB offset necessary to achieve this. The zero transition will thus occur at 1LSB plus the DAC zero error, plus the comparator offset voltage. These three parameters are frequently lumped together as the (untrimmed) zero transition of the ADC.

### 2.3.5 Gain error

This is the difference between the slope of a line drawn between the actual zero and full-scale transition points and that of a line drawn through the ideal transition points.

### 2.3.6 Non-linearity (linearity error)

Non-linearity is the maximum amount by which any actual transition points deviates from the corresponding ideal transition point. It is specified as a percentage of full-scale or a fraction of an LSB. A linearity error of less than ± ½LBS assures no missing codes.

### 2.3.7 Differential non-linearity

This is the maximum difference between any 1LSB increment of the analogue input and the ideal size of an LSB increment $\frac{V_{FS}}{2^n}$. Differential non-linearity of less than 1LSB guarantees no missing codes.

### 2.3.8 Resolution

The resolution of an ADC is simply the number of bit outputs that the converter possesses. As with a DAC, resolution implies nothing about the accuracy of a device.

### 2.3.9 Useful resolution

Useful resolution is the resolution (number of bits) at which an ADC has no missing codes, which for Ferranti ADCs is guaranteed over the operating temperature range. As with DACs, an n-bit ADC may have a useful resolution less than n bits, for reasons previously explained.

### 2.3.10 Conversion time

The time taken for an ADC to perform a complete conversion is known as the conversion time. For successive approximation converters conversion time is fixed by the number of bits and the clock frequency. However, for other types, conversion time may vary with input voltage. For example, a ramp and compare ADC requires $2^n - 1$ clock pulses for a full-scale conversion but only one clock pulse for a one bit conversion. It is thus important to check exactly what is being specified.

## 2.4 Bipolar operation

As with a DAC, an ADC may be used for bipolar operation. Taking the ZN427 as an example the input is offset by $\frac{+V_{REF}}{2}$ so that the input voltage presented to the ADC is always positive, even with negative input voltages down to $\frac{-V_{REF}}{2}$. The principle of offsetting an ADC input is illustrated in Fig. 20, whilst the transfer function of a 3-bit bipolar ADC is shown in Fig. 21. In this case the **output** coding is known as offset binary.

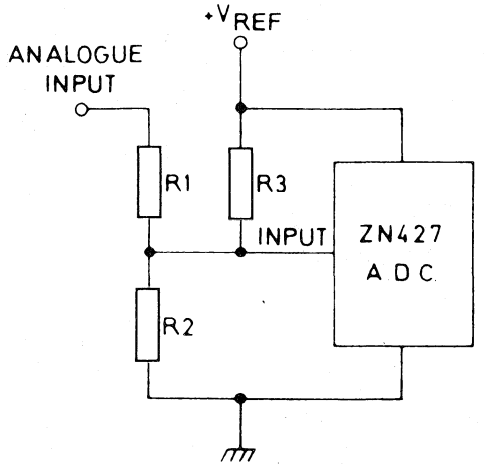



Fig. 20 Bipolar operation of an ADC

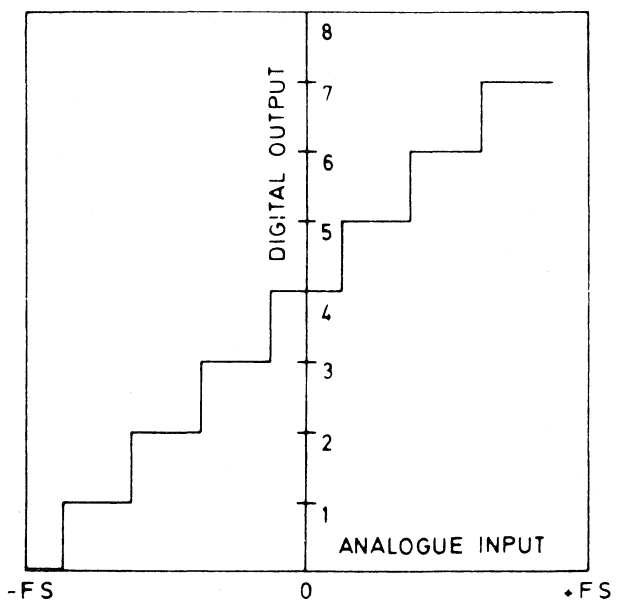



Fig. 21 Bipolar transfer characteristics of an ADC

# AP9007 Video ADC Evaluation Board



**The AP9007 evaluation board provides an easy-to-use demonstration system for the SP94308 8-bit ADC. The versatility of the evaluation board allows the SP94308 to be optimised for many different applications, with little effort. The evaluation board contains circuitry for generating reference voltages, separating the sync and buffering the clock.**

## BOARD FEATURES

- 8-Bit 18 MSPS
- On-Board Sync Separator
- On-Board Voltage Reference
- Buffered Clock Output
- Adjustable Reference Chain Voltages
- Adjustable Clamp Level
- TTL or ECL Level Clock Input
- TTL Level Outputs

## INPUT CONDITIONS

- +5V and -5.2V Power Supplies
- TTL or ECL Clock (AC Coupled On Board)
- Active Low Clamp Pulse (see Sync Separator)

## APPLICATIONS

- Evaluation of the SP94308 A/D Converter
- System Prototyping Aid
- Test Fixture

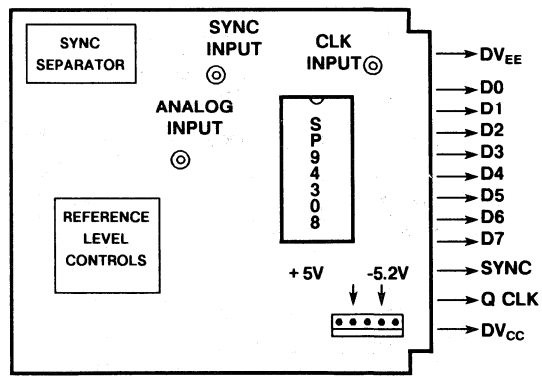



*Fig.1 AP9007 simplified board layout*

## SP94308 FEATURES

### High Accuracy

An accuracy of ±¾ LSB to 8 bits enables high quality TV pictures to be digitised without noticeable contouring.

### High Speed

The high sampling rate of the device facilitates digitisation of wide bandwidth video. Clocking at high speeds (4x colour subcarrier) also permits easier anti-aliasing filtering, when required.

### High Analog Bandwidth

Wide band video can be digitised with no loss of picture information.

### No Sample and Hold Required

The low aperture jitter and low hold time of the device allow high frequency analog signals to be digitised, without the need of an external sample and hold circuit.

### Internal Clock Buffer

A low level AC coupled signal can be used to clock the device therefore minimising clock breakthrough to other parts of the circuit.

### Internal Sync Clamp

Unlike other video ADCs, the SP94308 accepts AC coupled video signals directly. There is no need for a preceding black level clamp circuit.

### Internal Output Latch

An output latch ensures that the data is available for 90% or more of the clock cycle, therefore no external latching is required.

## INTRODUCTION

A block diagram of the SP94308 is shown in Fig.2. The design of the SP94308 incorporates many of the external support components required by conventional ADCs, when used in video applications. To demonstrate the versatility of the SP94308, two evaluation boards are available.

The AP9007 board described in this application note is designed to allow the device to be interfaced into almost any video system. With this board a wide range of input options are available by merely changing link positions or altering potentiometers. An on-board sync separator is avalable should an external sync pulse by unobtainable. All outputs, buffered clock and sync signals are available at the edge connector.

## GENERAL INFORMATION

The AP9007 evaluation board is designed to demonstrate the flexibility and the many features of the SP94308 Video ADC. The external components and adjustments on this application board allow the device to be interfaced into almost any video system with minimal effort. It also allows experiments to be performed for interfacing with the more unusual systems.

Unlike most video ADCs, especially subranging systems, the SP94308 does not require any preceding sample and hold circuit or buffer amplifier.

To use the full applications board simply connect the supplies to ±5V and apply a standard 1V p-p video signal to the input. Any 15MHz oscillator can be used to clock the device. The level of the clock input should be set to 0.8V p-p (ECL can be used directly, one link change for TTL). The board has been prealigned and will produce a TTL/CMOS digitised output of the active video and sync information. The evaluation board requires no DC clamping, video buffer, sample and hold, sync pulse, clock buffer or output latch.

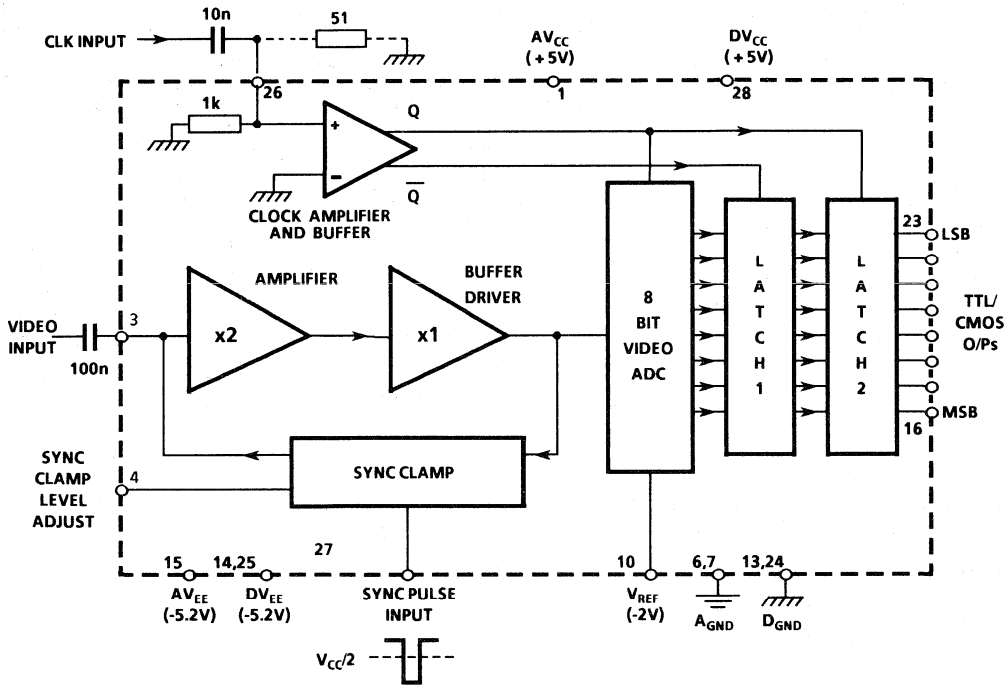



*Fig.2 Block diagram of SP94308*

## Board Supplies

The board is powered from ±5V. The +5V supply requires 70mA and the -5V supply requires 150mA. These are typical figures. All supplies are fed via the power supply connector to the edge connector.

## The Clock Signal (Low Level)

The board is designed to cope with a wide range of clock inputs. The SP94308 includes an internal clock amplifier which enables the clock to be driven from low level AC coupled signals. As the signals are Ac coupled either sine or square waves can be used. The board is configured for 800mV p-p clock inputs at frequencies from 10MHz to 20MHz.

A transistor has been included to buffer the clock signal to the edge connector. This also provides some reverse isolation from reflections or loads on the clock lines etc.

## TTL Clock

Link L4 has been provided to enable direct connection of TTL CLOCK to the board (see Table 2). With this link positioned for TTL, 0.2 of the TTL amplitude will be AC coupled and fed to the device.

## Analog Input

This should be a conventional 1V p-p syncs down composite video signal and can be either NTSC, PAL or SECAM. Please note that if the board is reconfigured for clamping with a burst gate pulse then, for optimum performance the burst should be removed from the analog input.

With any high analog bandwidth ADC, analog inputs that are above the NYQUIST frequency (½fc) will be reflected by the clock (aliases) into the normal signal bandwidth. The patterning caused by this can be removed from the picture by providing an adequate anti-aliasing filter before the ADC input.

## On-Board Clamp Gate

The SP94308 contains an input clamp circuit. This enables the video input to be AC coupled and allows automatic DC alignment of the video within the ADC.

One mode of operation is to clamp on the sync tips of the input video. This requires a clamp gate pulse which is coincidental with the sync tip. The pulse can be generated by the on board sync separator circuitry (see Fig.5 in the data sheet).

## External Clamp Gate

Link L2 provides external clamp gate operation and R13 terminates the clamp gate pulse. The clamp gate input should be normally high, switching down below the device clamp gate input threshold of Vcc/2 during the selected clamp time. See the data sheet for details and information regarding burst gate/black level clamping.

## Reference Voltages

The Plessey TAB1042 is a Quad Operational Amplifier. It is used with a voltage reference to provide full adjustment of all the device reference chain voltages. Please note that this would not be required in a practical minimum component

solution as fixed resistors, potentiometers or zener diodes could be used.

The 10 turn potentiometers RV1 and RV3 allow both the top and bottom of the reference chain to be adjusted. Link L1 allows the REF +ve to be connected to GND.

The preset RV3 is prealigned for -2V. It can, however, be adjusted to suit different levels of input. Also it can be used to reduce the reference chain voltage for applications that require digitisation of the video without digitising the sync.

### Clamp Level Adjust

Link L3 is provided to allow the device to be programmed for sync level clamping or black level clamping. When open circuit this pin will automatically self bias (-1.4V) for applications that require black level clamping. If pin 4 is connected to REF -ve then the device will be configured for applications using sync level clamping.

Link L3 also allows pin 4 of the device to be adjusted using preset RV2. This preset effectively moves the video across the reference resistor chain and can be used to align the device for various digital video standards. See link position, Table 2.

### Digitisation of Active Video Only

Pin 4 of the SP94308 can be programmed for different DC offsets on the input video. This can be used in applications that require digitisation of the active video only. RV3 can be adjusted to reduce the reference voltage, effectively increasing the gain of the device. This allows digitisation of the active video from a standard 1V p-p input. For this applications, RV2 should be adjusted so that the video black level corresponds to the all zeros code.

### Linearity Adjust

This adjustment is again for experimental purposes only and can be replaced with an external resistor as shown in the data sheet, Fig.3. The effect of this adjustment is to fine tune the differential linearity at 15 critical codes. This adjustment is best performed with a video ramp input applied to the board while the reconstructed output is viewed on an oscilloscope.

TOP VIEW
OF UNDERSIDE PINS

ALL TOP PINS = GND

| Pin No. | Function |
|---|---|
| 1 | NC |
| 2 | NC |
| 3 | NC |
| 4 | NC |
| 5 | NC |
| 6 | NC |
| 7 | NC |
| 8 | -5.2V |
| 9 | -5.2V |
| 10 | A0 LSB |
| 11 | A1 |
| 12 | A2 |
| 13 | A3 |
| 14 | A4 |
| 15 | A5 |
| 16 | A6 |
| 17 | A7 MSB |
| 18 | NC |
| 19 | NC |
| 20 | NC |
| 21 | NC |
| 22 | SYNC OUT |
| 23 | NC |
| 24 | NC |
| 25 | Q CLOCK |
| 26 | NC |
| 27 | +5V |
| 28 | NC |
| 29 | NC |
| 30 | NC |

*Table 1 Edge connections*

NOTE: Q CLOCK: This is a buffered version of the clock input, with a 0.7V drop due to the emitter follower.

| Name | Position | Description |
|---|---|---|
| L1 | Next to pin 1 on SP94308 made | This link determines whether the REF +ve pin (pin 2) is held to GND or variable.<br><br>If  then REF +ve is tied to GND<br><br>If  then the REF +ve adjust pot is active |
| L2 | Just right of the sync input | This link selects the internal/external sync option.<br><br>If  the external sync must be provided<br><br>If  the internal sync separator is selected. |
| L3 | Left of pins 5,6 on SP94308 | This link selects the voltage on the sync level adjust input (pin 4)<br><br>If  sync level adjust = REF -ve, -2V (Sync level clamping)<br><br>If  sync level adjust is variable by the Sync pot<br><br>If  sync level adjust is open circuit (black level clamping) |
| L4 | Right of SP94308 | This link selects full clock or attenuated clock input<br><br>If  full amplitude clock signal goes to device<br><br>If  0.2 x clock signal amplitude goes to device |
| L5 | Left of pins 12,13 on SP94308 | This link when open circuit leaves pin 18 (-250mV adjust) open circuit but decoupled. If the link is present then the Lin Adj pot is operational. |

*Table 2 Link positions*

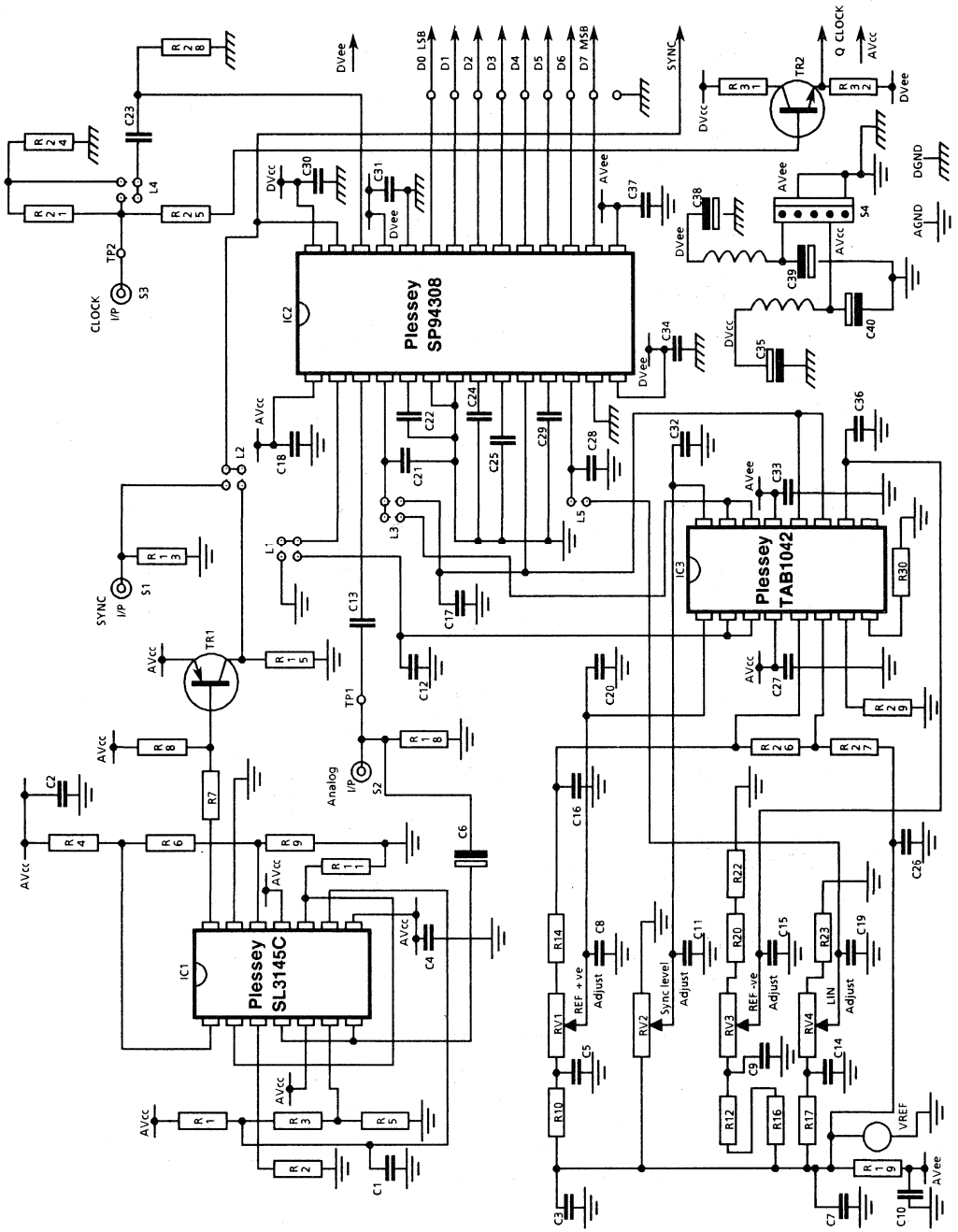



*Fig.3 SP94308 test/evaluation board*

| RESISTORS | | | |
|---|---|---|---|
| R1 | 10k | R17 | 1kΩ |
| R2 | 560Ω | R18 | 75Ω 1/8W |
| R3 | 390Ω | R19 | 330Ω |
| R4 | 10k | R20 | 1.2k |
| R5 | 10k | R21 | 39Ω |
| R6 | 10k | R22 | 47Ω |
| R7 | 2.2k | R23 | 39Ω |
| R8 | 560Ω | R24 | 10Ω |
| R9 | 10k | R25 | 10Ω |
| R10 | 10k | R26 | 1k |
| R11 | 1k | R27 | 1k |
| R12 | 220Ω | R28 | 1k |
| R13 | 47Ω 1/8W | R29 | 1k |
| R14 | 10k | R30 | 220k |
| R15 | 2.2k | R31 | 100Ω |
| R16 | 33Ω | R32 | 270Ω |
| **CAPACITORS** | | | |
| C1 | 1μF | C21 | 100nF |
| C2 | 10nF | C22 | 27pF |
| C3 | 10nF | C23 | 100nF |
| C4 | 10nF | C24 | 100nF |
| C5 | 10nF | C25 | 100nF |
| C6 | 47μF (Electrolytic) | C26 | 10nF |
| C7 | 10nF | C27 | 10nF |
| C8 | 10nF | C28 | 100nF |
| C9 | 10nF | C29 | 100nF |
| C10 | 10nF | C30 | 10nF |
| C11 | 10nF | C31 | 10nF |
| C12 | 10nF | C32 | 10nF |
| C13 | 100nF | C33 | 10nF |
| C14 | 10nF | C34 | 10nF |
| C15 | 10nF | C35 | 47μF (Electrolytic) |
| C16 | 10nF | C36 | 10nF |
| C17 | 0.47μF | C37 | 10nF |
| C18 | 10nF | C38 | 47μF (Electrolytic) |
| C19 | 10nF | C39 | 47μF (Electrolytic) |
| C20 | 10nF | C40 | 47μF (Electrolytic) |
| **POTENTIOMETERS** | | | |
| RV1 | 1k (Multiturn Cermet) | RV3 | 1k (Multiturn Cermet) |
| RV2 | 1k (Multiturn Cermet) | RV4 | 100Ω (Multiturn Cermet) |
| **SEMICONDUCTORS** | | | |
| IC1 | SL3145C | TR1 | 2N3906 |
| IC2 | SP94308 | TR2 | 2N3904 |
| IC3 | TAB1042 | $V_{REF}$ | ZNREF025 |
| **MISCELLANEOUS** | | | |
| S1 - S3 | Sub-Vis Sockets | 5 off | Micro Shunts |
| S4 | KK Molex Socket | 4 off | Rubber Feet |
| L1 - L4 | 4-way Unshrouded Header | 11 off | Veropins |
| L5 | 2-way Unshrouded Header | | |

*Table 3 Component list for SP94308 test/evaluation board*

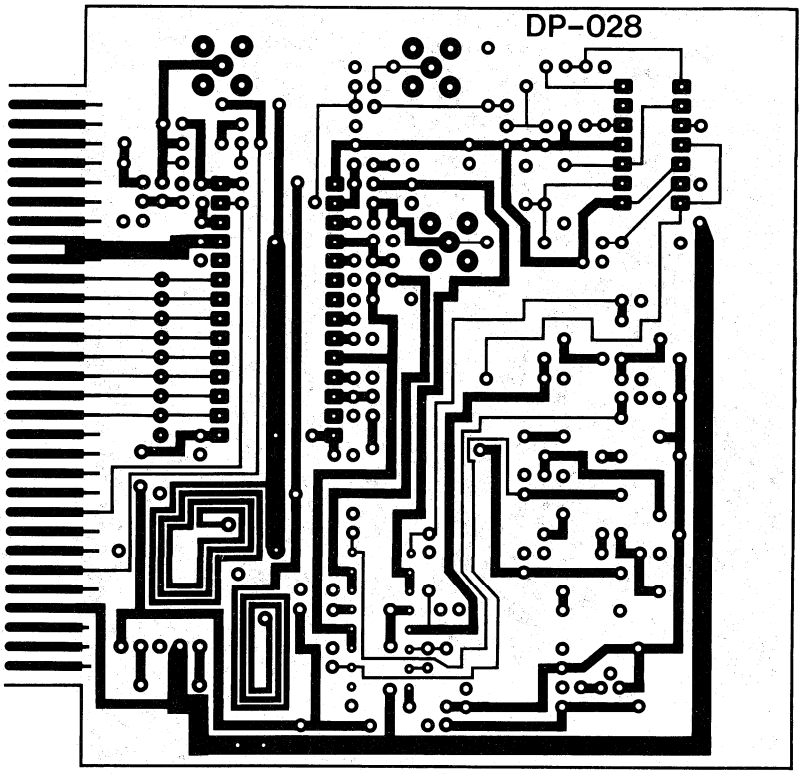



*Fig.4(a) AP9007 PCB copper track (1:1)*

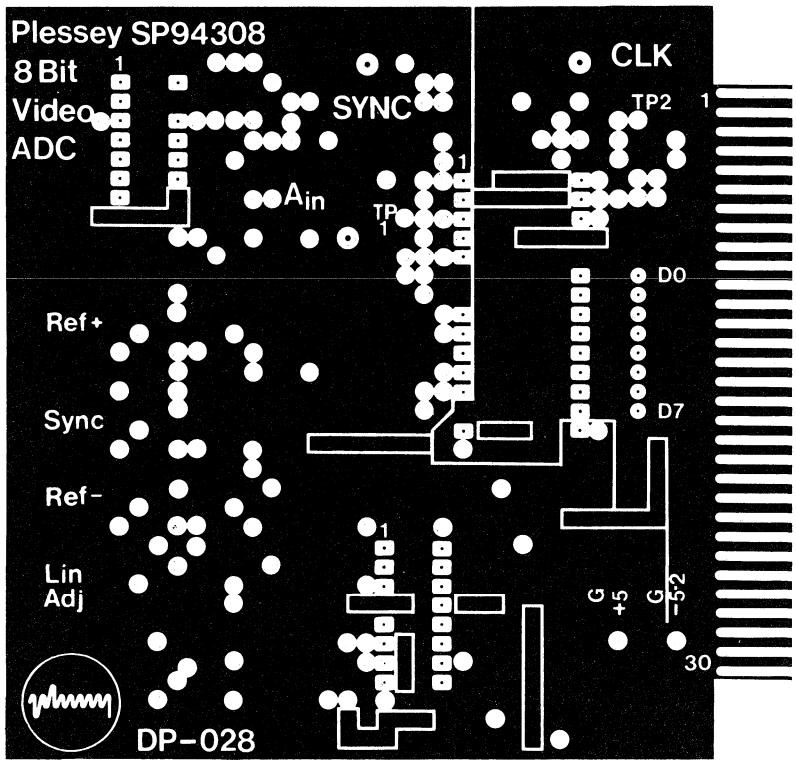



*Fig.4(b) AP9007 PCB ground plane and component side (1:1)*

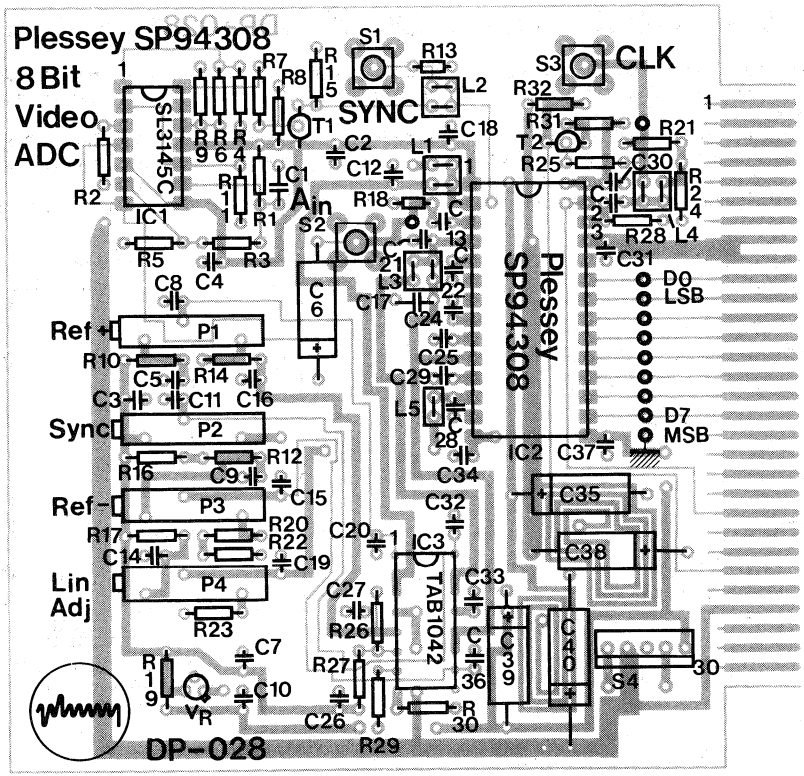



*Fig.4(c) AP9007 component layout (1:1)*

# AP9008 Low Cost Video ADC Evaluation Board AN57

**The Plessey AP9008 evaluation board provides a practical, low cost, video application circuit for the SP94308, 8-bit ADC. The features included within the SP94308 reduce the number of external support circuits and components required to produce a complete ADC system.**

**The AP9008 minimum component application board is designed to demonstrate the flexibility of the SP94308, whilst maintaining a low component count. Although the board can be used in a standalone manner, in a real system a number of components can be omitted e.g. termination resistors, power supply decoupling capacitors etc.**

**The SP94308 is designed to eliminate the need for the sample and hold circuit and buffer amplifier usually required by video ADC systems.**

## BOARD FEATURES

- 8-Bit 18 MSPS
- Low Component Count
- Sync and Clock available at Edge Connector
- Only one External Reference Required
- Optional Clamp Level Input
- ECL Level Clock Input
- TTL Level Outputs

## INPUT CONDITIONS

- +5V and -5.2V Power Supplies
- Clock Input 800mV p-p, AC Coupled On Board
- Active Low Clamp Pulse (see Data Sheet)
- Negative Reference Voltage (normally -2V)
- Clamp Level Input (Optional)

## APPLICATIONS

- Evaluation of the SP94308 A/D Converter
- System Prototyping Aid
- Test Fixture

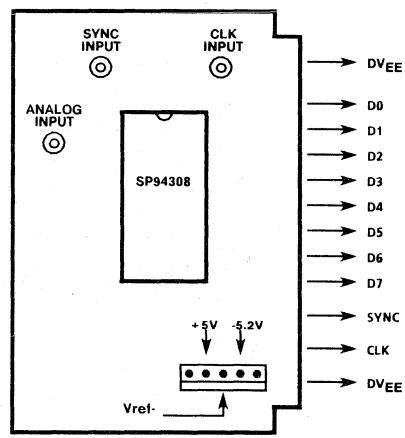



*Fig.1 AP9008 simplified board layout*

## APPLICATION INFORMATION

### Power Supplies

Power supplies for the board are fed via the Molex connector S4. The voltages and currents required are, +5V at 40mA and -5.2V at 110mA. A negative reference voltage is required by the device and this can be applied to the middle pin of the power supply connector. This reference takes approximately 6mA at -2V.

Both the +5V and -5.2V power rails are available at the edge connector, pins 27 and 8 to 9 respectively.

### Clock Input

Clock input is via the SMC socket S3 and is brought out to the edge connector pin 25. The device is designed to accept low level clock signals. This reduces the possibility of clock pick-up by other parts of the TV or system. On-board AC coupling removes any DC offset. This allows the device to be driven from ECL levels or any 50Ω generator that can produce up to 800mV.

The board can be driven from sine or square wave signals. However, if sine waves are used the maximum recommended amplitude signal is 800mV. This produces the fastest edge speeds at the clock input and will reduce aperture uncertainty caused by clock noise or jitter.

### Analog Input

The analog input is fed to the board via SMC socket S1 and is terminated by a 75Ω resistor (video standard termination).

The SP94308 can accept a conventional 1V p-p syncs down composite video signal which can be either NTSC, PAL or SECAM. Note that if the board is reconfigured for clamping with a burst gate pulse then, for optimum performance, the burst should be removed from the analog input. For applications requiring black level clamping or other video levels please refer to Digitisation of Active Video below.

With any high analog bandwidth ADC, analog inputs that are above the Nyquist frequency (½fc) will be reflected by the clock (aliases) into the normal signal bandwidth. The patterning caused by this can be removed from the picture by providing an adequate anti-aliasing filter before the ADC input.

### Clamp Gate Input

The clamp gate signal should be fed to the board via SMC connector S2 and is terminated by a 50Ω resistor. The clamp gate input is also taken to the edge connector, pin 22.

For normal sync level clamping, the clamp gate input should be normally high, switching down thorugh the device input threshold (Vcc/2) during the sync period. Details of black level clamping are given in the data sheet and in Digitisation of active Video.

## Reference

The negative reference for the SP94308 can be provided in a number of ways. In applications where accurate reference control is required, the voltage may be applied via the middle pin of the power supply connector S4. For less stringent systems R4 or D1 may be added to generate the reference from the -5.2V supply. If -2V is required R4 should be approximately 560Ω. Digitisation of Active Video details other possible voltages for the reference level.

## Clamp Level : Link 1

If a standard 1V p-p video signal is to be digitised, then link 1 should be used to connect the negative reference to the clamp level adjust. Link 1 can be left open circuit in which case the clamp level adjust input will float to -1.4V for applications requiring black level clamping. To align the device to other digital standards it may be necessary to take the clamp level adjust to different voltage levels. In this case, feed the required voltage into the upper side of link 1.

## Digitisation of Active Video

In the previous sections digitisation of 1V p-p video plus sync has been considered, using the sync tip as the clamping level. The versatility of the SP94308 allows effective alteration of the gain and offset of the device, so enabling specific sections of the video waveform to be digitised. For example, Fig.2 shows a luma signal in which only the active video is to be digitised. The SP94308 has an internal buffer with a gain of 2, giving the internal voltages shown in parentheses. When the sync pulse input is taken low, the internal clamp circuit offsets the waveform to the voltage applied on the sync level adjust pin. Fig.3 shows the result of sync level clamping to -2V, before and after the internal buffer. As only the active video is to be digitised, i.e. the section from 0 to -1.4V in Fig.3(b), then the voltage applied to pin 10 (REF -ve) should now be -1.4V. Reducing the voltage on the reference chain of the ADC can be compared to increasing the gain of the system. However, care should be taken when using this approach as a slight reduction in linearity will occur.

If black level clamping is required then setting the sync level adjust to -1.4V (Note: sync level adjust will float to 0.7 x REF -ve) and REF -ve to -1.4V will achieve the same results as in Fig.3, see Fig.4.

TOP VIEW
OF UNDERSIDE PINS

ALL TOP PINS = GND

| Pin No. | Function |
|---|---|
| 1 | NC |
| 2 | NC |
| 3 | NC |
| 4 | NC |
| 5 | NC |
| 6 | NC |
| 7 | NC |
| 8 | -5.2V |
| 9 | -5.2V |
| 10 | D0 LSB |
| 11 | D1 |
| 12 | D2 |
| 13 | D3 |
| 14 | D4 |
| 15 | D5 |
| 16 | D6 |
| 17 | D7 MSB |
| 18 | NC |
| 19 | NC |
| 20 | NC |
| 21 | NC |
| 22 | SYNC OUT |
| 23 | NC |
| 24 | NC |
| 25 | CLOCK O/P |
| 26 | NC |
| 27 | +5V |
| 28 | NC |
| 29 | NC |
| 30 | NC |

*Table 1 Edge connections*

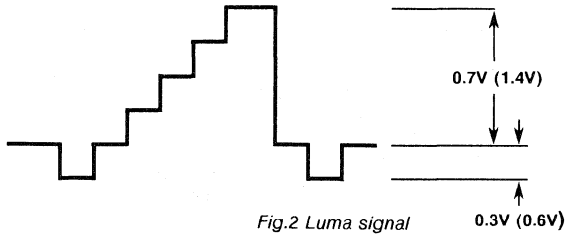
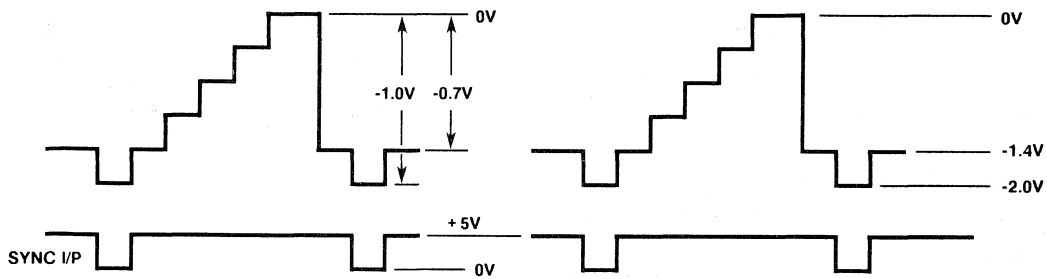


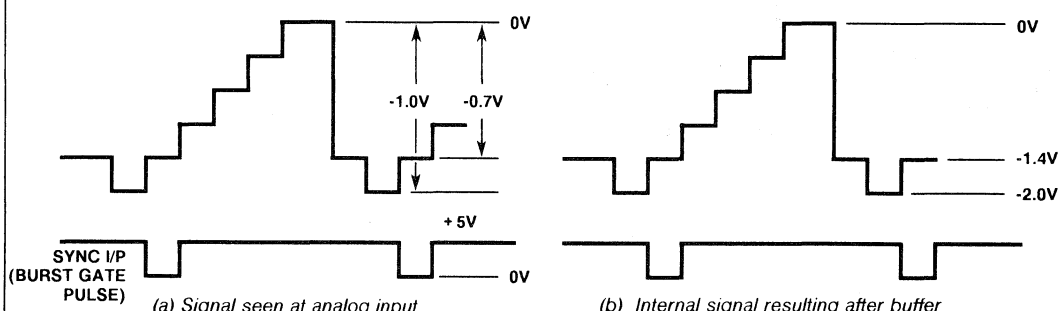

*Fig.2 Luma signal*




*(a) Signal seen at analog input*

*(b) Internal signal resulting after buffer*

*Fig.3 Luma signal after sync level clamping, sync level adjust =-2V*




*(a) Signal seen at analog input*

*(b) Internal signal resulting after buffer*

*Fig.4 Luma signal after black level clamping, sync level adjust =-1.4V*

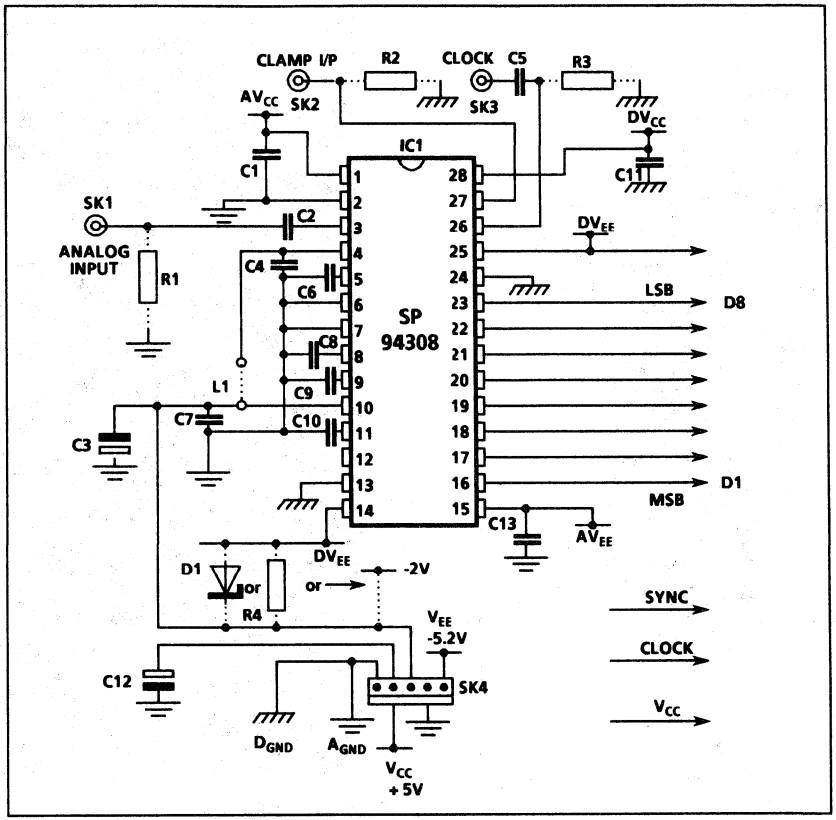



*Fig. 5 AP9008 circuit diagram*

| RESISTORS | | CAPACITORS for ADC, Clamp, Bias etc. | |
|---|---|---|---|
| R1 | 75Ω (Optional Termination) | C1 | 100nF (Optional Decoupling) |
| R2 | 47Ω (Optional Termination) | C2 | 100nF (Input Coupling & Line Clamp) |
| R3 | 47Ω (Optional Termination) | C3 | 47μF (Electrolytic Decoupling) |
| R4 | Approx.560Ω (Optional Low Cost -2V) | C4 | 100nF (Optional Decoupling) |
| | | C5 | 100nF (Coupling) |
| **SEMICONDUCTORS** | | C6 | 27pF at 20MHz or 47pF at 10MHz Clock |
| IC1 | SP94308 | C7 | 100nF (Decoupling) |
| D1 | BZX79C3V0 (Optional Low Cost -2V | C8 | 100nF (Decoupling) |
| | | C9 | 100nF (Decoupling) |
| **SOCKETS** | | C10 | 100nF (Decoupling) |
| S1 - S3 | Sub Vis Sockets (Optional) | C11 | 100nF (Optional Decoupling) |
| S4 | KK Molex Socket (Optional) | C12 | 47μF (Electrolytic Decoupling) |
| | | C13 | 100nF (Optional Decoupling) |

*Table 3 Component list and function*

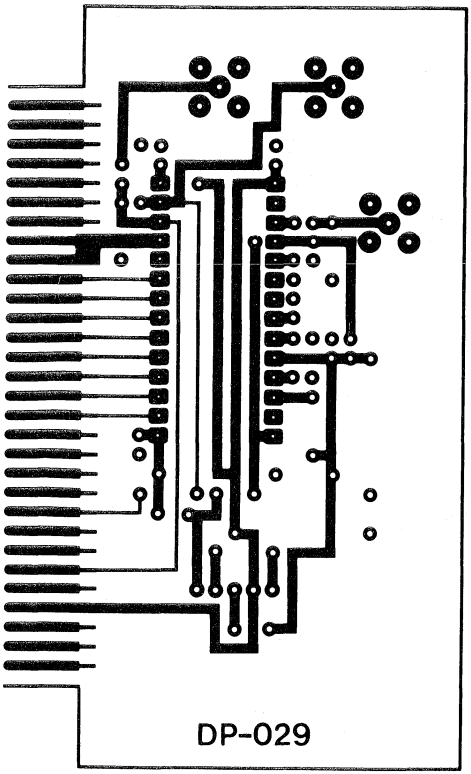



*Fig.6(a) AP9008 PCB copper track (1:1)*

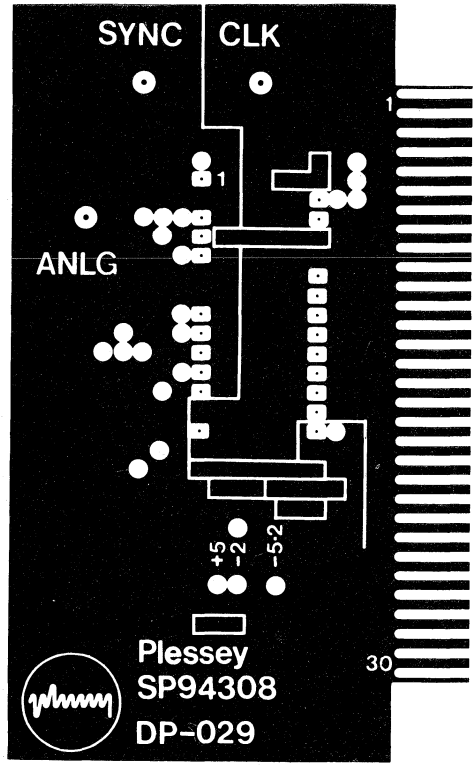



*Fig.6(b) AP9008 PCB ground plane and component side (1:1)*

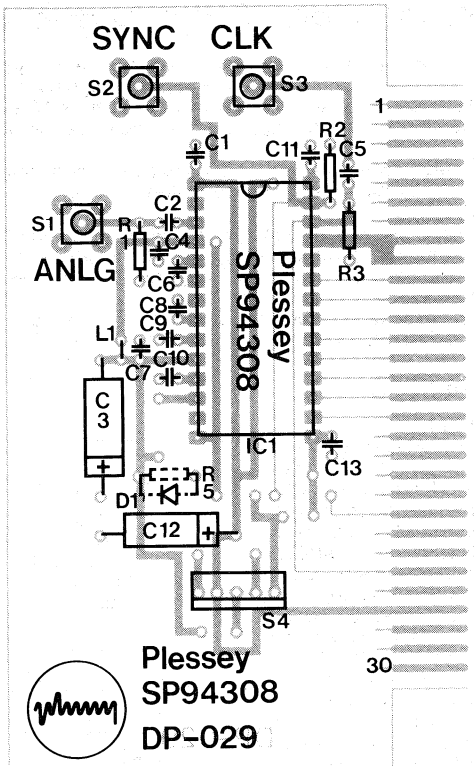



*Fig.6(c) AP9008 component layout (1:1)*

# Evaluation and Comparison of High Speed ADCs



**High speed ADCs are used in many varieties of applications; each application may require special consideration of one or more particular parameters. For example, designers of video (radar or TV) would pay particular attention to differential linearity, whereas designers using the ADC for measurement systems would need to pay attention to integral linearity. Other systems may need accurate information on analog power bandwidth or bit error rate.**

**Specification requirements therefore differ from application to application, and this can make comparisons of ADCs difficult. Outlined below are important tests and evaluation methods, starting with the most simple and progressing to the more sophisticated.**

**ADC evaluation falls into two main groups: the first group utilises high speed digital-to-analog converters to reconstruct the digital output into an analog form that can then be displayed on an oscilloscope. The second group of methods looks directly at the digital data. This requires a high speed logic analyser and usually a GPIB-compatible desk-top computer**

**The following discusses these evaluation methods using the Plessey SP97508 110MHz 8-bit ADC in the evaluation system (AP9006) described later.**

## TESTS USING DAC RECONSTRUCTION

### Method 1. Low Speed Ramp (Fig.1)

This test is very simple. A linear full scale triangular wave (or ramp) is applied to the ADC input, at a frequency that is less than $f_{clock}/(2 \times 2^N)$, where N = number of bits. This ensures that all the timing intervals are displayed. The output from the ADC is then reconstructed with a DAC which should have a greater resolution than the ADC to ensure that all output codes are displayed. The results can then be viewed on a good high resolution oscilloscope.

The resultant staircase has vertical voltages that are due to the DAC and horizontal time intervals that are due to the ADC. Therefore any vertical errors can be ignored as they are due to the DAC alone. The horizontal time intervals can be viewed in more detail by using the oscilloscope to invert and add the input signal. The remainder will be the quantisation noise. The error will be 1 LSB high $\pm\frac{1}{2}$ an LSB. Beware of 'scope input overload and the delay between the two signals when using this method.

A major point of interest on this reconstructed ramp is the mid-step or zero crossing where a large differential error or high speed group of glitches can occur. This is a common problem with many ADCs as the digital section of the ADC is changing from 10000000 to 01111111. All the binary outputs are changing at once and hence large current spikes can result.

Another cause of zero crossing error is four-stage design. Within most 8-bit flash ADCs the reference chain and/or the comparators are split into four ranks. The device can then behave as four 6-bit devices. This can give poor differential steps at seven critical codes along this ramp.

### Reference Voltage Considerations

The overall accuracy of the staircase will be mostly proportional to the reference voltage. This is because the internal comparator offsets will remain constant while the bit size will vary proportionally to the external reference voltage. Therefore it is important to consider the reference voltage before making comparisons between ADC linearity figures. Disadvantages of the ramp method are (a) it is difficult to obtain numerical results - although this can be achieved using a Tektronix 7854 scope - and (b) this test does not reflect the accuracy at speed.

### Method 2. Near Nyquist Beat (Fig.2)

The Nyquist frequency is exactly one half the clock frequency. If a sinewave analog input is set close to this frequency in an unfiltered system, a beat will result. The beat frequency will be

$$f_B = \left|\frac{f_C}{2} - f_{in}\right| \text{ (3MHz in Fig.2)}$$

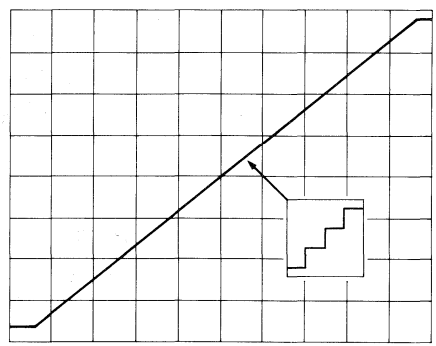


*Fig.1 ADC linearity. 1kHz ramp input sampled at 100MHz (2V I/P to ADC)*

This test is primarily for evaluation of analog bandwidth. The comparators acquire the input voltages at each end of the input dynamic range on successive samples. An ADC that can slew both positively and negatively fast enough to produce an undistorted sinewave beat contains an extremely fast comparator section. Disadvantages of this method are (a) again it is difficult to produce a numerical value of merit, (b) scope triggering is delicate and (c) DAC overshoot can cloud the results.

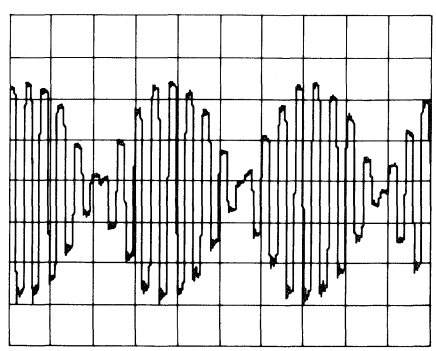


*Fig.2 ADC near Nyquist beat. 47MHz input sampled at 100MHz, 2V I/P to ADC*

## TESTS USING DIRECT DIGITAL ANALYSIS

This group of tests is performed by acquiring the digital data directly from the ADC. The data is usually acquired by a high speed logic analyser and then transferred to a desk-top computer for analysis. The ADC is usually driven with a sinewave of full amplitude. The following gives the more popular methods of analysing and plotting the data. It is essential with all the following methods that the input is set to precisely full scale.

Most of the methods below benefit from phase-locked sampling (stationary sampling). In most cases this enables the number of samples taken to be greatly reduced, therefore improving test/evaluation times.

### Method 1. Histogram Test (Fig.3)

This test plots the output code against occupancy of the code. A histogram is produced that should theoretically form a sinewave cusp. Deviations from this cusp will represent differential and integral linearity errors. A differential error would weight the probability of a code being occupied, either more or less than it should be over a large number of samples. This distorts the cusp in a positive or negative direction at the code in question. The advantage of this test is that it will indicate the dynamic accuracy of the ADC, i.e. the accuracy to input frequencies up to Nyquist. This is of course not practical using a DAC and oscilloscope. The disadvantages of this method are that (a) it requires a large number of samples and (b) as a cusp is formed, direct reading of linearity from the curve is difficult.

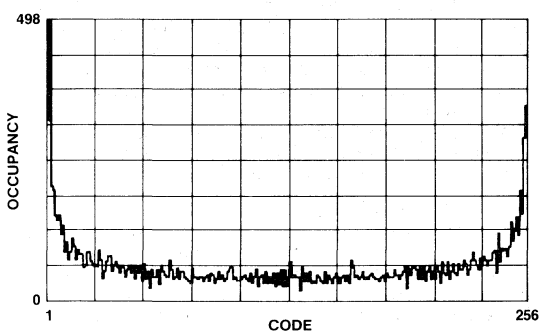



*Fig.3 Histogram test at 30MHz input*

### Method 2.Non-linearity in LSB (Fig.4)

This test is almost identical to the histogram method. The same data can be used within the desk-top computer. Again a large number of samples are taken and again the occupancy of each code is plotted. The subtle difference is that a $\sin^{-1}$ weighting is applied to the results which removes the cusp. The linearity is then plotted :

$$\left[1 - \frac{(Actual\ Probability)}{(\sin^{-1}\ Weighted\ Probability)}\right]$$

As the cusp has been removed, the resulting graph shows at a glance differential non-linearity in terms of LSB. This test can also be performed up to Nyquist limits. Disadvantages are that random errors are averaged out.

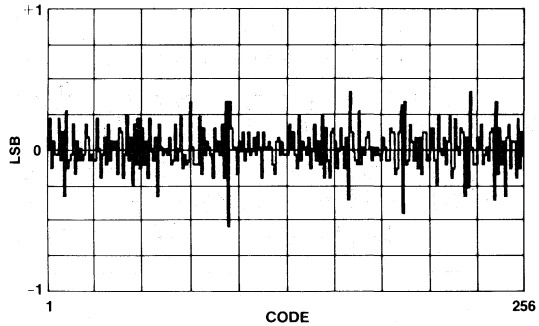



*Fig.4 Differential non-linearity in LSB*

### Method 3. Accumulation Error (Fig.5)

Again, this test can be performed from the initial data. The data is processed to give a graph of integral linearity which can be expressed in two main ways - 'end point' or 'best fit'. The 'best fit' method allows the points to be compared with a line drawn through the average of the results. The 'end point' method is more severe as the line is defined by the end points of the results. From Fig.5 we could quote an integral linearity of ±0.5 LSB for 'best fit', but only ±0.75 LSB for 'end point'. Therefore it is very important to know which method has been used before comparing integral linearity figures.

To form the graph a statistical method is used with many samples taken. The results are corrected for the sinewave cusp and a graph plotted of levels against deviation from the previously defined straight line. This method can also be performed at frequencies up to Nyquist. Fig. 6 shows a plot of end point integral linearity at near Nyquist frequencies for the SP97508. As this test represents the total deviation from a theoretically perfect ADC it is a very useful measurement. It also gives a clear representation of distortion caused by the quantising system.

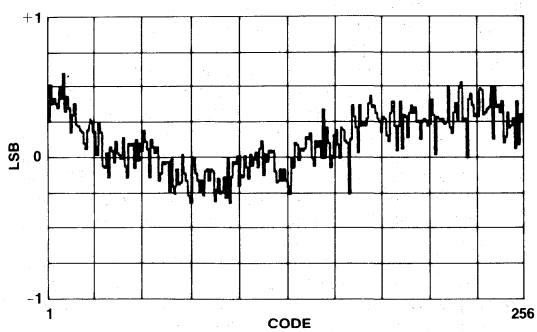



*Fig.5 Accumulation error (integral)*

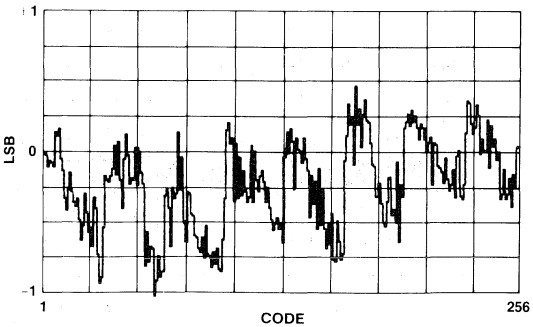



*Fig.6 Accumulation error at 30MHz*

### Method 4. Sinewave Curve Fit

This test is similar again in that the data acquired by a logic analyser is processed by a desk-top computer. The computer generates theoretically perfect sinewave data, from which the actual ADC information, contained in the logic analyser, is subtracted. The data for the perfect ADC is produced by curve fitting: the Least Squares method is usually used to minimise the error between the actual and theoretical data. A theoretically perfect digitised sinewave which has exactly the same amplitude, frequency and phase as the actual data is required. The remaining difference between these groups of data now represents not only differential and integral linearity but also noise and aperture uncertainty effects. The disadvantages of the method are that (a) the programming must be very precise, (b) DC offset errors are ignored.

### Method 5. Fast Fourier Transform

The fast Fourier transform (FFT) is simply a numerical method for conversion from the time domain to frequency domain. The method is based on the fact that any waveform can be constructed from a number of discrete pure sinewaves of different frequencies and amplitudes. These frequencies can then be plotted to give the spectrum of the signal.

Two methods are used for acquiring the data. The first and most popular, as in the previous methods uses a logic analyser, which transfers the data to a desk-top computer for FFT calculations. The second method (usually using a waveform analyser) uses a DAC to reconstruct the data which is digitised and sent to the computer for FFT. The spectral information from this method contains DAC distortions within the results. This can be an advantage if a complete system is to be analysed.

The FFT contains not only linearity information but also other errors that deteriorate the signal-to-noise ratio. Linearity errors cause sidebands to be produced in the frequency domain and so measurement and analysis of the system can be performed in great detail.

The disadvantages of the FFT method are (a) it is important to choose the input frequency to avoid coincidence between the fundamental and harmonics reflected back into the baseband by the sampling technique, (b) the input signal has to be exceptionally pure with very low harmonic content.

### Choice of Tests

To form a good general assessment of a high speed ADC it is necessary to perform the DAC reconstruction tests as they not only show any gross problems with minimal effort, but also give a clear picture of any gross problems with the analog bandwidth and slewing performance of the ADC.

For an evaluation and experimentation system the accumulation methods give a clear picture of performance but for a test system the sinewave curve fit or FFT methods test a wider range of parameters.

## OTHER TESTS AND CONSIDERATIONS

### Aperture Uncertainty

Aperture uncertainty refers to the amount of jitter at the instant the sample is taken. In other words the time taken between one sample point and the next may not be exactly the same on the following cycle. This uncertainty is usually in the order of picoseconds and so measurement is incredibly difficult. Aperture uncertainty is also found within the comparator section of the ADC. The aperture uncertainty will be increased if the comparators take slightly differing times to respond to the sample request. The results from techniques using stationary sampling are probably more than 20% inaccurate at high frequency. The effects of aperture uncertainty can also be masked by the phase jitter on the clock signal used for the ADC.

### Metastable States

This exotic term is used when discussing missing or random data errors. There is a finite probability that when a comparator is latched it is at balance. This in fact would be a very rare event, as noise and hysteresis would tend to trip the comparator within the time it is being latched. Nevertheless figures as high as 1 missing sample in $10^9$ have been quoted.

A balanced comparator would in fact cause an error within the decode ROM and in many ADCs that causes an all '0's output code for that sample.

### Mountain Climb Effect

The 'mountains' here are in fact the spikes produced by the fast edges of the clock. If they are not adequately removed from the reference chain and analog input an interesting effect occurs: as the clock edge speed is increased the reconstructed output will show a DC shift, sometimes above one LSB. This is due to the sample being taken at exactly the same time as the sample edge disturbs the input signal. The result is a 'DC' shift because they will always remain in phase. Good layout using split grounds and good decoupling will minimise this problem.

### Data Valid Time

This is an important and frequently ignored parameter. It is simply the proportion of time that the output data is valid, expressed as a percentage of the minimum clock period. If the ADC has a maximum frequency of 100MHz i.e. a minimum period of 10ns, a 70% data valid time indicates that the data would be valid for 7ns and could be acquired at any time within this period. This is important as the shorter the time, the harder it is to design the system. High cost can result if extra latches and delay lines are needed to collect the data consistently over the specified temperature range.

# AP9006 100MHz 8-Bit A/D-D/A Evaluation System

*(For information only – currently being updated)*

**The AP9006 evaluation system is a complete 8-bit 100MHz analog to digital conversion board. The system comprises an 8-bit ADC with supporting circuitry, a connecting loom and an 8-bit DAC board. This DAC board allows the ADC outputs to be reconstructed and viewed on an oscilloscope.**

**Each individual application of the ADC may require different optimisation of parameters; this board has been designed to meet general requirements but little else should be required to meet the demands of even the most precise 100MHz system.**

*(NOTE: Since publication, the SP9687, SP1692, SP9210 and TAB1042 have been made obsolete)*

## THE EVALUATION SYSTEM - AP9006

Included in the evaluation system are the SP97508 ADC board AP9004 (Fig.7), a length of 100Ω twisted pair and the SP97618 DAC applications board AP9005 (Fig.10). The D-A evaluation board provides a simple method of evaluating the all-important analog bandwidth of the ADC.It is suggested that, near Nyquist is viewed at 100MHz sampling to demonstrate the wide analog bandwidth of the SP97508 (see Figs.2, 3 and 4).

The ADC board (AP9004) comprises one SP97508 (8-bit ADC), one TAB1042 (quad op-amp), one SP9687 (dual comparator) one SP9210, one SP1662, one SL9999 and one RS7805 5V regulator.

### Evaluation Boards

In general, the performance of a high speed ADC can be greatly affected by the circuit board ground plane layout and associated component placements. Completed ADC and DAC boards with connecting loom are therefore available for evaluation and educational use. The items listed in Table 1 can be ordered from our Customer Service department.

| Item | Description |
|---|---|
| AP9004 | CompleteADC board and data |
| AP9005 | Complete DAC board and data |
| AP9006 | Complete ADC, DAC and connecting loom with data (recommended system) |

*Table 1 Evaluation systems*

### Power Supplies

The evaluation system requires external -5.2V and +12V supplies. A +5V supply is also required but this is provided from the +12V supply by an RS7805 regulator on the board. For convenience all power supplies have been taken through the edge connector to supply the DAC evaluation board.

| Supply | AP9004 ADC Board only | AP9006 ADC & DAC System |
|---|---|---|
| -5.2V | 700mA | 1050mA |
| +12V | 110mA | 110mA |

*Table 2 Power supply currents*

The current taken from the -5.2V supply increases to 1050mA when the DAC board is connected, due to the extra current taken by the line termination and device supplies.

### ADC BOARD AP9004

The AP9004 applications board has been designed to allow adjustments to be made to all the important parameters that effect the performance of the SP97508 110MHz ADC. RV2, which adjusts the DC input offset, allows a wide range of input signals to be applied.

A wide range of clock signals can also be applied to the board as the SP9687 and SP1662 devices form a complete clock conditioning circuit for the ADC.

To enable the board to drive lines of 50Ω and 100Ω directly, the SP9210high speed latch has been used.

The TAB1042 (TAB1043 recommended for new designs) quad operational amplifier has been used to provide the adjustable DC voltages which supply the reference chain of the ADC. The bottom of the reference chain $V_{RB}$ can be adjusted using RV3 and the mid reference voltage can be adjusted using RV1.

### Analog Input to the Board

The analog input is fed to the SL9999 and is terminated by 56Ω (R7). An offset can be applied by varying RV2 (see Fig.8).

The SL9999 is a fast ADC driver capable of driving the input capacitance of the SP97508 at over 50MHz and ×4 gain. Hence the peak-peak input voltage to the board is 0.5V.

### The SL9999 ADC Driver

For a full evaluation of the SP97508 the input signal from the signal source should be coupled via R21 and R29 into the ADC. But in practical systems it can be difficult to drive the input capacitance of the ADC. This is due to the combination of high frequency, high capacitance and large voltage swings needed, whilst maintaining good linearity. In addition, the ADC input capacitance changes dynamically with input voltage. These factors led to the development of the SL9999 ADC driver.

The SL9999, unlike other ADC driving circuits, can be used to provide gain as well as satisfying the above requirements. Also the separate buffer in the SL9999 can be used to aid in setting reference voltages for low DC drift applications.

As the SL9999 is an op-amp, the gain of the driver circuit is simply defined by the two resistors R18 and R11; the DC offset is controlled by RV2.

It is important to minimise strays around this ultra fast op-amp. Care should be taken in the choice of components, component placement and track layout. Eighth watt carbon resistors have been used to minimise stray inductance and capacitance and Rf has been positioned directly from pin 3 to pin 13 of the device, to reduce lead length and strays.

Note that the SL9999 is useful for many other difficult applications such as line driving etc. and makes a useful lab stock device.

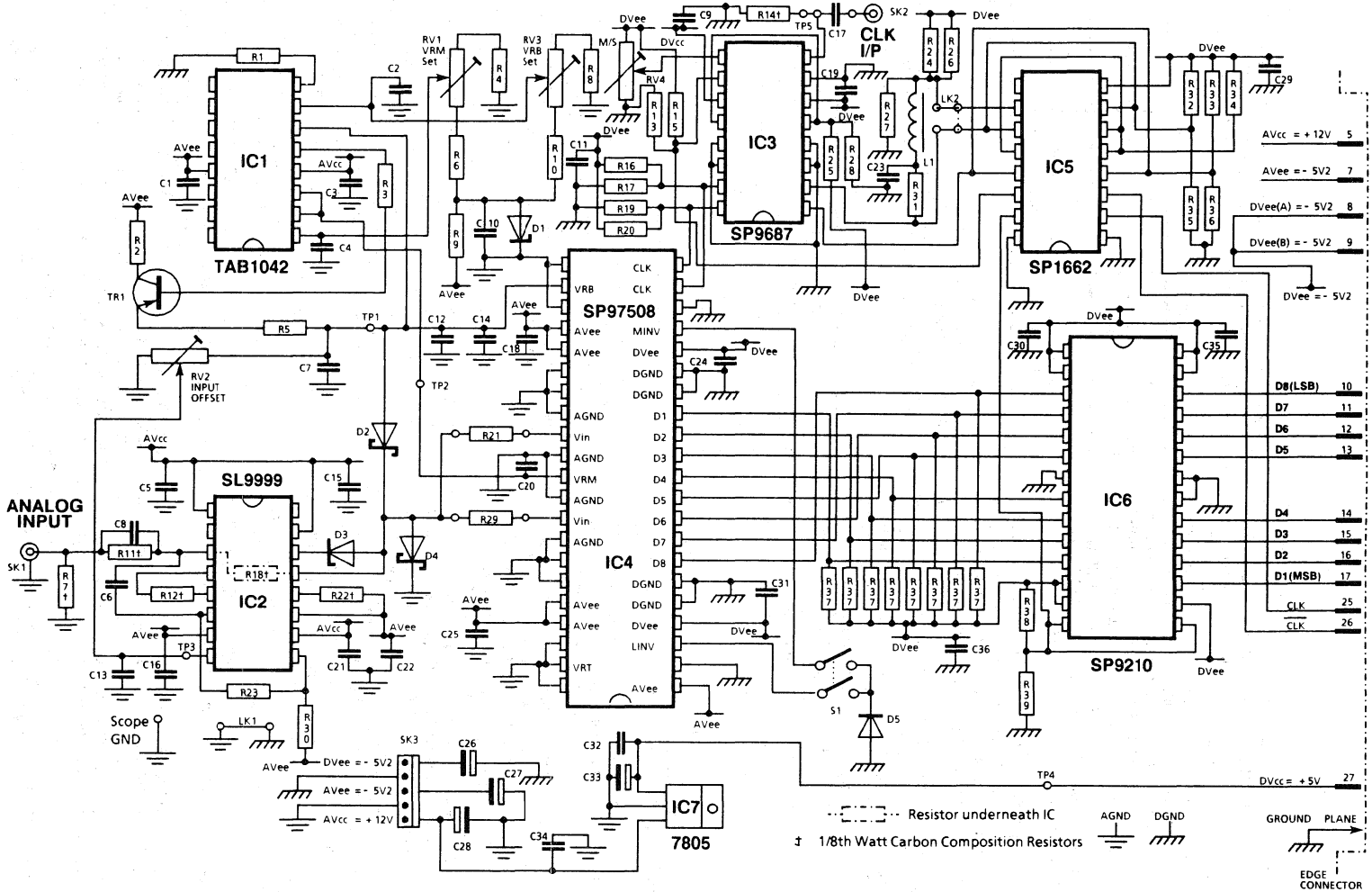



*Fig.7 SP97508 ADC evaluation board AP9004*

## The Clock Conditioning Circuit

Unlike many other 8-bit ADCs the SP97508 can be clocked from a unity mark/space ratio clock, up to its maximum clock frequency (110MHz). This is due to the exceptionally wide bandwidth comparators and latches used in the device design.

As metastable states are of great concern in some communications applications, and the occurrence of these infrequent errors is affected by the mark/space ratio of the clock (in any flash ADC) we have provided a method on the board that can be used to select the clock mark/space ratio. We believe the optimum mark/space ratio for minimum errors is 3 to 1 (see data sheet).

The SP9687 dual comparator has been used to receive the incoming clock from either a sinewave oscillator or a pulse generator. Link LK2 can be positioned to select either unity or 3:1 mark/space ratio clock.

## Component List for the AP9004 Board

### RESISTORS

All ¼W unless otherwise stated

| | | | |
|---|---|---|---|
| R1 | 220kΩ | R21 | 2.7Ω (optional) |
| R2 | 47Ω | R22 | 18Ω 1/8W |
| R3 | 10Ω | R23 | 470Ω |
| R4 | 2.2k | R24 | 1.2k |
| R5 | 10Ω | R25 | 3.9k |
| R6 | 3.3k | R26 | 4.7k |
| R7 | 56Ω 1/8W | R27 | 270Ω |
| R8 | 3.9k | R28 | 1k |
| R9 | 560Ω | R29 | 2.7Ω (optional) |
| R10 | 560Ω | R30 | 270Ω |
| R11 | 560Ω 1/8W | R31 | 220Ω |
| R12 | 220Ω 1/8W | R32 | 270Ω |
| R13 | 150Ω | R33 | 270Ω |
| R14 | 47Ω 1/8W | R34 | 1k |
| R15 | 270Ω | R35 | 150Ω |
| R16 | 270Ω | R36 | 150Ω |
| R17 | 150Ω | R37 | 1kΩ 8-way SIL |
| R18 | 2.2k 1/8W | R38 | 270Ω |
| R19 | 150Ω | R39 | 150Ω |
| R20 | 270Ω | | |

### CAPACITORS

All encapsulated chip unless otherwise stated

| | | | |
|---|---|---|---|
| C1-C5 | 10nF | C24,C25 | 10nF |
| C6 | 3.9pF | C26-C28 | 47µF 16V Electrolytic |
| C7 | 10nF | C29-C31 | 10nF |
| C8 | Optional | C32 | 1µF |
| C9-C11 | 10nF | C33 | 47µF 16V Electrolytic |
| C12 | 10nF | C34 | 220nF |
| C13-C22 | 10nF | C35,C36 | 10nF |
| C23 | 6.8pF | | |

### SEMICONDUCTORS

| | | | |
|---|---|---|---|
| IC1 | TAB 1042* | D1 | ZN REF 025 (2.5V ref. ) |
| IC2 | SL9999 | D2 | BAT 83 |
| IC3 | SP9687 | D3 | BZX 5V6 |
| IC4 | SP97508 | D4 | BAT 83 |
| IC5 | SP1662 | D5 | IN 4148 |
| IC6 | SP9210 | | |
| IC7 | 7805 | TR1 | 2N3906 (PNP) |

*NOTE:The TAB1042 will soon be discontinued. The TAB1043 can be used as a replacement, with a small mask change; please contact the Applications Laboratory if this causes concern.

## SOCKETS

| | |
|---|---|
| SK1,SK2, | PCB Mounting SUB-VIS or SMC |
| SK3 | 5-pin KK MOLEX |

## POTENTIOMETERS

| | |
|---|---|
| RV1-RV4 | 1K Multiturn |

## MISCELLANEOUS

| | |
|---|---|
| 6-off | Veropins |
| S1 | 2-way SPST DIL Switch |
| 1 | Microshunt |
| 4-off | Rubber Feet |
| 1 | 4-way Header |
| 1 | 16 pin Turned Pin IC Socket |
| 1 | Wire Link (24 Gauge Wire) |
| L1 | 220nH Inductor |

## EDGE CONNECTORS (Top View)

| ADC BOARD | | DAC BOARD | |
|---|---|---|---|
| **Pin No.** | **Function** | **Pin No.** | **Function** |
| 1 | N/C | 1 | N/C |
| 2 | N/C | 2 | N/C |
| 3 | N/C | 3 | N/C |
| 4 | N/C | 4 | N/C |
| 5 | $AV_{CC}$ OUT | 5 | N/C |
| 6 | N/C | 6 | N/C |
| 7 | $AV_{EE}$ OUT | 7 | N/C |
| 8 | $DV_{EE}$(A) OUT | 8 | $DV_{EE}$(A) IN |
| 9 | $DV_{EE}$(B) OUT | 9 | $DV_{EE}$(B) IN |
| 10 | D8 LSB | 10 | D8 LSB |
| 11 | D7 | 11 | D7 |
| 12 | D6 | 12 | D6 |
| 13 | D5 | 13 | D5 |
| 14 | D4 | 14 | D4 |
| 15 | D3 | 15 | D3 |
| 16 | D2 | 16 | D2 |
| 17 | D1 MSB | 17 | D1 MSB |
| 18 | N/C | 18 | N/C |
| 19 | N/C | 19 | N/C |
| 20 | N/C | 20 | N/C |
| 21 | N/C | 21 | N/C |
| 22 | N/C | 22 | N/C |
| 23 | N/C | 23 | N/C |
| 24 | N/C | 24 | N/C |
| 25 | CLK | 25 | CLK |
| 26 | $\overline{CLK}$ | 26 | $\overline{CLK}$ |
| 27 | $DV_{CC}$ OUT | 27 | $DV_{CC}$ IN |
| 28 | N/C | 28 | N/C |
| 29 | N/C | 29 | N/C |
| 30 | N/C | 30 | N/C |

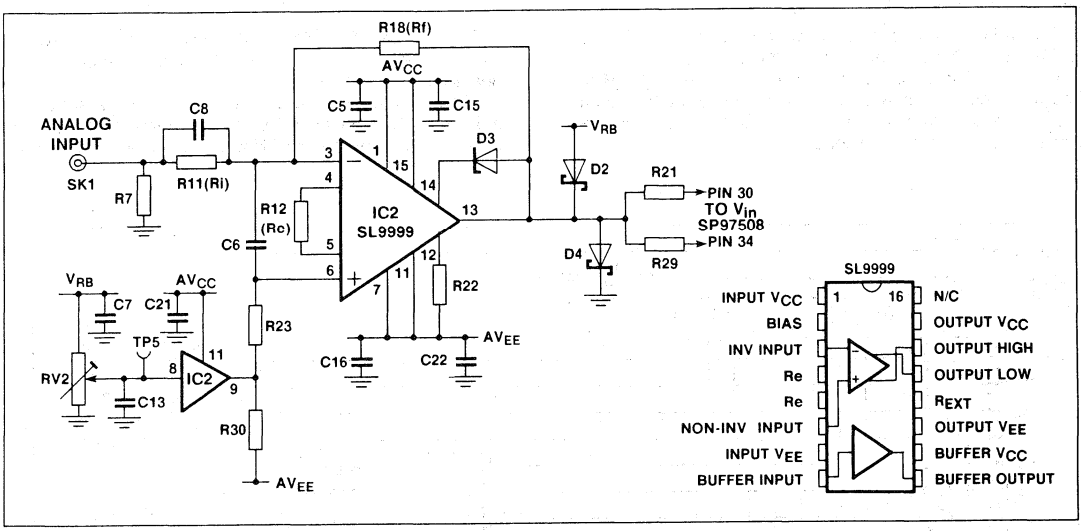



*Fig. 8 Analog input driver for AP9004 ADC board*

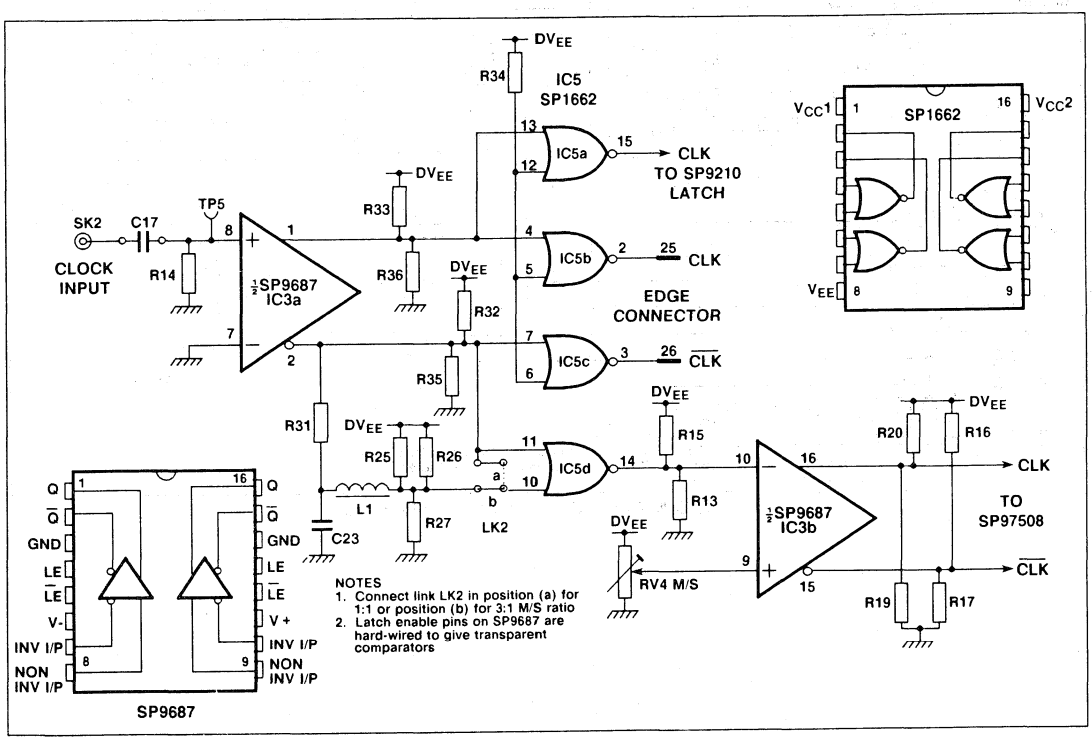



*Fig.9 Clock system for AP9004 board*

## DAC BOARD AP9005

The following information describes the SP97618 250MHz graphics DAC applications board AP9005.

This board is capable of acquiring the 8-Bit 100MHz data from the ADC board in a fast retaining latch. It then converts this data into an analog signal that can be displayed on a fast oscilloscope.

The Plessey SP97618 DAC used on this board is a complete graphics DAC with video control inputs and is ideal for high resolution video signals

The switch S1 can be used to select individual data bits and switch S2 can be used to demonstrate the graphics facilities of the device (FT,FH,BLANK,BRIGHT and SYNC)

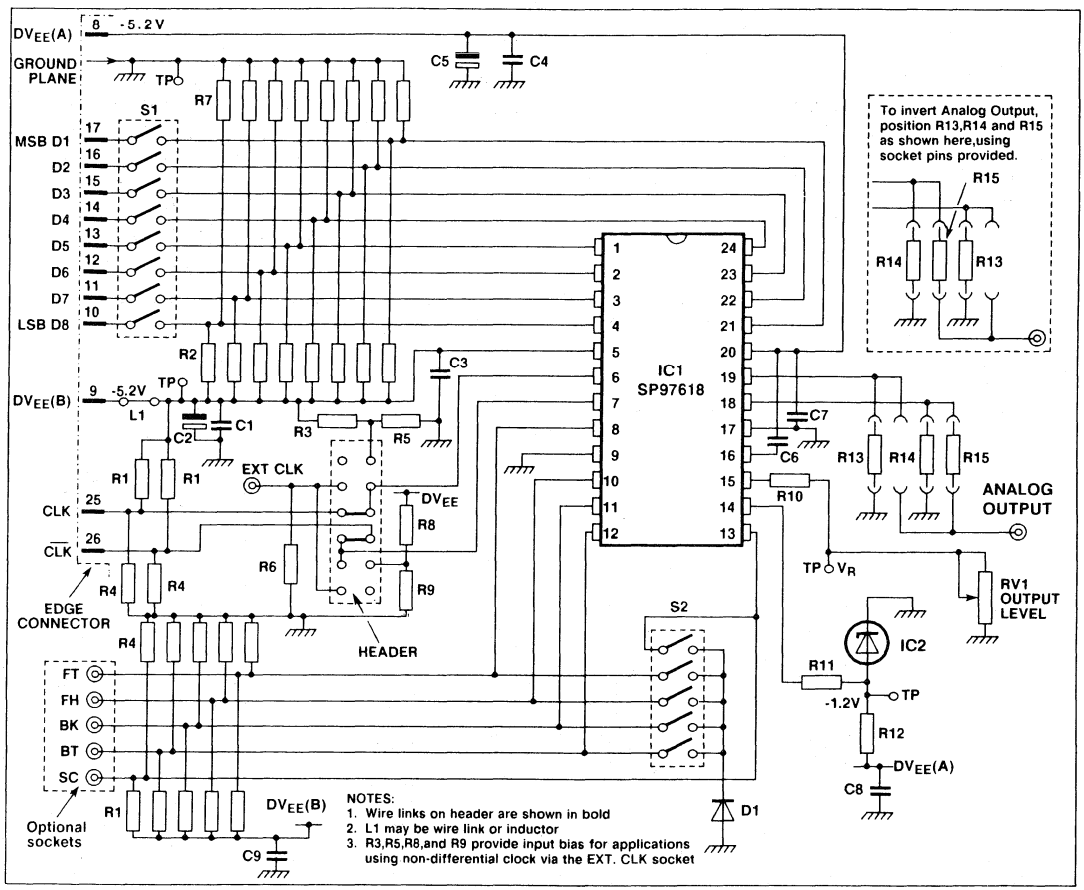



*Fig. 10 SP97618 DAC applications board AP9005*

## RESISTORS

| | |
|---|---|
| R1 | 8 x 270Ω SIL RS Part No. 140-237 |
| R2 | 8 x 270Ω SIL RS Part No. 140-237 |
| R3 | 270Ω |
| R4 | 8 x 150Ω SIL RS Part No. 140-215 |
| R5 | 150Ω |
| R6 | 47Ω 1/8 watt |
| R7 | 8 x 150R SIL RS Part No. 140-215 |
| R8 | 270Ω |
| R9 | 150Ω |
| R10 | 470Ω |
| R11 | 1K |
| R12 | 2K |
| R13 | 39Ω |
| R14 | 75Ω |
| R15 | 24Ω |

RV1 1K CERMET 20 TURN

## CAPACITORS

| | |
|---|---|
| C1 | 0.1µF Encapsulated Chip |
| C2 | 47µF 16v Electrolytic |
| C3 | 10nF Encapsulated Chip |
| C4 | 10nF Encapsulated Chip |
| C5 | 47µF 16v Electrolytic |
| C6 | 10nF Encapsulated Chip |
| C7 | 0.1µF Encapsulated Chip |
| C8 | 10nF Encapsulated Chip |
| C9 | 10nF Encapsulated Chip |

## SEMICONDUCTORS

| | |
|---|---|
| IC1 | SP97618(Plessey) |
| IC2 | LM113 or LM313 |
| D1 | 1N4148 or similar |

## MISCELLANEOUS

| | |
|---|---|
| S1 | 8-way SPST DIL Switch |
| S2 | 6-way SPST DIL Switch |
| 1-off | 12-way Unshrouded Header |
| 2-off | Sub-Vis Connectors |
| 4-off | Vero Pins |
| 2-off | Micro Shunts |
| 4-off | Rubber Feet |

## RELATED DOCUMENTS

**Low Cost Video Speed A-D/D-A**
**(Publication No.P.S. 1993) (Plessey Semiconductors)**
**High Speed Data Products Integrated Circuits Handbook**
**(Publication No.P.S. 1989) (Plessey Semiconductors)**
**A Complete 100MHz 8-Bit ADC/DAC Evaluation System**
**(Publication No.P.S.2048)**

## ACKNOWLEDGEMENTS

DM/DP-87
Plessey Design UK
Plessey Applications UK
Plessey Applications California USA

## REFERENCES

Dynamic Performance Testing of A to D Converters -
Hewlett Packard Product Note 5180A-2.

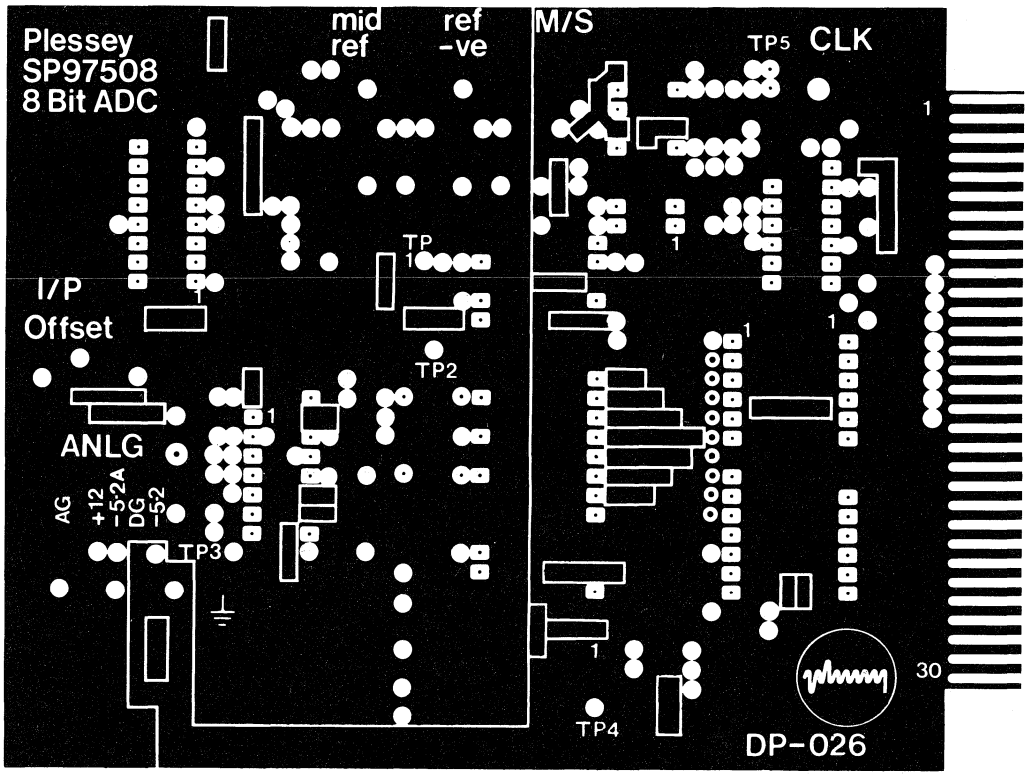



*Fig.11(a) AP9004 ADC board, ground plane*

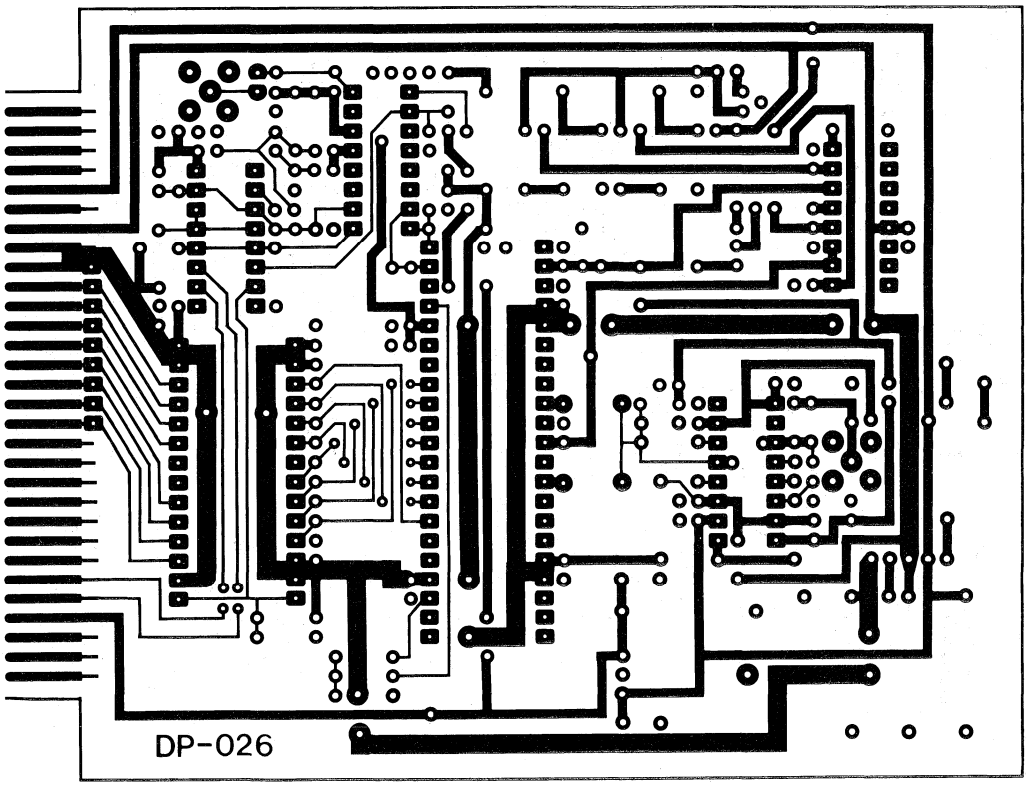



*Fig.11(b) AP9004 ADC board, track side*

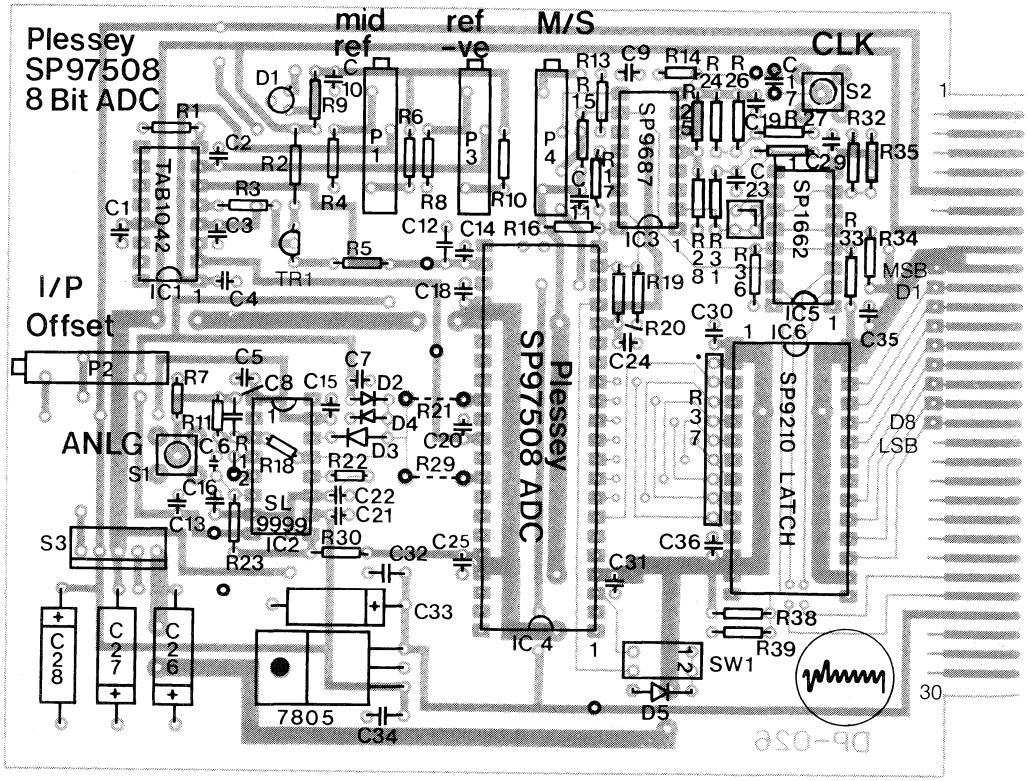



*Fig.11(c) AP9004 ADC board, component layout*

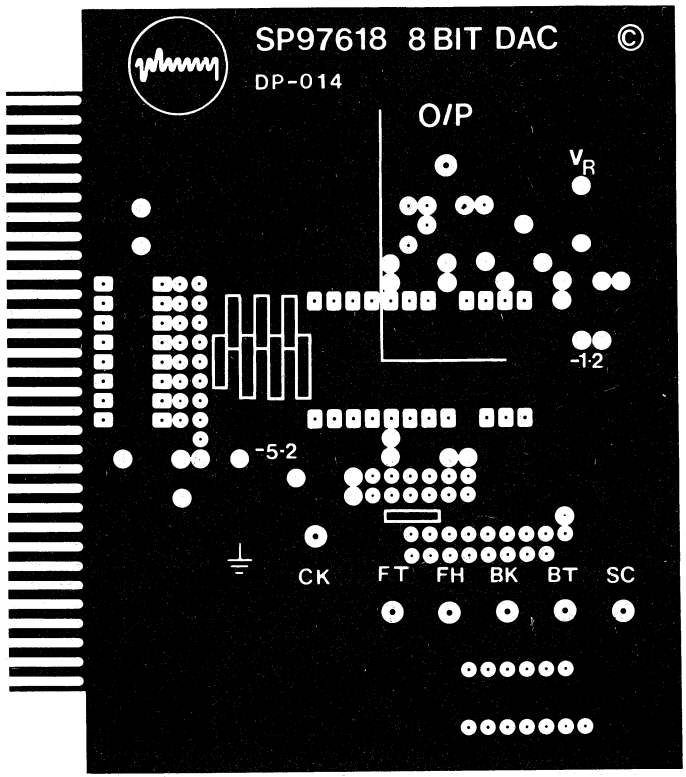



*Fig.12(a) AP9005 DAC board, ground plane*

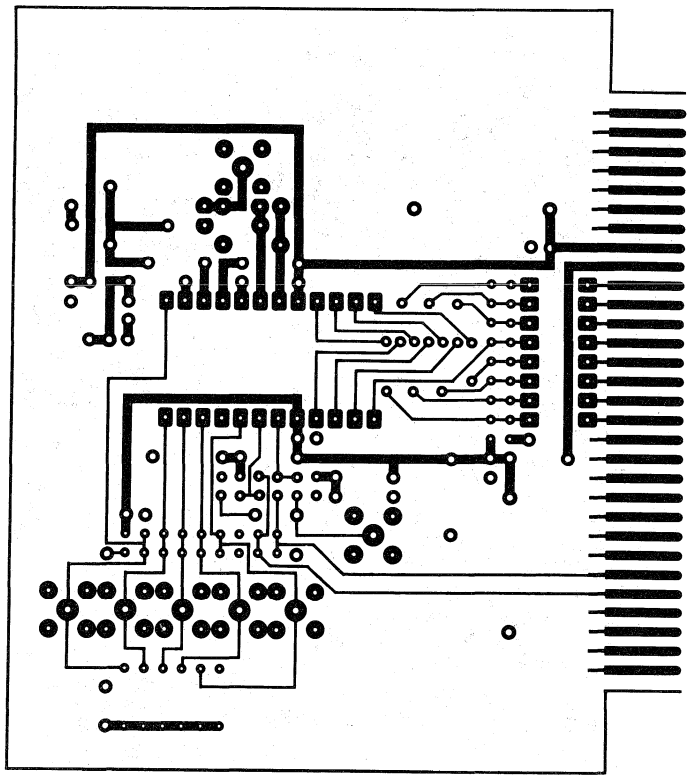


*Fig.12(b) AP9005 DAC board, track side*

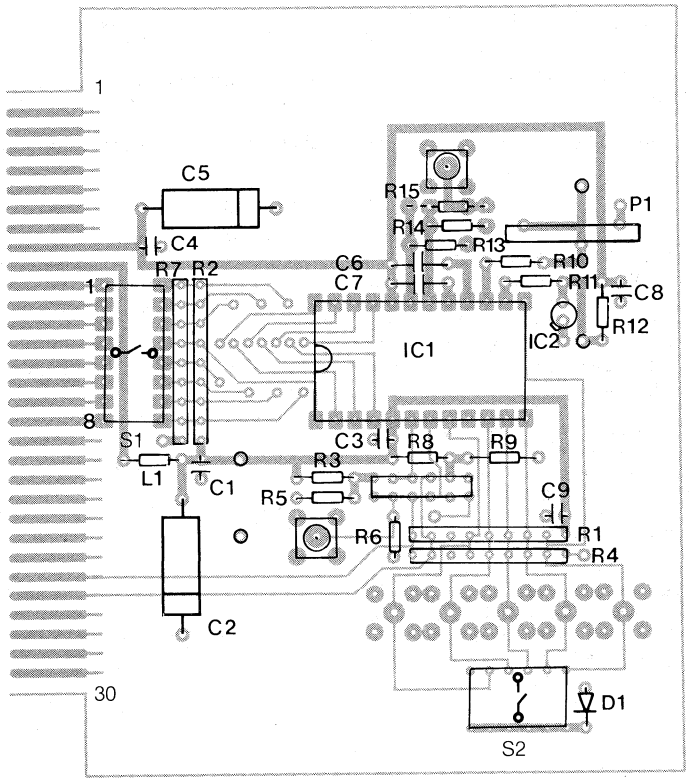



*Fig.12(c) AP9005 DAC board, component layout*

# High Speed ADC Bit Error Rate Measurement — AN65

**This application note describes a measurement system which can be used to measure the number of bit errors per second produced by a high speed ADC. The technique can be used at low frequency or with full amplitude near Nyquist input conditions (50MHz).**

**This application note should be read in conjunction with '100MHz ADC/DAC evaluation system for the SP97508 ADC and SP97618 DAC'.**

## INTRODUCTION

It has been generally assumed that the only way to make accurate ADC bit error rate measurements was to use a very large high speed memory to capture vast amounts of data. Then a computer would be needed to sift through this data, to find and count the number of bit errors. This method becomes impractical at very high data rates with today's ADCs, as the size of high speed memory required to capture the data becomes too large and costly.

The measurement technique described here, needs neither the computer or memory, yet it gives a readout of errors per second *in real time.* This is achieved using standard lab equipment and the Plessey application board AP9004 (SP97508 ADC) plus two AP9005s (SP97618 DAC).

## BASIC THEORY OF THE TECHNIQUE

Before examining this system at near Nyquist input frequency the explanation can be simplified by first describing a low input frequency system. Then it can be shown how this simple system can be modified to measure bit errors with a full amplitude near Nyquist input.

### Low Speed System

If the slew rate of the input signal to the ADC under test is set to a very low frequency (say, f') it is certain that at a clock frequency of $f_c$ at least one sample would be taken between each of the comparators within the flash ADC. The resulting reconstructed DAC output would then show all $2^N$ levels.

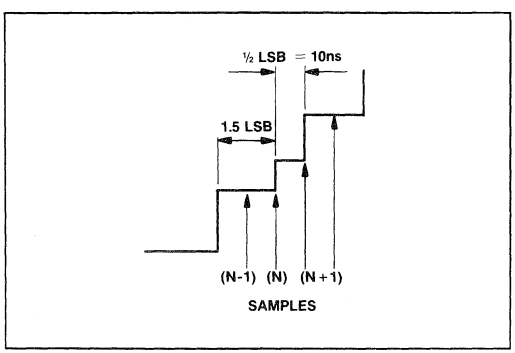



*Fig.1*

If f' is calculated for a specific $f_c$ and N (number of bits) it can be ensured that the data from the ADC will never change by more than one LSB between any two successive samples. See Fig.1.

Therefore, at the output of the ADC, (DATA N) - (DATA (N-1)) $\leq$ 1 LSB.

This rule will only break down if a code error or a bit error occurs. It will be discussed later how to count the resulting error codes, but first to set up this system the value of f' must be calculated.

### Calculation of f'

From Fig.1 a general formula can be derived for f' in terms of N, $f_c$ and the minimum differential linearity error ($e_{min}$).

To do this must first be calculated the maximum rate of change of voltage which gives one LSB change at the output of the ADC, each time we take a sample.

$$\text{The rate of change of the input is } \frac{\Delta V}{\Delta t}$$

The voltage at the input for a 1 LSB change at the output is:

$$\Delta V = V\,p\text{-}p\ \frac{1}{2^N - 1} \quad N = \text{number of bits}$$

Now to take into account the minimum differential linearity:

$$\Delta V = \frac{V\,p\text{-}p}{2^N - 1}\ (e_{min})$$

$\Delta t$ is simply $\frac{1}{f_c}$ ie, one clock cycle

$$\text{Therefore } \frac{\Delta V}{\Delta t} = \frac{\frac{V\,p\text{-}p}{2^N - 1}\ (e_{min})}{\frac{1}{f_c}} = \frac{V\,p\text{-}p\ f_c\ (e_{min})}{2^N - 1} \quad \ldots (1)$$

It is now possible to calculate the sinusoidal input frequency f' which gives this maximum rate of change of input voltage.

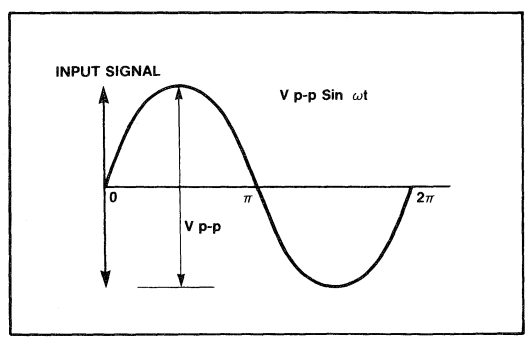



*Fig.2*

The maximum rate of change of a sinewave is when $\omega t = 0$, $\pi$ or $2\pi$.

$$\text{ie. when } \frac{dV}{dt}(V\,p\text{-}p\ \sin\ \omega t) = 0, \pi \text{ or } 2\pi$$

$$\text{Now } \frac{dV}{dt} V\,p\text{-}p\ \sin\ \omega t = V\,p\text{-}p\ \omega\ \cos\ \omega t$$

Therefore as $|\cos\ \omega t| = 1$ for $\omega t = 0, \pi$ or $2\pi$, the maximum rate of change must be given by:

$$V\,p\text{-}p\ \omega \times 1$$

$$\text{Therefore } \frac{dV}{dt} \text{ max } = V\ p\text{-}p\ 2\pi f' \qquad \ldots (2)$$

$$\text{Hence, when } \frac{dV}{dt} \text{ max } = \frac{\Delta V}{\Delta t}$$

The required conditions are satisified. ie. when equation (1) = equation (2).

$$\frac{V\ p\text{-}p\ f_c\ (e_{min})}{2^N - 1} \qquad V\ p\text{-}p\ 2\pi f'$$

Cancelling V p-p and rearranging for f' gives:

$$f' = \frac{f_c\ (e_{min})}{2\pi\ (2^N - 1)} \qquad \ldots (3)$$

As we now have a general formula for the maximum input frequency at which the ADC outputs only change by 1 LSB, we can calculate f' for our 100MHz 8-bit device (SP97508) ($e_{min}$) = ½ LSB.

$$f' = \frac{100MHz\ 0.5\ LSB}{2\pi\ (2^8 - 1)}$$

$$\text{Therefore } f' = \frac{100MHz\ 0.5}{1602}$$

$$f' = 31.2kHz$$

The analog input must therefore be set to less than 31.2kHz to ensure that the output code only changes by 1 LSB or less between each sample. A safety factor can be applied to this frequency but we must not go too low as we need to measure errors on as many levels as possible within each second (20kHz is a suitable low frequency).

## COUNTING THE BIT ERRORS

Before proceeding with any bit error measurement we must first make sure that the device is not producing code errors.

This is easily done by viewing the reconstructed 20kHz sinewave output on a scope. As code errors occur on every cycle they are easily visible on an 8-bit device.

As stated previously, a bit error has occurred if the difference between any two adjacent codes is greater than I LSB. We can therefore detect the occurence of any bit error by subtracting data (N-1) from data N and then looking for a result greater than one.

This system delays the 8 bits output by one clock cycle and then sums this with the complement of the original data, thus producing the difference between data N and data N-1. If the LSB is ignored the resulting 7 bits should remain at zero unless a bit error occurs. Bit errors are detected by the OR gate. These pulses can then be counted using a frequency counter yielding a result in errors per second.

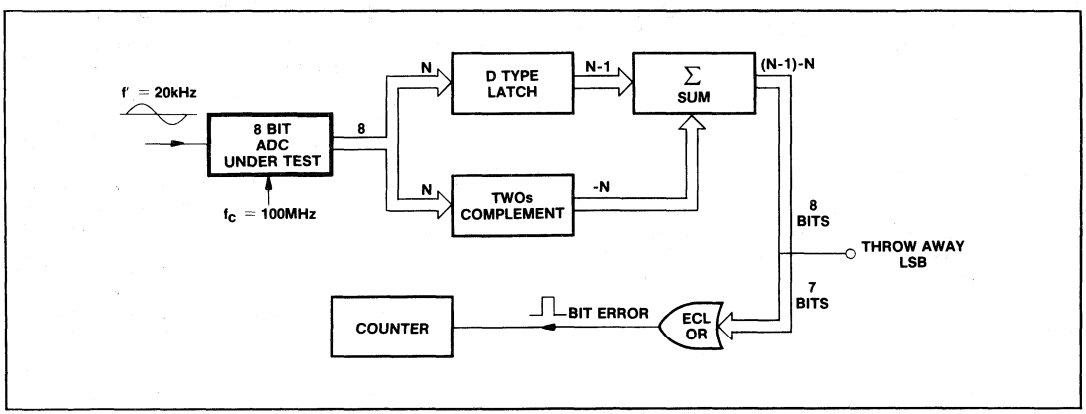



*Fig.3*

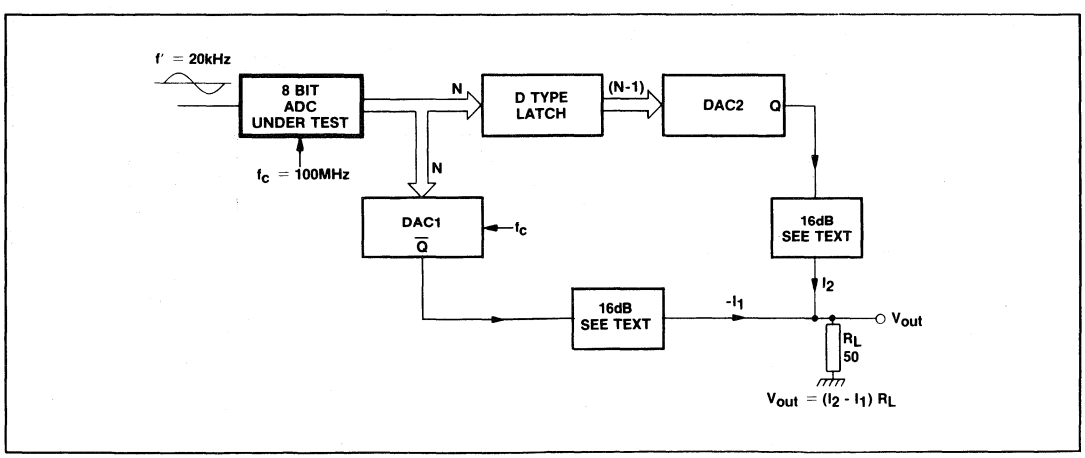
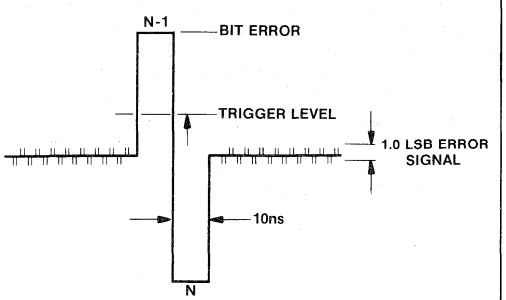



*Fig.4*

### Analog Technique

This analog technique is an alternative to the digital subtraction method. Digital subtraction can be very difficult at 100MHz and above. (However it can be ideally suited to production testing.) The analog technique now described takes advantage of the very high speed latched DACs now available (SP97618 or SP98608). These 200MHz or 400MHz DACs can be used to reconstruct the data. The subtraction can then be performed very simply by summing the true and inverse analog DAC output currents into a 50Ω load (Fig.4).

$V_{out}$ will be a small error voltage signal 1 LSB high, unless of course a bit error occurs, in which case a pulse is produced with an amplitude proportional to the erroneous code the error has caused. The pulse will also be seen on the next cycle of the clock, due to the one cycle delay in the latch. On this second cycle a negative going voltage will be seen.




NOTE: This waveform can only be seen with full intensity on the scope and a very bad ADC in circuit, as it may only trigger the scope 1-200 times per second.

*Fig.5*

Counting these bit errors is very simple as most scopes produce a trigger output signal from the rear panel. This can be connected directly to a counter. The scope trigger level can then be adjusted so that the normal 1 LSB error is ignored. The scope trigger must be set to DC and normal with the timebase at about 100ns/div.

The system can be calibrated to look for bit errors greater than a chosen number of bits. This is done by switching off the LSBs of DAC1 to produce the error amplitude above which bit errors are to be counted. The scope trigger is then set so that triggering is just lost. The LSBs can then be reintroduced into DAC1 and the errors counted on the counter as above. This technique is most useful when small code errors are present as these need to be ignored to measure the remaining bit errors.

### Attenuators

These are placed in the path of the current flowing to the summation resistor, and provide a cleaner signal on the scope. This is due to the fact that most current output DACs are very capacitance sensitive. The attenuators reduce the amount of scope input capacitance seen by the DAC outputs. The settling times of the DACs are therefore much improved.

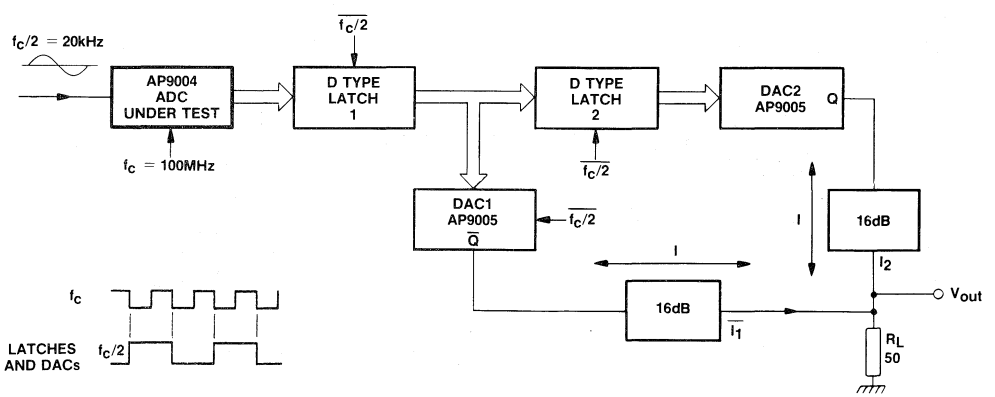
## HIGH SPEED INPUT BIT ERROR MEASUREMENTS

### Measurement of Bit Errors with Full Amplitude near Nyquist Input Signals

The bit error rate of an ADC is not only dependent on the clock mark-to-space ratio and temperature, but also on the frequency of the anlog inmput, and of course the input amplitude.

The definitive test for bit errors within an ADC would therefore be with a full ampltiude near Nyquist input signal at maximum ambient temperature and 1:1 clock mark-to-space ratio.

This measurement can be achieved by adding a simple D type latch (clocked at $f_c/2$) to the output of the ADC and again we can follow the previous analog measurement technique to measure the bit error rate, under high frequency input conditions.




The length of cable from each DAC to the load should be adjusted for minimum glitches on $V_{out}$.

*Fig.6*

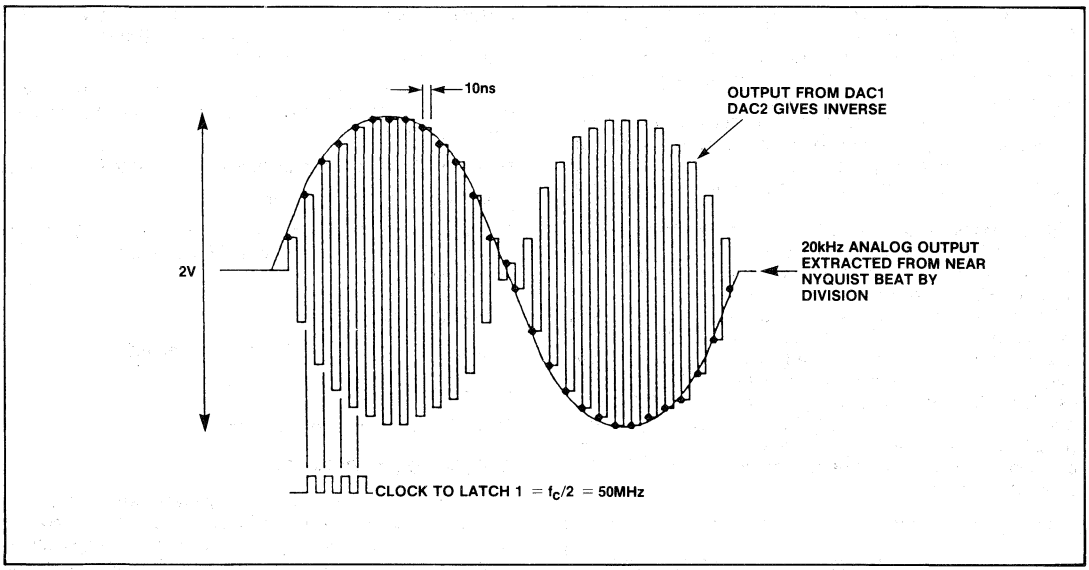



*Fig.7*

D type latch 1 will now divide the output data. This means that every other data word is discarded. The reason for doing what seems to be a waste of good output information is to extract the envelope from the Nyquist beat pattern (see Fig.7).

If the analog input to this system is set correctly (f'a) we can again be confident that even though the input frequency is at near Nyquist, there will be only one LSB change at the output of the ADC, but this time on every other clock cycle.

The analog input frequency must be within f' of Nyquist:

$$f'a = \frac{f_c}{2} \pm f'$$

In general the lower of the two resulting frequencies is chosen.

$$f'a = \frac{f_c}{2} - f'$$

The general expression for the near Nyquist input frequency that will produce only one LSB change every other clock cycle is:

$$f'a = \frac{f_c}{2} - f'$$

$$f'a = \frac{f_c}{2} - \frac{f_c\,(e_{min})}{2\pi\,(2^N - 1)}$$

$$\text{Therefore } f'a = \frac{f_c}{2}\left(1 - \frac{(e_{min})}{\pi\,(2^N - 1)}\right) \quad \ldots (4)$$

Where:
- $f_c$ = clock frequency
- $N$ = number of bits
- $f'a$ = analog input frequency
- $(e_{min})$ = minimum differential error

We can now determine this input frequency for the 100MHz 8-bit device.

$$f'a = \frac{100MHz}{2}\left(1 - \frac{0.5}{\pi\,(2^8 - 1)}\right) = 49.9687MHz$$

The two analog waveforms from each DAC are summed in $R_L$ to produce the small 1 LSB error signal as before. The only difference between this and the low speed test is that due to the fact that the ADC output was divided by 2. The displayed error count must now be multiplied by 2.

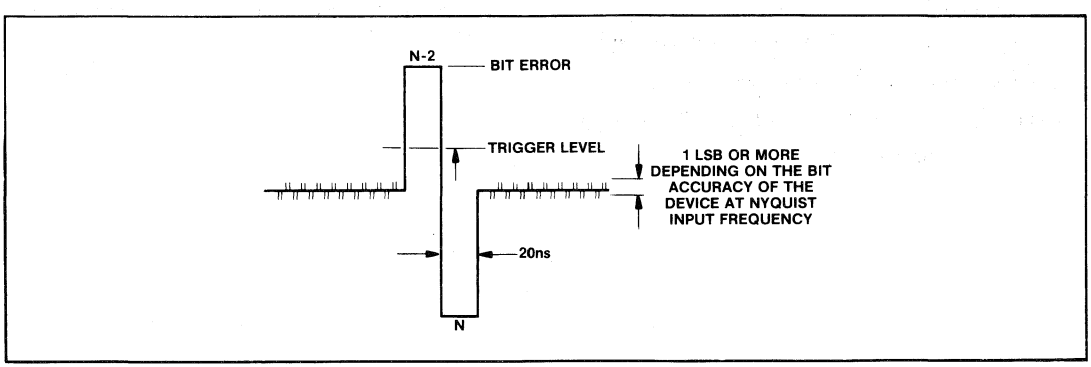



*Fig.8*

It is wise to add a small safety margin to this input frequency, as some competitors products will show significant deterioration of accuracy with input frequency. A frequency of 49.98MHz was chosen as a standard input frequency for tests on the SP97508.

The results from the counter (connected to the trigger outputs of scope) will be in counts per second. As the total number of operations per second is $10^8$ ($f_c$ = 100MHz) a result of 4 counts per second would be equal to 4 x 2 in $10^8$ ie. 8 in $10^8$ bit errors.

It is possible when using the high speed technique to simply switch the analog input from 49.98MHz to 20kHz to find the low frequency error rate (do not forget to multiply the result by x2 if the division is not removed).

The system timing allows both the data capture time and mark space ratio to be adjusted without affecting the measurement technique. These adjustments can be made to the system by connecting the HP8640 (used as a master oscillator) to a HP8082 pulse generator. The HP8640 also drives the SP9131 divide by 2 circuit. The pulse generator (HP8082) drives the clock of the ADC via a SP8687 comparator which is already present on the AP9004 applications board.

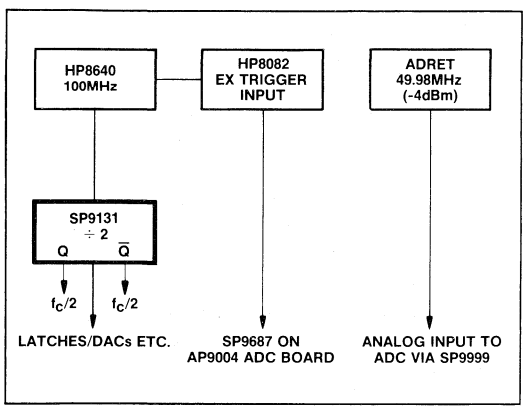



*Fig.9*

## EQUIPMENT AND SETTINGS FOR FULL NYQUIST BEAT BIT ERROR RATE TEST

**HP8640 or equalivent** (master system clock)
+10dBm, 100.000MHz, AM = off, FM = off, RF = on.

**HP8082** (clock conditioning for ADC, driven from 8640)
Ext trig, slope/polarity = pos, rate = 100m 10m ⟲
← knob position.
Pulse delay = 2n-5n ⟲, Pulse width = 5n-50n ⟲
Trans time = 1n-5n ⟲ ⟲, Amplitude (into 50Ω) = 1.0-2.0 both, vernier = ⟲, offset = on ⟲, $\overline{\text{use output}}$ (right), neg pos = pos, normal compl = compl.

**ADRET** or equivalent (analog input to ADC. Another HP8640 could be used). 49.98MHz, -4.98MHz, -4dBm (adjust to full amplitude reconstructed output).

**Counter** (to count triggers ie. bit errors from external trigger out of scope). Philips M6671 was used with all buttons out apart from power.

Measuring time = 1 second, hold off = 0, set to freq A, use A input, trigger ( ⟲ Pushed in).

**Scope** (any 300MHz scope with trigger out), 5mV/DIV. AC coupled (full BW), trig = normal DC -ve slope time base 100ns/div.

### Power Supplies

+5V at 220mA, -5.2V at 1.52A, +12V at 108mA.

### Attenuator

Two 50Ω attenuators set to 16dB.

## CONCLUDING REMARKS

We have shown that an accurate and consistent measurement of bit errors can be achieved using general lab equipment, combined with standard applications boards, two latches and a little ingenuity. This technique can be used even when the ADC is performing under the most severe input and clock conditions.

The major advantage of this method is that the result from the counter is in real time. Therefore it is much easier to see the effects of small parametric changes to the setup of the ADC on the bit error rate result. This allows easy optimisation of all the critical factors which effect the bit error rate within a system.

Measurements have been made on standard products versus competitive products. Without exception the SP97508 has peformed better than the competitive products at high analog input frequency and voltage. Ths is simply due to the higher input analog bandwidth of the device. This extra speed yields comparators that can regenerate their full output drive quickly. This in turn greatly reduces the probability of metastable states, and therefore reduces the bit error rate, under all conditions. When the mark-to-space ratio is adjusted to give a longer period for the input comparators to regenerate a full output, the bit error rate from the ADC is improved still further, in all devices evaluated so far. The optimum mark-to-space ratio for the SP97508 was found to be 7ns - 3ns.

We realise the effects of bit errors on systems such as digitised scopes, multi quadrant transmission systems, radar systems, video printers etc. It is hoped that this applications note will provide a quick and effective method, for the evaluation and comparison of this important device parameter.

# A Complete 100MHz A/D-D/A Evaluation System

*(For information only – currently being updated)*

**The AP9001 evaluation board is a complete 6 bit 100MHz A to D system. The resulting low external component count can be seen easily when comparing the SP9756 with other solutions. The reduction in external component count is possible because the device includes a clock driver stage, band gap reference, output D-type latch and a reference chain.**

**Each individual application of the ADC may require different optimisation of parameters; this board has been designed in a general manner, yet little else should be required to meet even the most precise 100MHz systems.**

**The SP9756 is a 6-bit flash ECL analog-to-digital converter. It incorporates 64 individual comparators, a clock driver circuit, reference chain and a D-type output latch. This flash ADC is capable of sampling in excess of 110MHz, with a wide analog bandwidth and good dynamic performance.**

**A choice of accuracy is available: the accuracy of the SP9756-8 is typically ± ⅛ LSB at 2V input and therefore it is ideally suited for use in systems that incorporate expansion to higher resolutions. Alternatively the SP9756-6 is guaranteed to be accurate to ± ½ LSB for inputs between 1V and 2V in cost conscious designs.**

*(NOTE: Since publication, the TAB1042, SP9687, SP9210 and SP9768 have been made osolete. In addition, the SP9756 has been superseded by the SP97506)*

## THE EVALUATION SYSTEM - AP9003

Included in the evaluation system are:- ADC board (Fig.1), a length of 100Ω twisted pair and the SP9768 DAC applications board (Fig.2). The twisted pair shows the effectiveness of the SP9756 output latch and enables the user to interface easily with other digital circuitry. The D-A evaluation board provides a simple method of evaluating the all-important analog bandwidth performance of the ADC. It is suggested that, near Nyquist - and even near clock - beats are viewed at 100MHz sample to demonstrate the wide analog bandwidth of the SP9756 (see Figs. 14, 15 and 16).

The ADC board (AP9001) comprises one SP9756 (6-bit ADC), one TAB1042 (quad op.amp), one SP9687 (dual comparator) and one RS7805 5V regulator.

### Evaluation Boards

In general, the performance of a high speed ADC can be greatly affected by the circuit board ground plane layout and associated component placements. Completed ADC and DAC boards with connecting loom are therefore available for evaluation and educational use. The items listed below can be ordered from our Customer Service department.

| Item | Description |
|---|---|
| **AP9001** | Complete ADC board and data |
| **AP9002** | Complete DAC board and data |
| **AP9003** | Complete ADC, DAC and connecting loom with data (recommended system) |

*Evaluation systems*

### Power Supplies

The evaluation system requires external -5.2V and ±12V supplies. A +5V supply is also required but this is provided from the +12V by an RS7805 regulator. For convenience all power supplies have been taken through the edge connector to supply the DAC evaluation board.

| Supply | AP9001 ADC board | AP9003 ADC & DAC system |
|---|---|---|
| -5.2V | 240mA | 660mA |
| +12V | 90mA | 90mA |
| -12V | 90mA | 90mA |

*Table 1 Power supply currents*

The current taken from the -5.2V supply increases to 660mA when the DAC board is connected, due to the extra current taken by the line termination and device supplies.

### Analog Input to the Board

The analog input is fed directly to the SP9756 and is terminated by R14 = 47Ω. Socket pins are provided for AC or DC coupling. An offset can be applied by varying RV2 (see Fig.3).

The source impedance should be 25Ω, certainly no higher than 50Ω (see Fig.4 for device input impedance).

Ideally the reference should be set to accept an analog input of 2V p-p with its center offset by -1V. The range of this offset is approximately +1V to -1.2V.

### Clock Input to the Board (Fig.5)

The SP9756 has an on-chip differential clock driver which allows the device to be driven directly from an ECL source. To aid interfacing to the applications board a comparator has been added. This allows a sinewave oscillator to be used to clock the device. An offset provided by RV4 can be adjusted for AC-coupled inputs or adjusted for an input trip level of -1.28V for ECL signals.

RV4 can also be used with a DC-coupled sinewave input to vary mark/space ratios when experimenting at clock frequencies above 130MHz.

A signal generator with low frequency jitter should be used that is capable of driving the board's 50Ω termination.

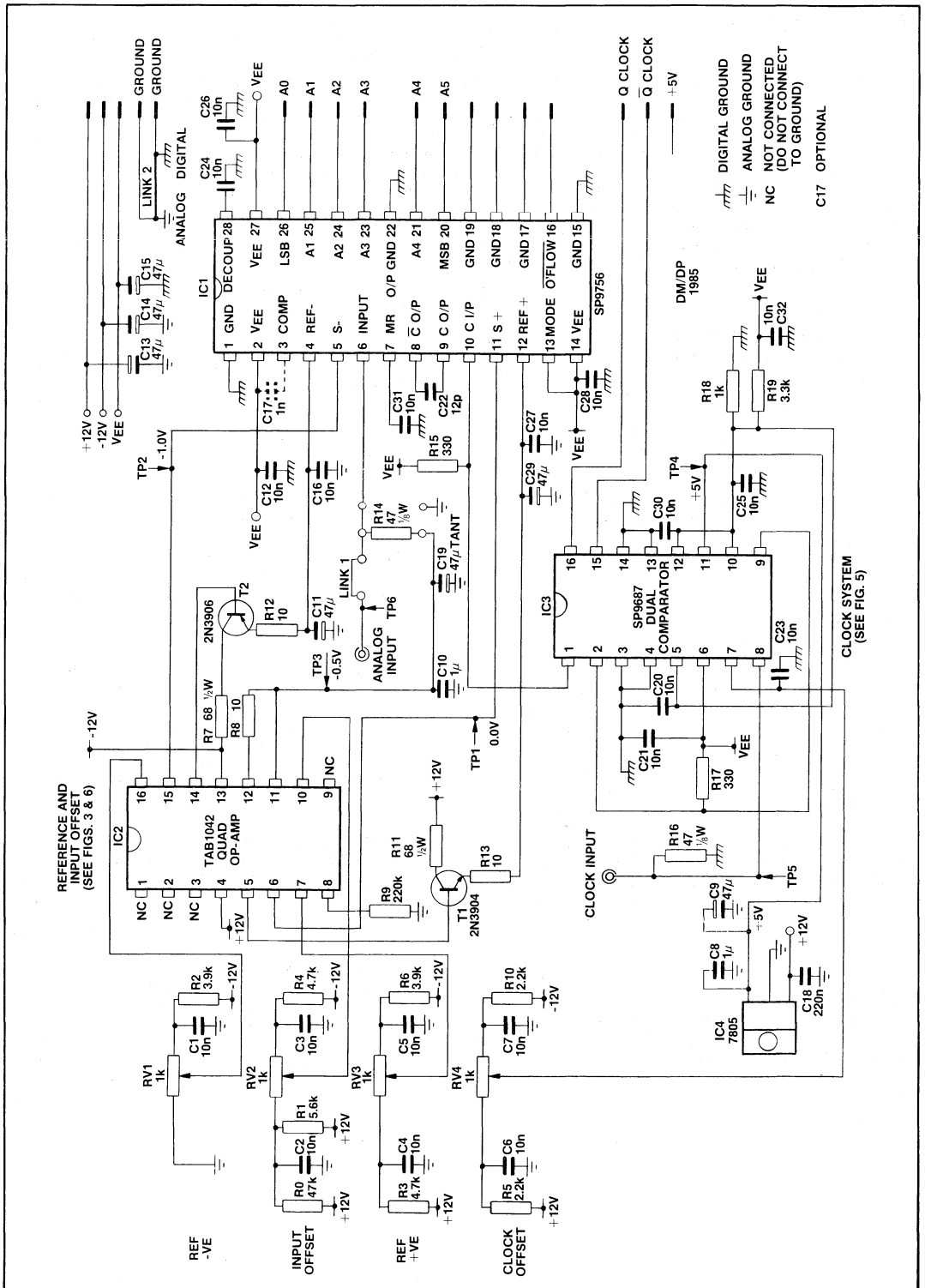
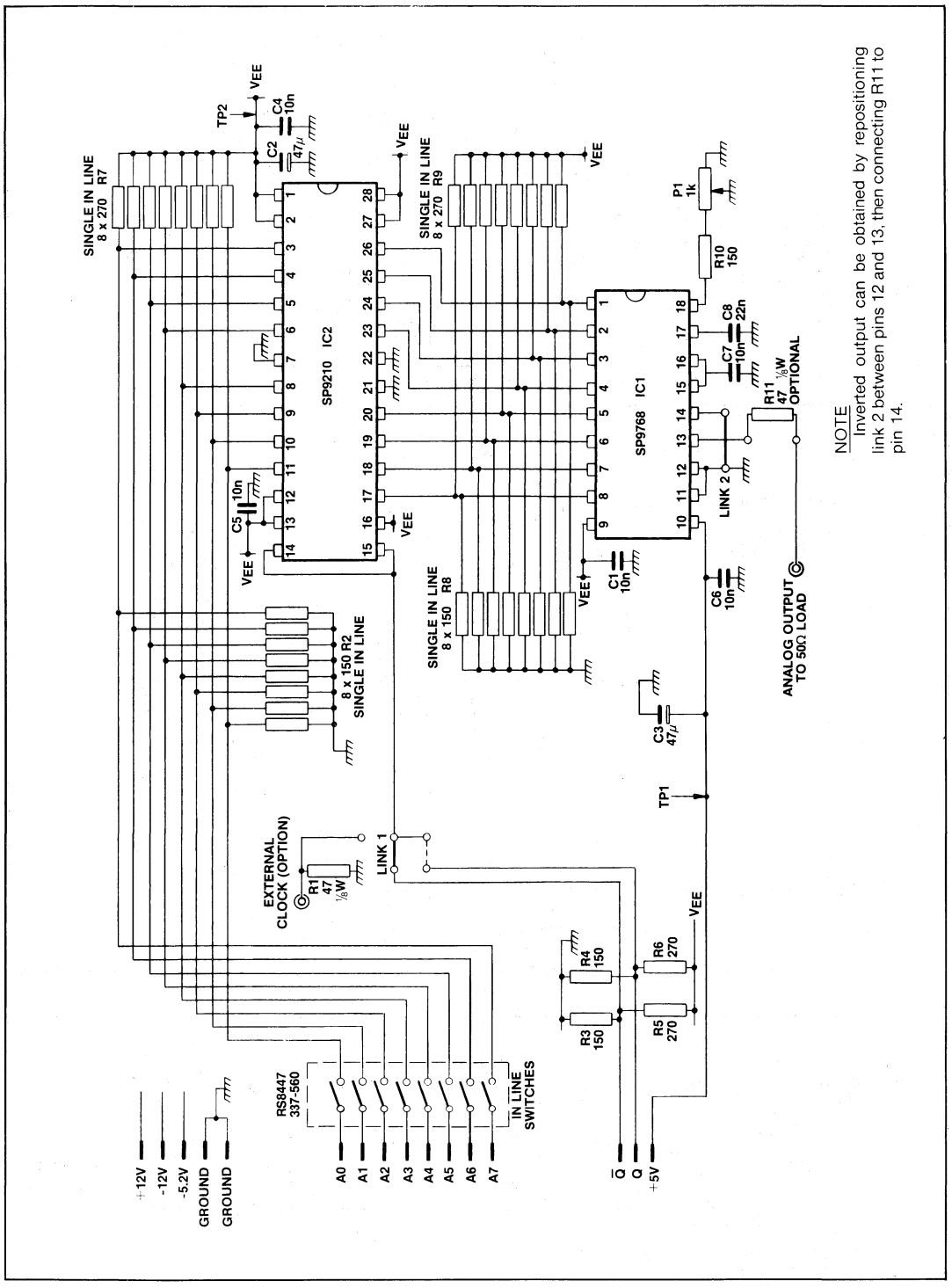



*Fig.1 SP9756 100MHz 6-bit ADC evaluation board - AP9001*




NOTE
Inverted output can be obtained by repositioning link 2 between pins 12 and 13, then connecting R11 to pin 14.

*Fig.2 SP9768 8-bit DAC board - AP9002*

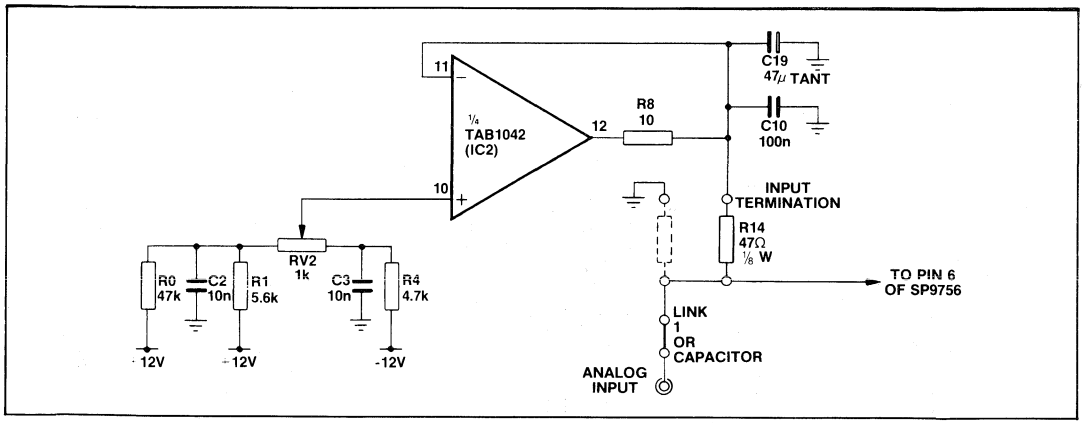



*Fig.3 Input offset*

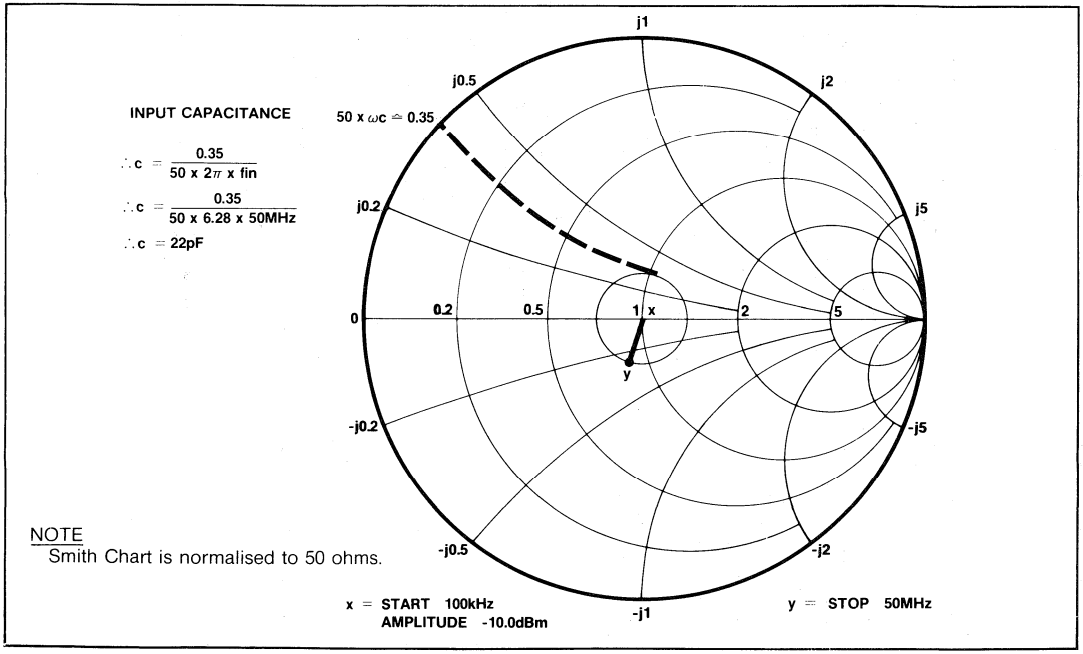



*Fig.4 Analog input to board*

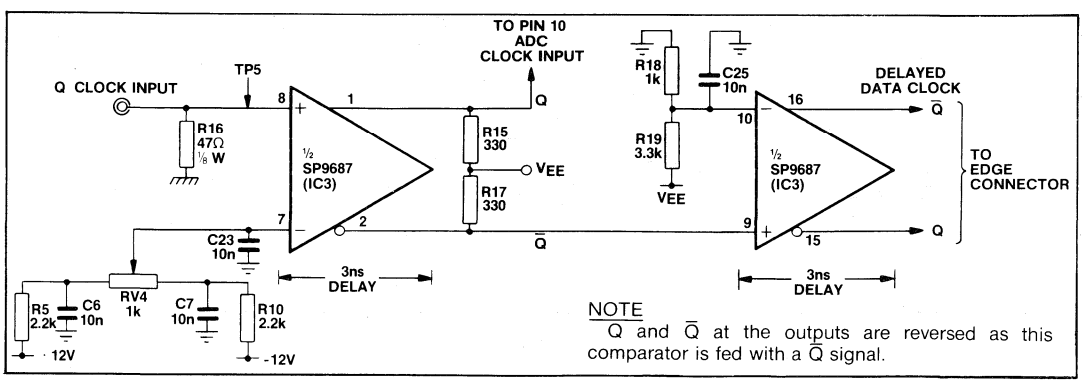



*Fig.5 Clock system*

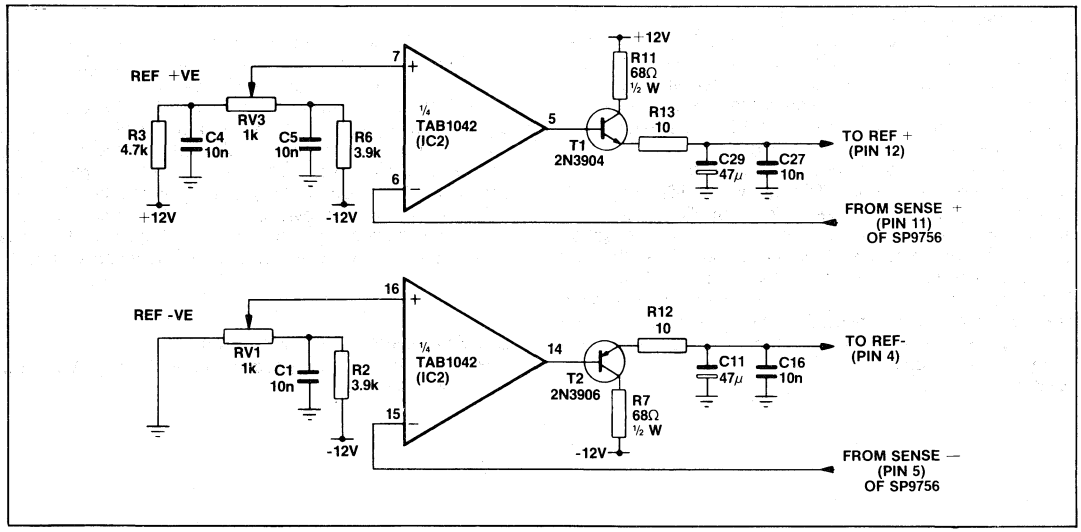



*Fig.6 Reference setting*

## Reference Settings

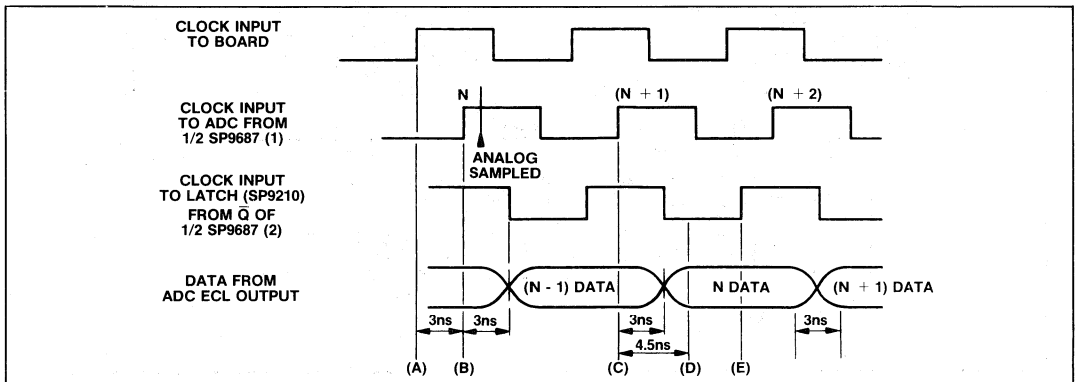
The SP9756 incorporates optional sense outputs (pins 5 and 11) at each end of the reference chain. These allow the reference voltages to be set with precision. The sense outputs permit Kelvin connections to be used to force the precise voltage to the end reference resistors, thus avoiding errors normally caused by bond wire resistances. RV3 is used to set the positive reference voltage via one of the TAB1042 amplifiers. For optimum performance, RV3 should be adjusted until the positive sense voltage (REF +) = 0.0V. This potentiometer will adjust the REF+ from +0.6V to -2.2V. RV1 is used to set the negative reference voltage via another amplifier in the TAB1042. For optimum performance RV1 should be adjusted until the sense negative voltage = -2.0V. RV1 will adjust the REF- from 0V to 2.5V. Experiments an be performed on the ADC by adjusting the voltage across the reference chain from 0.5V to 2.0V. Optimum performance will be obtained using a reference voltage of 2.0V.

## Digital Outputs

The digital outputs from the SP9756 are brought directly to the edge connector and should be terminated with 100ohm connected to -2V. This termination can be achieved using the Thevenin equivalent circuit, as demonstrated with the DAC application board.

If direct connection to a logic analyser is necessary then the outputs should be terminated on the ADC board using the holes provided.

Other digital signals going to the edge connector are CARRY OUT Q clock and $\overline{Q}$ clock. The clock outputs from the board have been delayed by 3ns using the propagation delay of 1/2 the SP9687 dual comparator.




(A) POINT IN TIME THAT THE BOARD SEES FIRST RISING EDGE
(B) POINT IN TIME THAT THE SP9756 SAMPLES
(C) POINT IN TIME THAT THE NEXT SAMPLE IS TAKEN
(D) POINT IN TIME THAT THE DATA BECOMES VALID
(E) POINT IN TIME THAT THE DATA IS ACQUIRED INTO THE SP9210 LATCH

NOTES
1. The analog input signal is sampled approximately 1.2ns after point (B).
2. As the ribbon cable connecting the two boards will delay the clock and data by the same amount it has been omitted from the diagram.
3. The fact that all intervals are 3ns is mere coincidence.
4. The tolerance on SP9687 propagation delay is ±1.5ns. The SP9210 setup time is 1.5ns and hold time is 1ns.
5. As 70% of the data is valid no expensive delay line is required.

*Fig.7 SP9756 applications board. Clock timing shown at 100MHz*

### Clock and Data Timing (Fig.7)

The SP9756 accepts standard ECL clock inputs. It then converts them to a differential clock signal used internally. The propagation delay of this internal circuit is approximately 1.2ns, which means that the point that the analog signal is actually sampled is 1.2ns after each rising edge of the clock input to the device.

The clock input to the board is compared to a trip level that can be externally adjusted. This allows an ECL or an AC-coupled signal to be used. The SP9687 dual high speed comparator is used as it combines low propagation delay (3ns) and complementary ECL outputs. The other half of this dual comparator is connected in series with the first. The reason for this is twofold: first it provides reverse isolation (preventing reflected signals interfering with the clock signal to the SP9756) and secondly it provides the 3ns delay needed to position its rising edge in the centre of the valid data period.

This Q signal from the second half of the SP9687 can therefore be used directly to clock the circuit acquiring the digital information from the ADC board.

For single shot applications it is important to note that the digital word corresponding to any sample will be valid at the output 4.5ns after the second rising edge of the clock input i.e. the data out is valid after the n + 1th sample. This is simply due to the output D-type latch within the SP9756.

This D-type latch provides DATA OUT which is valid for 70 % of the clock cycle at 100MHz. This implies that external latch and expensive delay lines can in most applications be omitted.

### Evaluation System Construction

Printed circuit board layouts for the ADC and DAC boards are given in Figs. 8 to 13.

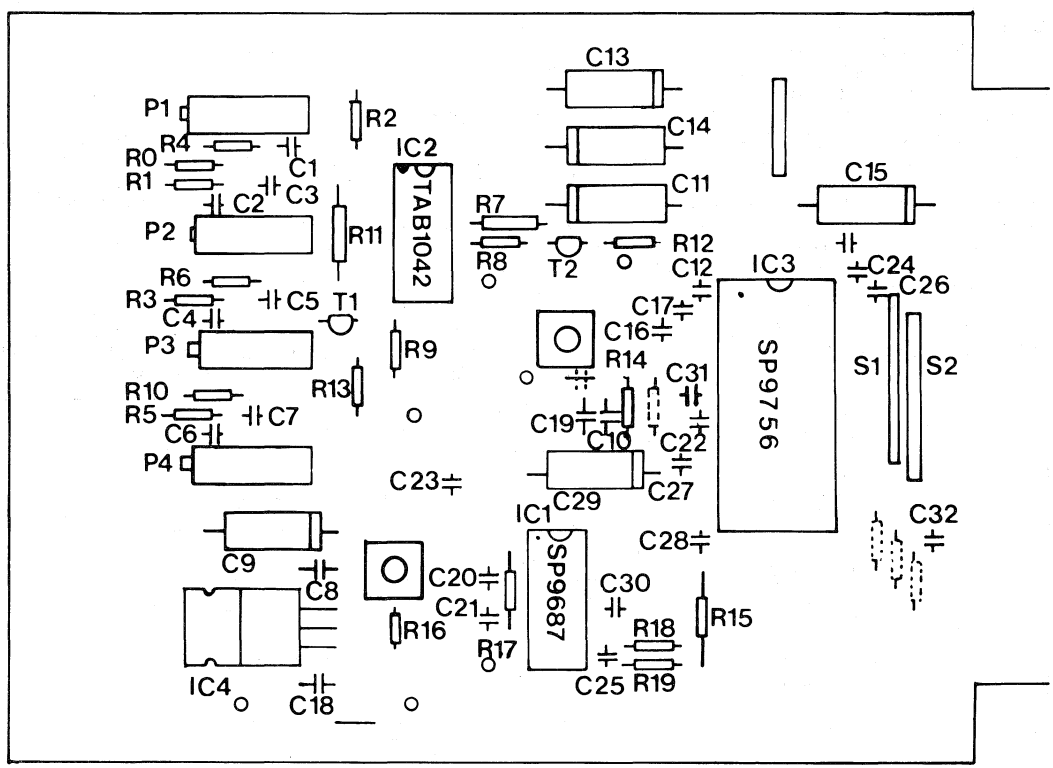



*Fig.8 ADC board, component layout - AP9001*

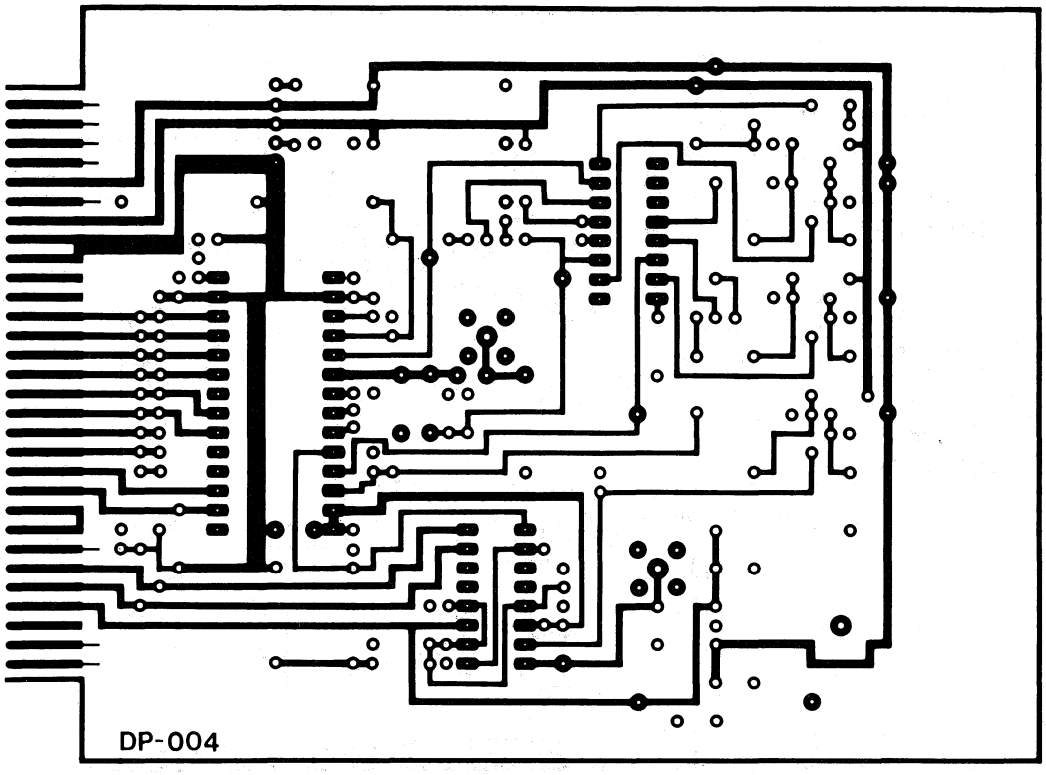



*Fig.9 ADC board, underside (black = copper)*

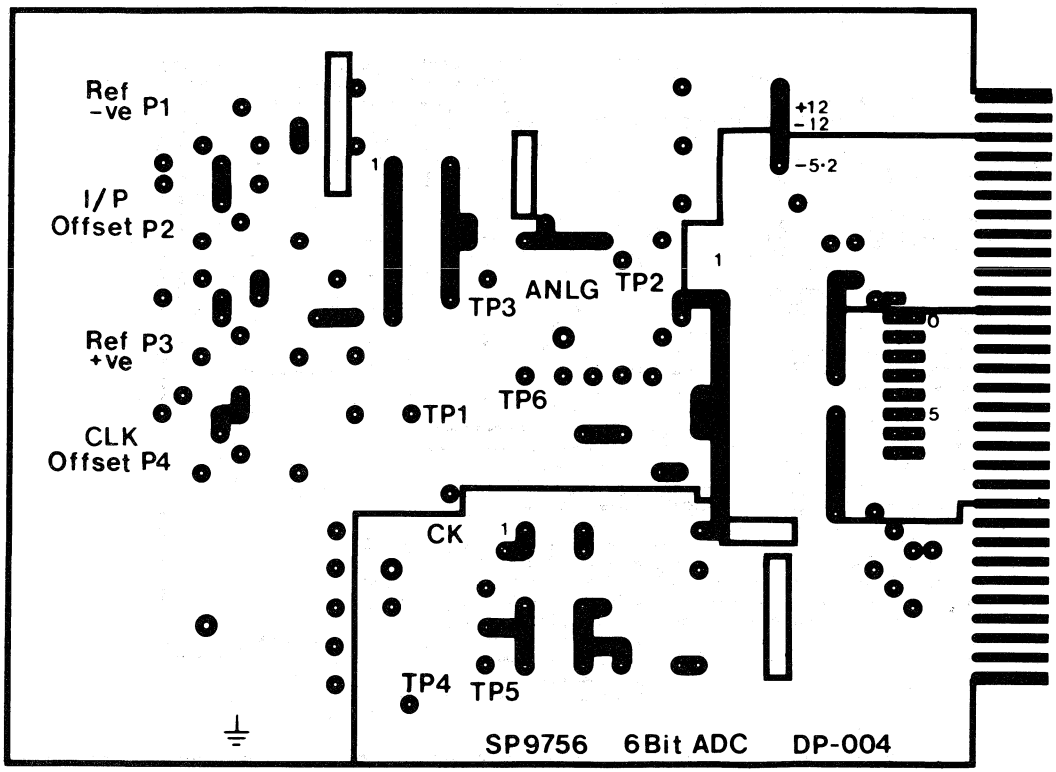



*Fig.10 ADC board, component side (white = copper)*

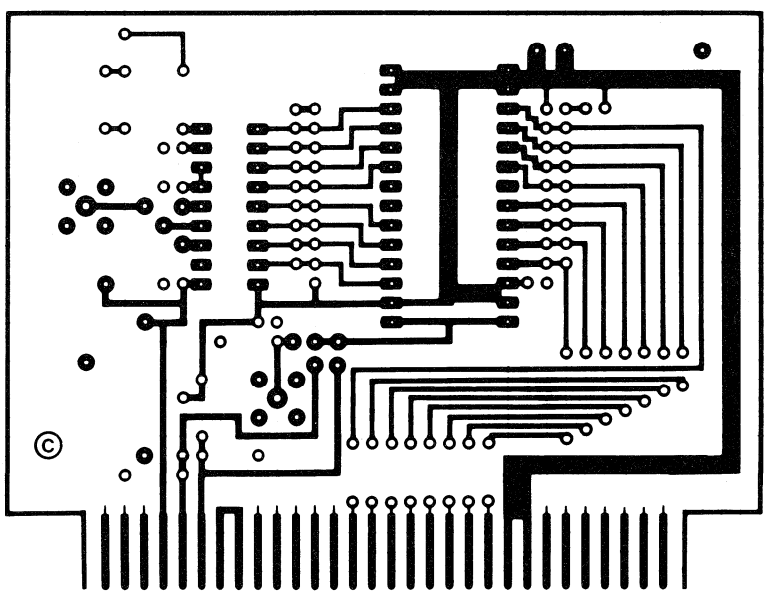



*Fig.11 DAC board, underside (black = copper)*

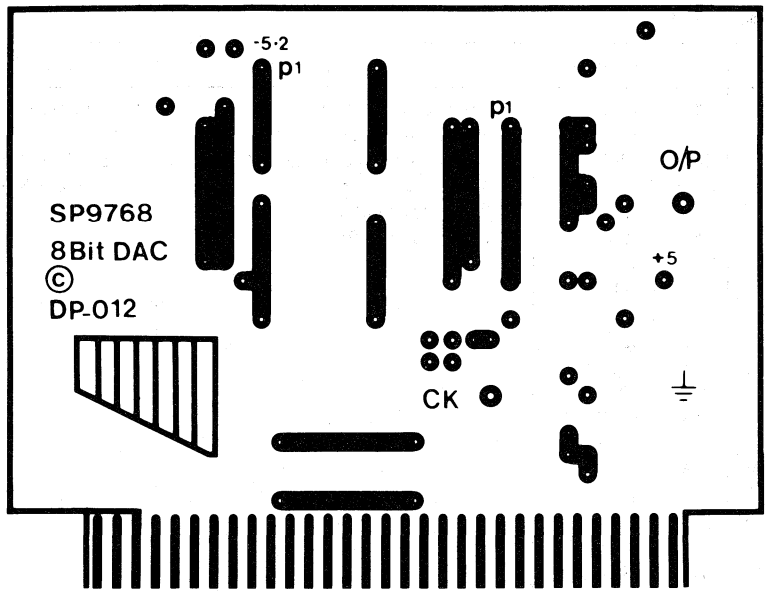



*Fig.12 DAC board, component side (white = copper)*

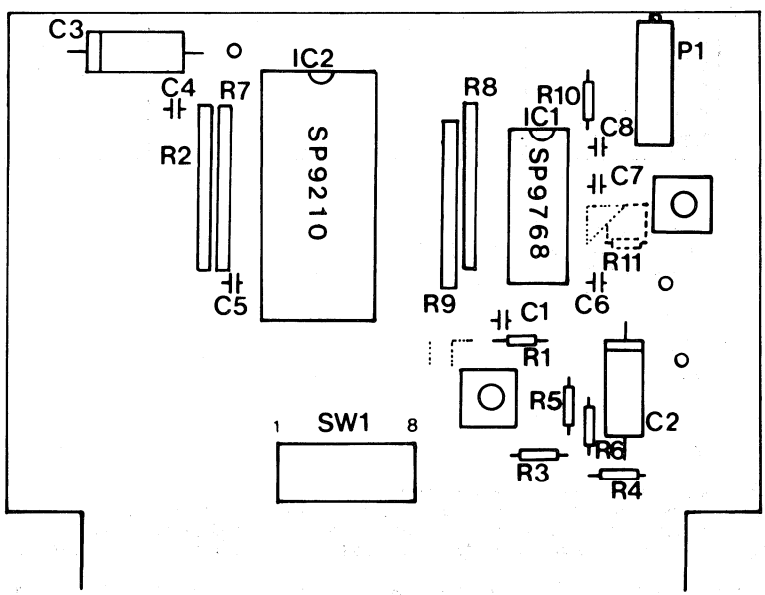
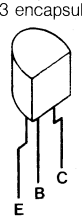



*Fig.13 DAC board, component layout*

## ADC BOARD COMPONENTS

| Resistors | | Capacitors | | Semiconductors | Miscellaneous |
|---|---|---|---|---|---|
| R0 | 47k | C1 | 10nF | IC1 SP9756-6, 6-bit ADC | 2-off sub-vis connectors |
| R1 | 5.6k | C2 | 10nF | IC2 TAB1042 Quad op.amp | 1-off Molex 5-pin connector |
| R2 | 3.9k | C3 | 10nF | IC3 SP9687 Dual comparator | 270Ω SIL x 8 (Note 7) |
| R3 | 4.7k | C4 | 10nF | IC4 7805 5V regulator | 150Ω SIL x 8 (Note 7) |
| R4 | 4.7k | C5 | 10nF | TR1 2N3904 (NPN) | |
| R5 | 2.2k | C6 | 10nF | TR2 2N3906 (PNP) | |
| R6 | 3.9k | C7 | 10nF | | |
| R7 | 68 1/2W | C8 | 1μF | | |
| R8 | 10 | C9 | 47μF | | |
| R9 | 220k | C10 | 1μF | | |
| R10 | 2.2k | C11 | 47μF | | |
| R11 | 68 1/2W | C12 | 10nF | | |
| R12 | 10 | C13 | 47μF | | |
| R13 | 10 | C14 | 47μF | | |
| R14 | 47 1/8W | C15 | 47μF | | |
| R15 | 330 | C16 | 10nF | | |
| R16 | 47 1/8W | C17 | 1nF | | |
| R17 | 330 | C18 | 220nF | | |
| R18 | 1k | C19 | 47μF tant | | |
| R19 | 3.3k | C20 | 10nF | | |
| RV1 | 1k | C21 | 10nF | | |
| RV2 | 1k | C22 | 12pF | | |
| RV3 | 1k | C23 | 10nF | | |
| RV4 | 1k | C24 | 10nF | | |
| RV = | (43P102 TYPE SPECTROL) | C25 | 10nF | | |
| | | C26 | 10nF | | |
| | | C27 | 10nF | | |
| | | C28 | 10nF | | |
| | | C29 | 47μF | | |
| | | C30 | 10nF | | |
| | | C31 | 10nF | | |
| | | C32 | 10nF | | |

NOTES
1. Resistors are 1/4W when not specified.
2. RV1 to RV4 are 20 turn preset potentiometers (43P102/R8432).
3. 1nF = 1000pF = 103 encapsulated chip.
4. 2N3904
   2N3906




5. Analog and clock inputs are connected using sub-vis type connectors.
6. The input can be AC coupled at link 1. An extra capacitor = 100nF (non-electrolitic) should be used.
7. If the board is to be used directly into another circuit without connecting lead, output termination on the board can be provided using two '8' single in line resistor strips. 270 ohm strip should be connected to -5.2V and 150 ohm should be connected to 0V. (RS part numbers are 140-237 and 140-215 respectively.)
8. Holes have also been provided for Q and $\overline{Q}$ clock pulldown resistors. 330 ohm resistors may be used on the ADC board.
9. The loom connecting this board to the DAC board is twisted pair with a characteristic impedance of 100 ohm. RS Stock No. 360-071.
10. All capacitors have minimum voltage rating of 16V.

## DAC BOARD COMPONENTS

| Resistors | | Capacitors | | Semiconductors | Miscellaneous |
|---|---|---|---|---|---|
| R1 | 47 1/8W | C1 | 10nF | IC1 SP9768 8-bit DAC | In-line switch, |
| R2 | 8 x 150 single in-line (RS Part No. 140-215) | C2 | 47$\mu$F | IC2 SP9210 8-bit Latch | RS8447/337-560 |
| R3 | 150 | C3 | 47$\mu$F | | |
| R4 | 150 | C4 | 10nF | | 2-off sub-vis connectors |
| R5 | 270 | C5 | 10nF | | |
| R6 | 270 | C6 | 10nF | | |
| R7 | 8 x 270 single in-line (RS Part No. 140-237) | C7 | 10nF | | |
| R8 | 8 x 150 single in-line (RS Part No. 140-215) | C8 | 22nF | | |
| R9 | 8 x 270 single in-line (RS Part No. 140-237) | | | | |
| R10 | 150 | | | | |
| R11 | 47 | | | | |
| RV1 | 1k multi turn (43P102) (R8432) | | | | |

NOTES
1. Link 1 can be repositioned for Q or $\overline{Q}$ clocks from the edge connector or from the on board sub-vis connector.
2. Link 2 can be repositioned for true or inverse analog outputs.
3. The output amplitude should be adjusted to 0.5V p-p with RV1.
4. R11 is optional. A 1V p-p output can be obtained by replacing R11 with a link.
5. The output will be DC biased below ground by 0.25V with R11, or -0.5V with R11 shorted.
6. The DAC board will accept an 8-bit input for future expansion.

## EDGE CONNECTIONS

### TOP VIEW

| ADC BOARD | | DAC BOARD | |
|---|---|---|---|
| **Pin No.** | **Function** | **Pin No.** | **Function** |
| 1 | N/C | 1 | N/C |
| 2 | N/C | 2 | N/C |
| 3 | N/C | 3 | N/C |
| 4 | N/C | 4 | N/C |
| 5 | +12V | 5 | N/C |
| 6 | N/C | 6 | N/C |
| 7 | -12V | 7 | N/C |
| 8 | -5.2V | 8 | -5.2V |
| 9 | -5.2V | 9 | -5.2V |
| 10 | N/C | 10 | A0 LSB |
| 11 | N/C | 11 | A1 |
| 12 | A0 LSB | 12 | A2 |
| 13 | A1 | 13 | A3 |
| 14 | A2 | 14 | A4 |
| 15 | A3 | 15 | A5 |
| 16 | A4 | 16 | A6 |
| 17 | A5 MSB | 17 | A7 MSB |
| 18 | N/C | 18 | N/C |
| 19 | N/C | 19 | N/C |
| 20 | N/C | 20 | N/C |
| 21 | $\overline{CO}$ | 21 | N/C |
| 22 | N/C | 22 | N/C |
| 23 | N/C | 23 | N/C |
| 24 | N/C | 24 | N/C |
| 25 | Q CLOCK | 25 | Q CLOCK |
| 26 | $\overline{Q}$ CLOCK | 26 | $\overline{Q}$ CLOCK |
| 27 | +5V | 27 | +5V |
| 28 | N/C | 28 | N/C |
| 29 | N/C | 29 | N/C |
| 30 | N/C | 30 | N/C |

# Evaluation and Comparison of High Speed ADCs

**High speed ADCs are used in many varieties of applications; each application requires special consideration to a particular parameter. For example, designers of video (radar or TV), would pay particular attention to differential linearity, whereas designers using the ADC for measurement systems would need to pay attention to integral linearity. Other systems may need accurate information on analog power bandwidth or bit accuracy.**

**Specification requirements therefore differ from application to application, and this can make comparison of ADCs difficult. Outlined below is a list of important tests and evaluation methods, starting with the most simple and progressing to the more sophisticated.**

ADC evaluation falls into two main groups: the first group utilises a high speed digital to analog converter to reconstruct the digital output into an analog form that can then be displayed on an oscilloscope (Fig.21). The second group of methods looks directly at the digital data. This requires a high speed logic analyser and usually a GPIB-compatible desk-top computer (Fig.22). Computer programs and detailed test methods are available from Hewlett Packard, product note 5180A-2.

## TESTS USING RECONSTRUCTION THROUGH A DAC

### Test 1. Low Speed Ramp (Fig.14)

This test is very simple. A linear full scale triangular wave (or ramp) is applied to the ADC input, at a frequency that is less than $f_{clock}/(2 \times 2^N)$, where $N$ = number of bits. This ensures that all the timing intervals are displayed. The output from the ADC is then reconstructed in a DAC which should have a greater resolution than the ADC to ensure that all output codes are displayed. The results can then be viewed on a good high resolution oscilloscope.

The resultant staircase has vertical voltages that are due to the DAC and horizontal time intervals that are due to the ADC. Therefore any vertical errors can be ignored as they are due to the DAC alone (using the six most significant bits of the Plessey SP9768 DAC, the vertical steps will appear ideal for a 6-bit ADC). The horizontal time intervals can be viewed in more detail by using the oscilloscope to invert and add the input signal. The remainder will be the quantisation noise. The error will be 1 LSB high $\pm$ 1/2 an LSB. Beware of 'scope input overload and the delay between the two signals when using this method.

A point of major interest is that a differential error or high speed groups of glitches occurs at the mid-step or zero crossing. This is a common problem with many ADCs. At this point the digital section of the ADC is changing from 100000 to 011111; as all the binary outputs are changing at once, large current spikes can result.

Another cause of zero crossing error is two-stage design. Within many flash ADCs the reference chain and/or the comparators are split into two ranks. The device then behaves as two 5-bit devices. This has been avoided in the design of the SP9756.

### Reference voltage considerations

The overall accuracy of the staircase will be mostly proportional to the reference voltage. This is because the comparator offsets will remain constant while the bit size will vary with the reference voltage. Therefore it is important to know the reference voltage before making comparisons. Disadvantages of the ramp method are (a) it is difficult to obtain numerical results - although this can be achieved using a Tektronix 7854 scope and (b) this test does not reflect the accuracy at speed.

### Test 2. Near Nyquist Beat (Fig.15)

The Nyquist frequency is exactly one half the clock frequency. If a sinewave analog input is set close to this frequency in an unfiltered system, a beat will result. The beat frequency will be

$$f_B = \left| \frac{fc}{2} - f_{in} \right| \text{ (3MHz in Fig.15)}$$

This test is primarily for evaluation of analog bandwidth. The comparators acquire voltages at each end of the input range on successive samples. An ADC that can slew both positively and negatively fast enough to produce an undistorted sinewave beat, contains an extremely fast comparator section. Disadvantages of this method are (a) it is difficult to produce a numerical value of merit, (b) scope triggering is delicate and (c) DAC overshoot can cloud the results.

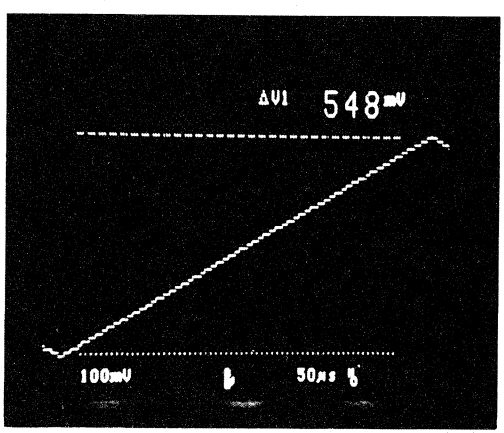



*Fig.14 SP9756-6 ADC Linearity. 1kHz ramp input sampled at 100MHz (1V I/P to ADC)*

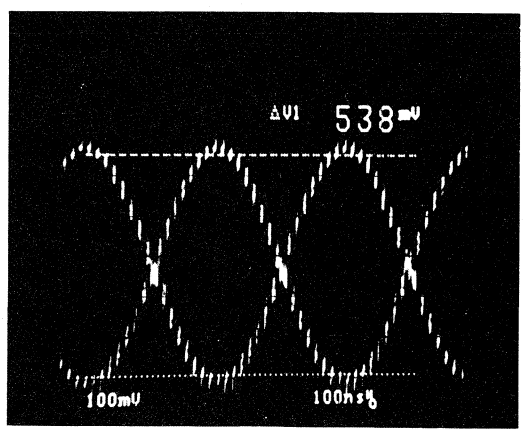



*Fig.15 ADC Near Nyquist Beat. 53MHz input sampled at 100MHz 1V I/P to ADC*

### Test 3. Near Clock Beat (Fig.16)

This is similar to Test 2, except the analog frequency is set close to the clock frequency. Again a beat is produced, $f_B = |fc - f_{in}|$ (3MHz in Fig.16). This is an extremely severe test of input bandwidth. An undistorted sinewave with full amplitude can be produced by the Plessey SP9756 followed by the SP9768 DAC. This test can be extended by increasing the clock and analog frequency i.e. keeping the beat constant, until the output amplitude is reduced by 3dB. This gives an approximate figure for power bandwidth (300MHz using the SP9756).

The disadvantage of this method is that the test can be affected by the DAC. As the DAC is being updated beyond its specified limits, slight glitches and disturbances can result.

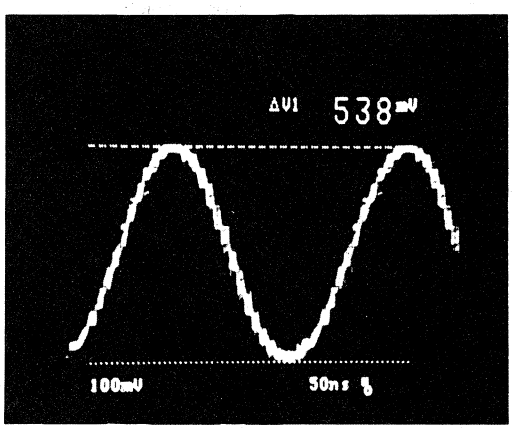



*Fig.16 ADC Near Clock Beat. 103MHz input sampled at 100MHz 1V I/P to ADC*

## TESTS USING DIRECT DIGITAL ANALYSIS

This group of tests are performed by acquiring the digital data directly from the ADC. The data is usually acquired by a high speed logic analyser and then transferred to a desk-top computer for analysis. The ADC is usually driven with a sinewave of full amplitude. The following gives the more popular methods of analysing and plotting the data. It is essential with all the following methods that the input is set to precisely full scale.

Most of the methods below benefit from phase-locked sampling (stationary sampling). In most cases this enables the number of samples taken to be greatly reduced and therefore improving test times.

### Method 1. Histogram Test (Fig.17)

This test plots the output code against occupancy of that code. A histogram is produced that theoretically should form a sinewave cusp. Deviations from this cusp will represent differential and integral linearity errors. A differential error would weight the probability of a code being occupied, either more or less than it should be. This distorts the cusp in a positive or negative direction at the code in question. The advantage of this test is that it will indicate the dynamic accuracy of the ADC, i.e. the accuracy to input frequencies up to Nyquist. This is of course not practical using a DAC and oscilloscope. The disadvantages of this method are that (a) it requires a large number of samples and (b) as a cusp is formed, direct reading of linearity from the curve is difficult.

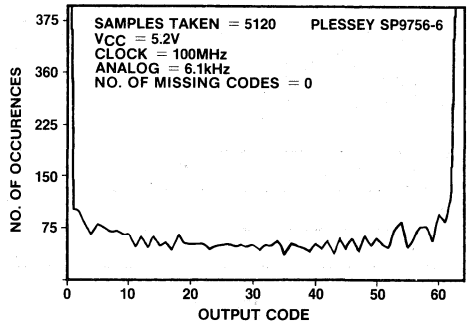



*Fig.17 Histogram test*

### Method 2. Non-lin in LSB (Fig.18)

This test is almost identical to the histogram method. The same data can be used within the desk-top computer. Again a large number of samples are taken and again the occupancy of each code is plotted. The subtle difference is that a $\sin^{-1}$ weighting is applied to the results. This removes the cusp. A graph of differential linearity can be plotted from

$$\frac{\text{(Actual probability)}}{(\sin^{-1}\text{ weighted probability})}$$

As the cusp has been removed, the resulting graph shows at a glance differential non-linearity in terms of LSB. This test can also be performed up to Nyquist limits. A disadvantage is that noise and bandwidth limitations are not evident.

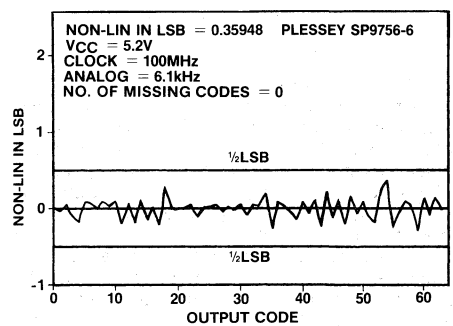



*Fig.18 Differential non-linearity in LSB*

### Method 3. Accumulation Error (Fig.19)

Again, this test can be performed from the initial data. The data is processed to give a graph of integral linearity which can be expressed in two main ways - 'end point' or 'best fit'. The 'best fit' method allows the points to be compared with a line drawn through the average of the results. The 'end point' method is more severe as the line is defined by the end points of the results. From Fig.19 we could quote an integral linearity of 0.25 LSB for 'best fit', but only 0.35 LSB for 'end point'. Therefore it is very important to know which method has been used before comparing integral linearity figures. To form the graph a statistical method is used with many samples taken. The results are corrected for the input sinewave and a graph plotted of levels against deviation from the straight line drawn between end points. This method can also be performed at frequencies up to Nyquist. Fig.20 shows a plot of end point integral linearity at near Nyquist frequencies for the SP9756. As this test represents the total deviation from a theoretically perfect ADC it is a very useful measurement. It also gives a clear representation of distortion caused by the quantising system.

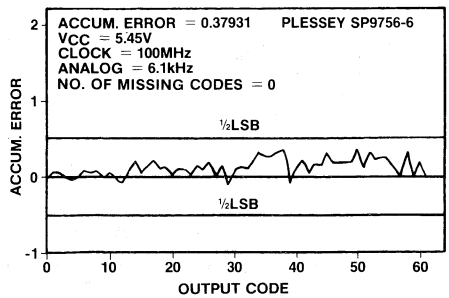



*Fig.19 Accumulation error (integral)*

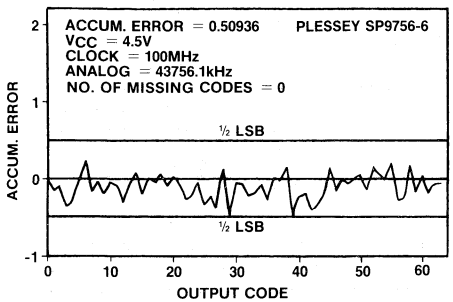



*Fig.20 Accumulation error at near Nyquist*

### Method 4. Sinewave Curve Fit

This test is similar again in that the data is processed by a desk-top computer. The idea is to take a theoretically perfect ADC, generated by the computer and then subtract the actual ADC information contained in the logic analyser from it. The data for the perfect ADC is produced by curve fitting: the Least Squares method is usually used to minimise the error between the actual and theoretical data. A theoretically perfect digitised sinewave which has exactly the same amplitude, frequency and phase as the actual data is required. The remaining difference between these groups of data now represents not only differential and integral linearity but also noise and aperture uncertainty effects. The disadvantages of the method are that (a) the programing must be precise, (b) analog bandwidth problems are not evident and (c) DC offset errors are ignored.

### Method 5. Fast Fourier Transform

The fast Fourier transform (FFT) is simply a numerical method for conversion from the time domain to frequency domain. The method is based on the fact that any waveform can be constructed from a number of discrete pure sinewaves of different frequencies and amplitudes. These frequencies can then be plotted to give the spectrum of the signal.

Two methods are used for acquiring the data. The first and most popular, as in the previous methods uses a logic analyser, which transfers the data to a desk-top computer for FFT calculations. The second method (usually using TEK7854 waveform analyser) uses a DAC to reconstruct the data which is digitised and sent to the computer for FFT. The spectral information from this method contains DAC distortions within the results. This can be an advantage if a complete system is to be analysed.

The FFT contains not only linearity information but also other problems that deteriorate the signal-to-noise ratio. Linearity errors cause sidebands to be produced in the frequency domain and so measurement and analysis of the system can be performed in great detail.

The disadvantages of the FFT method are (a) it is important to choose the input frequency to avoid coincidence between the fundamental and harmonics reflected back into the baseband by the sampling technique, (b) the resultant spectrum will also contain the second harmonic of the input. For ADCs over 7 bits it is usually necessary to subtract this harmonic and its aliases from the results and (c) analog bandwidth is not apparent in the results.

## CHOICE OF TESTS

To form a good general opinion of a high speed ADC it is necessary to perform the DAC reconstruction tests as they not only show any gross problems with minimal effort, but they give a clear picture of the analog bandwidth and slewing performance. For an evaluation and experimentation system the accumulation methods give a clear picture of performance but for a test system the sinewave curve fit or FFT methods test a wider range of parameters.

## OTHER TESTS AND CONSIDERATIONS

### Aperture Uncertainty

Aperture uncertainty refers to the amount of jitter at the instant the sample is taken. In other words the time taken between one sample point and the next may not be exactly the same as this time on the following cycle. This uncertainty is usually in the order of 20ps and so measurement is incredibly difficult. The results from techniques using stationary sampling are probably more than 50 % inaccurate at high frequency. The effects of aperture uncertainty are usually masked by the phase jitter on the clock signal used to drive the ADC.

Aperture uncertainty is also found within the comparator section of the ADC. The aperture uncertainty will be increased if the comparators take slightly differing times to respond to the sample request.

### Metastable States

This exotic term is used when discussing missing samples. There is a finite probability that when a comparator is latched it is at balance. This in fact would be a very rare event, as noise and hysteresis would tend to trip the comparator within the time it is being latched. Nevertheless figures as high as 1 missing sample in $10^{12}$ have been quoted. The Plessey SP9756 has been designed using techniques to reduce metastable states.

A balanced comparator would in fact cause an error within the decode ROM that in many ADCs causes an all '0's output code for that sample.

### Mountain Climb Effect

The 'mountains' here are in fact the spikes produced by the fast edges of the clock. If they are not adequately removed from the reference chain and analog input an interesting effect occurs: as the clock edge speed is increased the reconstructed output will show a DC shift, sometimes above one LSB. This is due to the sample being taken at exactly the same time as the sample edge disturbs the input signal. The result is a 'DC' shift because they will always remain in phase. Good layout using split grounds and good decoupling will minimise this problem.

## Data Valid Time

This is an important and frequently ignored parameter. It is simply the proportion of time that the output data is valid, expressed as a percentage of the minimum clock period. If the ADC has a maximum frequency of 100MHz i.e. a minimum period of 10ns, a 70 % data valid time indicates that the data would be valid for 7ns and could be acquired at any time within this period. This is important as the shorter the time, the harder it is to design the system. High cost can result if extra latches and delay lines are needed to collect the data consistently over the specified temperature range.

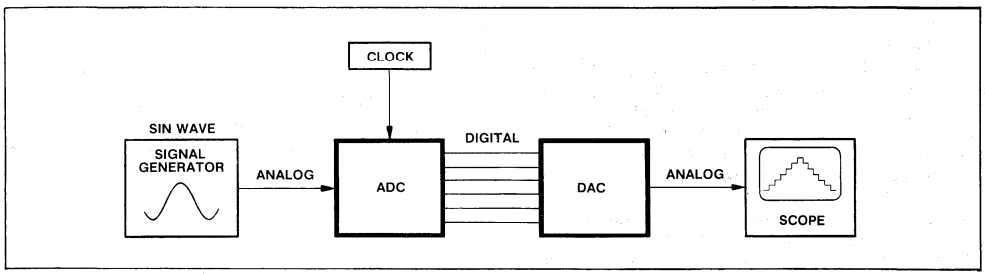



*Fig.21*

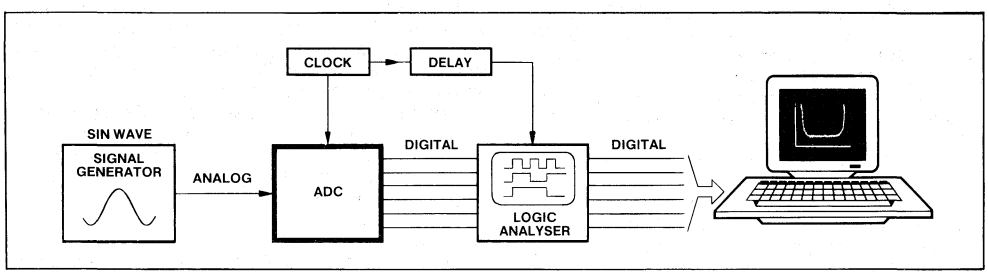



*Fig.22*

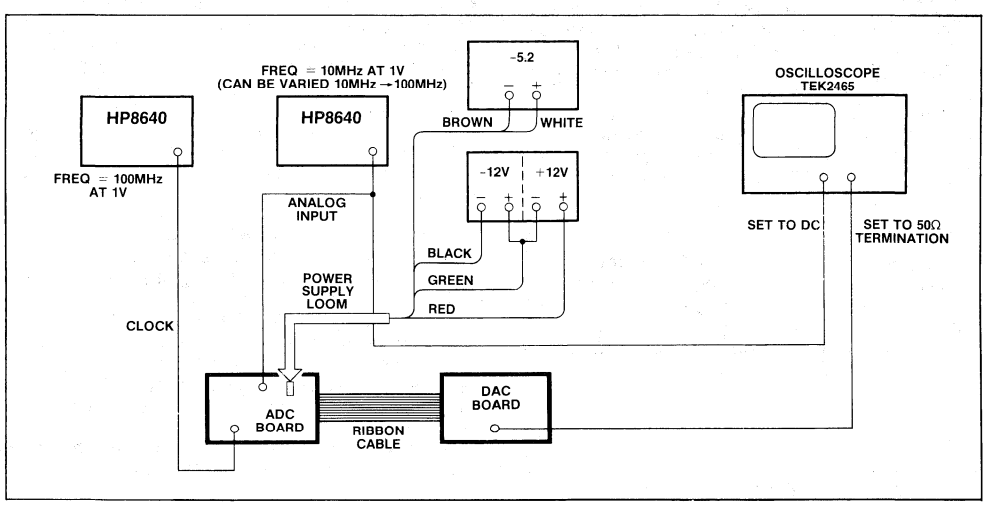



*Fig.23 Connection to equipment*

## RELATED DOCUMENTS

**Low Cost Video Speed A-D/D-A (Plessey Semiconductors SP9754 Application Note PS 1993)**
**Data Products Integrated Circuits Handbook (PS 1989) (Plessey Semiconductors)**


## ACKNOWLEDGEMENTS

Plessey Design UK
Plessey Applications California USA
Plessey Applications UK


## REFERENCES


Dynamic performance testing of A to D converters - Hewlett Packard Product Note 5180A-2.

# SP973T8 - An 8-Bit Wideband Flash ADC with TTL Outputs

AN72

**This Application Note covers both general ADC system Design and practical circuit ideas to support the SP973T8 30MHz Flash TTL ADC.**

## DYNAMIC RANGE

The dynamic range of any flash ADC can be calculated very simply. As each extra bit causes a doubling of the number of comparators used in the device input, this in turn causes a two to one improvement in the dynamic range of the device. A two to one improvement is 6dB, so if we multiply the number of bits by 6, we get the approximate dynamic range of the device in decibels.

This can be further refined by taking into account the shape of the remaining quantisation noise produced by the ADC. Theoretically this gives a constant 1.8dB improvement above the 6 x N figure. However in any practical system we would have a variation in the amplitude of the quantisation noise, caused by the differential linearity error within the ADC. Therefore an ADC with an accuracy of $\pm \frac{1}{2}$ LSB will not have the full 1.8 dB advantage. It can be shown that for a $\pm \frac{1}{2}$ LSB device an improvement of about 1.2 dB is seen.

Hence, for an ADC with N bits and $\pm \frac{1}{2}$ LSB accuracy, the theoretical maximum dynamic range is given by:-

6 x N + 1.2. For an 8- Bit device we have : 49.2dB

The Bit accuracy of many ADCs falls sharply with increasing analog input frequency; all Plessey Semiconductors' standard products are tested dynamically to avoid such problems.

## ANALOG INPUT

The SP973T8 is a high speed flash ADC with a wideband input. Therefore the input circuitry is guaranteed not to slew rate limit at high input frequency. This is very important when digitising pulses or when high accuracy is required, up to the Nyquist frequency limit.

The Nyquist limit is simply one half of the clock frequency, and if any signal is applied to the ADC input above this limit it will be reflected, by the clock, back into the passband of the ADC. This effect is called *aliasing*.

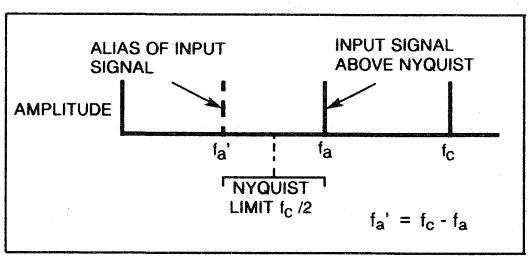



*Fig 1*

In many systems anti-aliasing filters are required to prevent any high level inputs above fc /2.

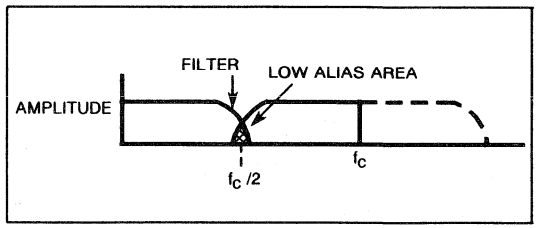



*Fig 2*

With many video ADCs on the market the analog bandwidth of the input stage will produce slight distortion, and hence produce intermodulation products which can be above the Nyquist frequency limit. With these ADCs restricting the analog input bandwidths is largely ineffective, as it is the ADC itself which causes signals above Nyquist to be generated.

These distortion effects would be difficult to determine from the specification of the device, as they are difficult to test in production. To make matters even worse, sometimes when specifing signal to noise of a device the alias signals are ignored.

### Bit Accuracy

One parameter sometimes specified by manufacturers, which will show the true bandwidth and quality of an ADC, is Bit Accuracy. For any ADC to maintain ± 1 LSB at near Nyquist frequency requires an input stage with excellent bandwidth and very low distortion. (see 'near Nyquist beat' test in Application Note AN56 for further information)

To achieve this within the SP973T8 an input bandwidth of over 80MHz was required; this maintains virtually ideal characteristics within a 10MHz input bandwidth.

The high $f_T$ (7GHz) of WS process has made high input bandwidths possible on a device with similar and in most cases lower power consumption than competitive products.

## DRIVING THE INPUT CAPACITANCE

Not only is it important to have low distortion within the ADC but also the circuit driving the ADC must show equivalent wideband performance.

High speed flash 8-Bit ADCs have 255 comparators all connected to the input. The SP973T8 is no exception, and hence it has an input capacitance of about 40pF. This capacitance is slightly voltage-dependent and therefore it is important to provide a good quality low impedance drive for the SP973T8.

Plessey provide two op-amps with the required performance: the SL541 and the SL9999.

**SL541**

The SL541 is a bipolar device with high slew rate and excellent pulse handling, plus very good overload performance. The device has been used by many manufacturers as the op-amp driver in ADC systems.

One reason for this is the provision for adjustable open loop gain. The open loop gain can be reduced by a single resistor for stable operation at closed loop gain as low as unity.

The SP973T8 input requires a high current drive at high frequency. Therefore it is advised that one of the Plessey range of high performance transistors is used within the op-amp feedback loop (2N3904 or equivalent).

**SL9999**

This device is similar to the SL541, but has three main differences.

First, the bandwidth of the SL9999 is up to 400MHz under unity gain conditions and at least 200MHz when driving a 30pF capacitive load.

The second difference is that the SL9999 contains a power output stage which is capable of driving at least ± 50mA, this is adjustable down to ± 10mA using an external resistor ($R_X$ in Fig 4).

The third difference is that external compensation cannot be provided. To avoid problems it is recommended that a closed loop gain of about 4 is used, when driving ADC inputs.

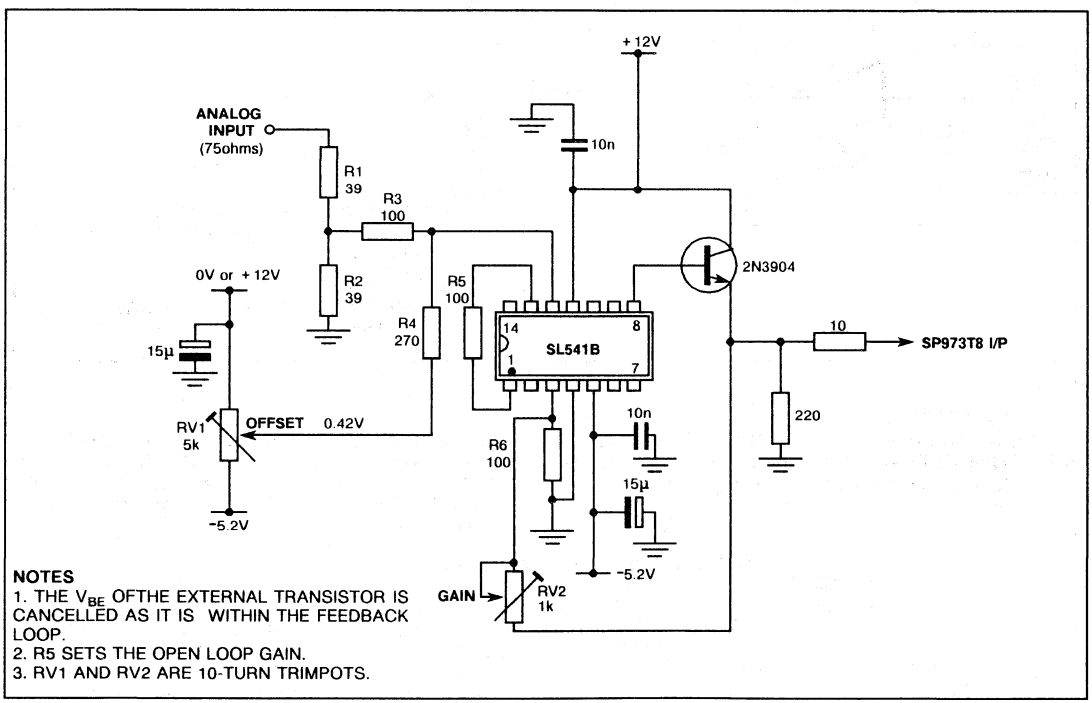



*Fig. 3*

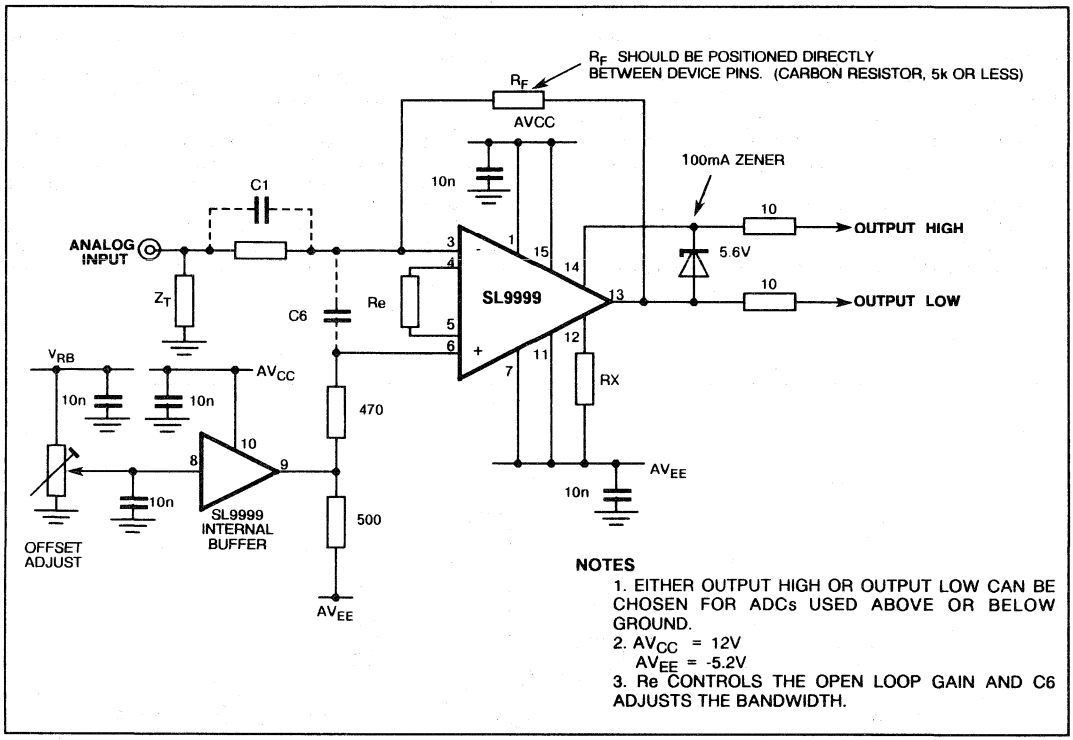



*Fig 4*

**OTHER ADC DRIVERS**

Another device of interest for ADC input driving is the SL6140 400MHz Wideband Amplifier. Although this device may not have the current drive required for precision at high speed, its AGC capabilities can be very useful in wide dynamic range applications. The SL6140 has current sourced outputs which require pull-up resistors. See also the ZN428 DAC for AGC input control from a microprocessor.

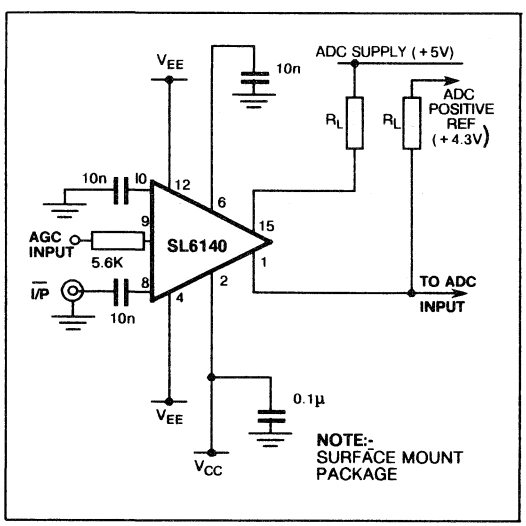



*Fig 5*

**CLOCK INPUT**

The SP973T8 is specified as a 30MHz ADC. However, the typical production device will perform adequately at clock frequencies of over 50MHz with an input of up to 10MHz.

Unlike many ADCs the SP973T8 has an internal clock amplifier and buffer. This amplifier has been introduced to avoid one of the most difficult problems when using an ADC in a system design : clock pickup. A fixed frequency at up to 30MHz with TTL type levels, would cause crosstalk resulting in reduced performance (patterning on video signals, etc.)

The clock input has been designed so that both differential or single ended drive can be used at low voltage levels. Pins 5 and 6 can be used differentially and will accept standard ECL. (See SP92701 device). For single ended operation pin 6 can be decoupled to ground, and pin 5 driven with a 1V peak to peak signal. Pin 6 will then bias to +3.8V and can then be used to bias pin 5, through a resistor for AC coupled clock applications. See Fig 6.

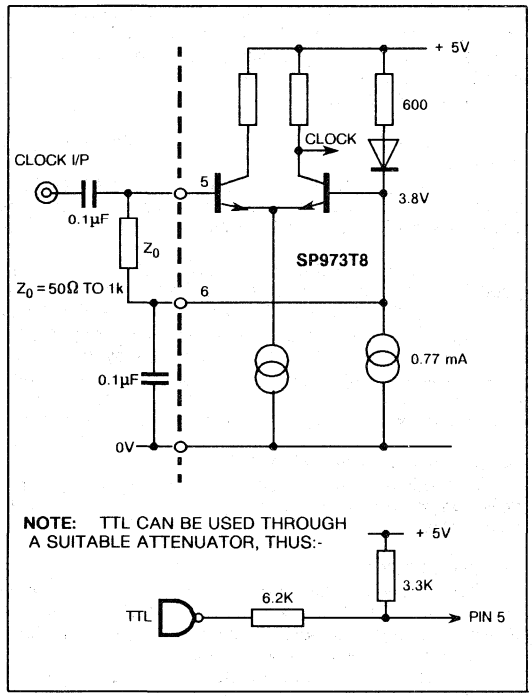



*Fig. 6*

## REFERENCE VOLTAGES

The internal reference chain requires two DC voltages applied to the top and bottom of the internal resistor ladder, as shown in Fig. 7.

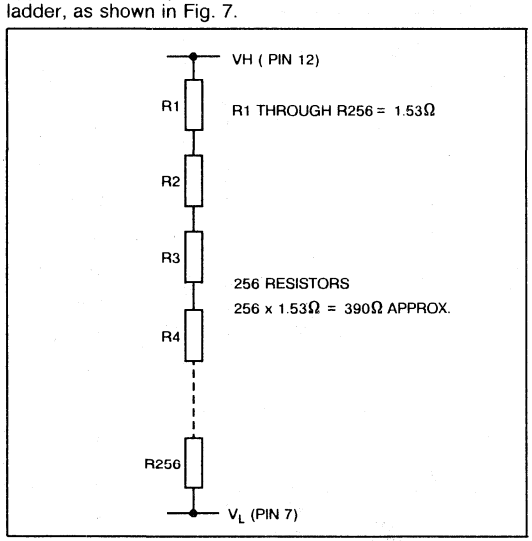



*Fig. 7*

The best differential linearity from any flash ADC is achieved when the maximum reference voltage is applied to the reference chain. This is because the offset voltages of each internal comparator will remain constant.

So increasing the reference voltage will improve the ratio of Bit size to offset voltage and hence improve the overall accuracy. For the SP973T8:-

VH Max = + 4.5V

VL Min = + 1.9V

Therefore the recommended values for VH and VL are

VH = + 4.3V

VL = + 2.3V

The tolerance on the reference chain's absolute resistance is about ± 25% from batch to batch, therefore the current taken by the reference chain for worst case conditions is approximately

$$\frac{2V}{390\text{-}0.25\text{x}390} = 6.8\text{mA}$$

Using a reasonable safety factor 8mA worst case current should be catered for.

## SETTING THE REFERENCE VOLTAGES

### Method 1

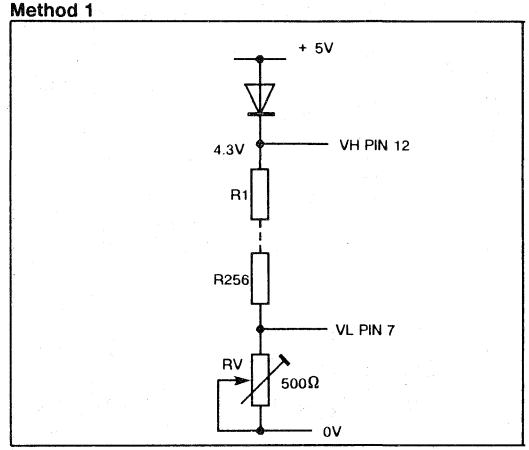



*Fig. 8*

This is the simplest and least precise method. RV is adjusted to maximum resistance then when power is applied RV is decreased until VL = 2.3V.The diode will set VH to approximately 4.3V. There are three main disadvantages with this method. First, setup of RV is needed for each device, second, the 2mV/°C of the diode will change the VH voltage with temperature (over 100mV drift) and third, no supply line regulation is provided.

### Method 2

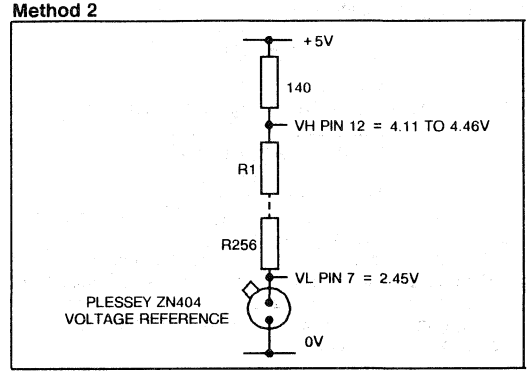



*Fig. 9*

This method is more temperature stable than method 1 and requires no setup as long as a device batch to batch tolerance on VH of 4.11V to 4.46V can be tolerated.

Once again, no supply line regulation is provided using this method. As the differential linearity of the SP973T8 is well within the ± 0.5 LSB limit, the reduced reference voltage has little or no effect (VH -VL = 1.85V)

**Method 3** (precision reference voltages)

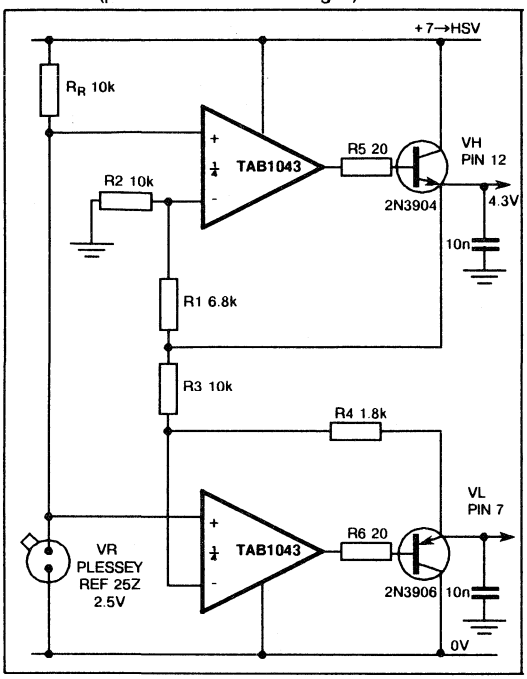



*Fig. 10*

$$VH = \frac{(R1 + R2)}{R2} VR \quad \text{---------- (1)}$$

$$VL = \frac{VR\,(R3 + R4) - VH\,R4}{R3} \quad \text{------- (2)}$$

With R2 and R3 set to 10k. R1 can be calculated by re-arranging equation (1):

$$R1 = \frac{R2\,VH - R2}{VR}$$

R4 can be calculated by re-arranging equation (2):

$$R4 = \frac{R3\,(VR - VL)}{VH - VR}$$

This method gives excellent supply line regulation and precise voltage settings of VH and VL.

The temperature stability will also be excellent and will depend primarily on the input offset with temperature variation of the op-amps used. The Plessey SL562 is a suitable single op-amp or the TBA1043 is a quad version which can also be used.

The only disadvantage with this method is that a separate supply at least 2V above the ADC supply is required. This is a consequence of the output high voltage from the op-amp (we would require a +5V output with the op-amp on a +5V supply!)

**SP973T8 OUTPUT DATA** (see SP973T8 datasheet Fig. 5 for typical test load)

The output levels are TTL compatible, and switch from 0V to +4V. The output drive is capable of providing a useful output with 10pF loads at clock frequencies of over 120MHz.

The outputs are double latched which gives a very good data valid time. This means that the data can be captured any time within the clock cycle except the first 10ns ($t_{pd}$). The data is clocked onto the output pins by the falling edge of the clock signal. The typical system would therefore use the rising edge of the clock to capture the data into RAM or directly into a digital to analog converter (the Plessey MV95308 is a suitable complementary DAC).

**SINGLE- SHOT OPERATION**

To produce a single sample of an analog input the device must be clocked twice. This is due to a one cycle delay inherent within the device.

**MID- REFERENCE**

This is simply the centre of the reference chain bonded out to pin 10 of the device. One of its uses is to provide a decoupling point which aids in the removal of digital noise from the reference chain.

Another use is to trim the device integral linearity in precision measurement systems, as shown in Fig. 11.

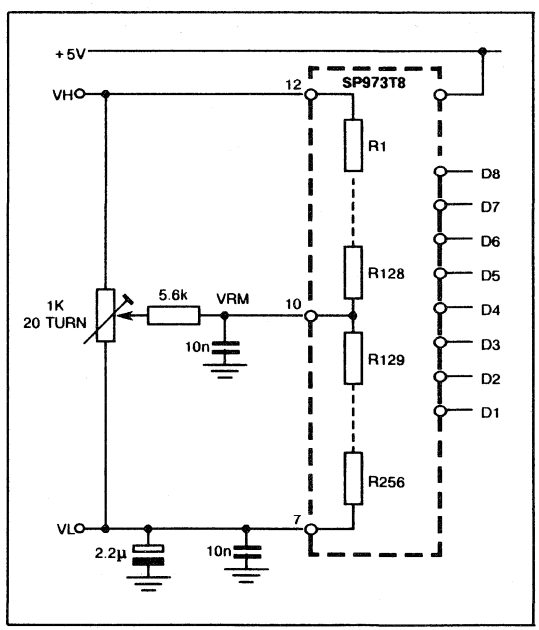



*Fig. 11*

Another and more common use of VRM is to provide a bias input for AC coupled analog inputs, as shown in Fig. 12. Pin 10 is used to bias the analog input.

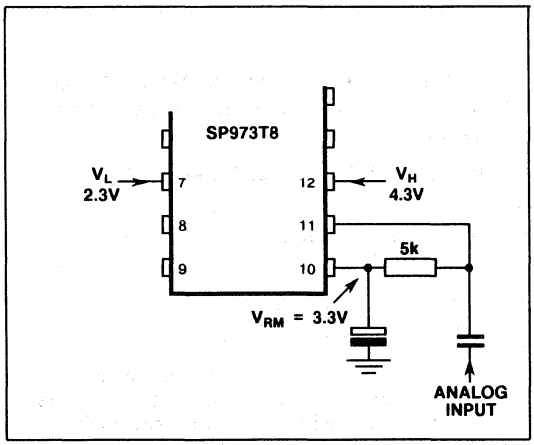



*Fig. 12*

**LAYOUT AND GROUND SYSTEM**

The main objective when laying out the PCB, is to avoid clock or data edges crosstalking into the analog input or onto the ADC references. This can be achieved most effectively by the use of a split ground plane. One analog and one digital ground plane connected together at one point close to the device, is the most suitable approach.

Supply line decoupling is very important when dealing with a mix of analog and digital signals. Low inductance capacitors should be used located close to the device pins.

**STANDARD TV VIDEO ENCODING**

The SP94308 is an 8-Bit 20 MHz TTL ADC which has been specially designed for digitisation of composite video PAL or NTSC signals. Its speed and performance allow digitisation at the standard digital video clock speed equal to three times colour subcarrier with analog bandwidths of over 6MHz (NOT for wideband applications).

The SP94308 contains clock buffering, input buffer and x2 input amplifier, plus a black level clamp and many other useful features that benefit system design (refer to Application Notes AN52, page 4-23 and AN 57, page 4-32). The SP973T8 is recommended for composite video systems where the bandwidth of the signal exceeds 6MHZ (satellite systems, MAC systems,etc.).

**HIGH FREQUENCY DIGITISATION**

The SP973T8 is only one device in our complete range of ADCs. For example, the SP97508 8-Bit 110MHz ADC has ECL outputs and is also designed for wideband applications (refer to Application Note AN65, page 4-54).

**CHARGE COUPLED DEVICES (CCDs)**

Many systems require ADCs and then RAM to store and processed analog information. If random access to the stored information is not required, i.e., time delay or time expansion or contraction, then it can be more cost effective to use a CCD. The range includes devices such as the MS1013, 20MHz low cost 910 element device, which is ideal for video applications. Devices which can be used in systems at 100MHz and above are included in the CCD range. Ask for Application Note AN55 - not published in this Handbook.

**SUMMARY**

Finally, we hope that a clearer distinction has been made between a standard video ADC and the wideband SP973T8. Not only can a wideband device be used in quality video systems, but also in pulse measurement equipment, digital oscilloscopes, radar I and Q channel, video digitisation, nucleonics collision ionisation pulse measurements - indeed, any other system in which the performance of the equipment is defined by the quality of the ADC.

# ZN425 8-Bit A-D/D-A Converter Applications

*(NOTE: This application note is currently being updatad as some devices referred to in have become obsolete since publication.)*

## 1. INTRODUCTION

**Digital to analogue, (D-A), and analogue to digital (A-D), conversion is a specialised field of electronics. It is useful to consider first the general principles of such conversion techniques, and definitions commonly used in the general field of A-D and D-A conversion.**

**The discussion is limited to 8-bit converters of a type similar to the ZN425E, illustrated in Fig.1a.**

Digital information, fed in to the converter, normally as parallel bits, generates an anlogue output corresponding to the value of the binary coded number entered at the input. Ignoring errors for the moment, and assuming that the analogue output is a voltage, the output can be expressed as:

$$V_{out} = V_{full\ scale} \times \frac{\text{Binary input}}{\text{Full-scale binary input}}$$

which, in the case of the ZN425E, is

$$V_{out} = V_{REF} \times \frac{\text{Binary input}}{256}$$

The voltage output is obtained using a resistive ladder network shown in Fig. 1b. Switches connect resistors within the network either to the reference voltage or to the ground line according to the state of the binary inputs controlling each particular switch.

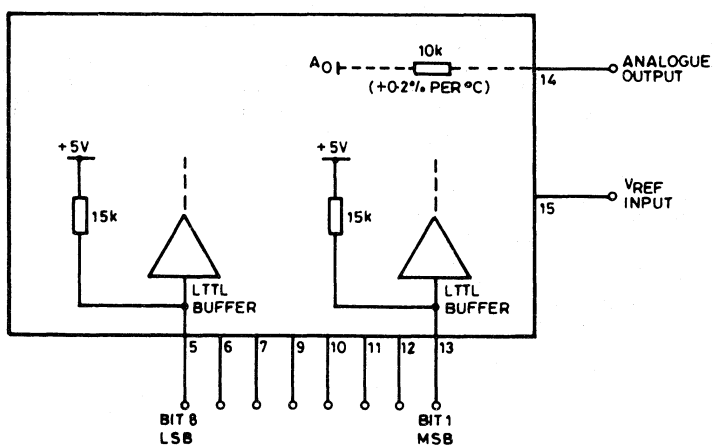



**Fig. 1a Basic 8-bit D-A converter**

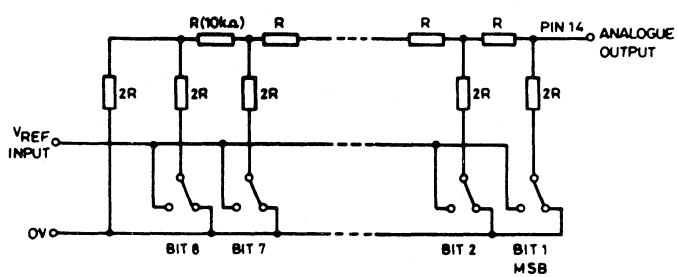



**Fig. 1b The R-2R ladder network**

The block diagram of the ZN425E circuit is reproduced in Fig. 2.

The integrated circuit is fully monolithic. It contains a resistive ladder network, a logic input select switch, voltage switches, an internal reference and a counter. The D-A reference may be connected to the internally generated reference or to an external reference voltage. The inclusion of a counter within the circuit considerably extends its application. A 'staircase' waveform can be very simply generated at the analogue output by feeding a train of clock pulses into the counter.

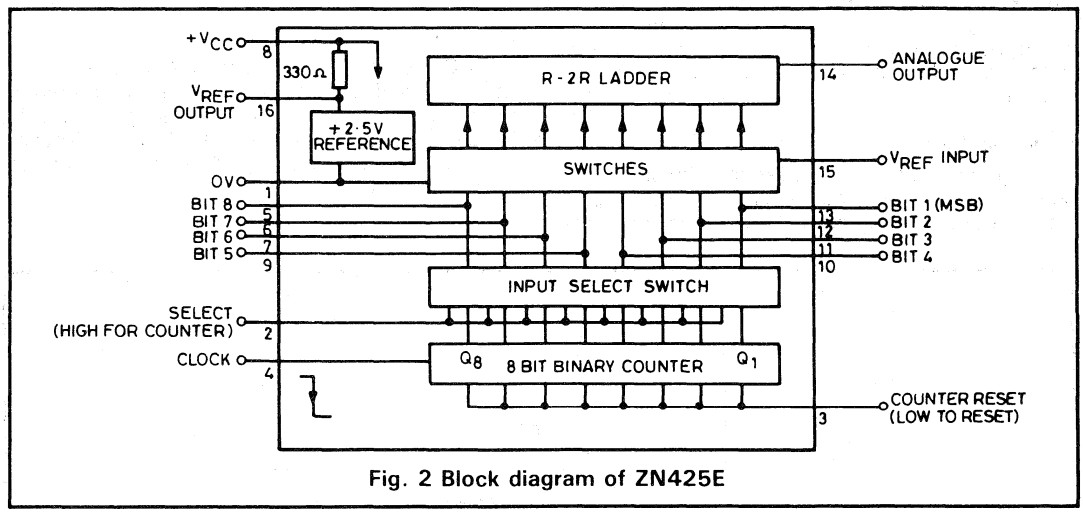



**Fig. 2 Block diagram of ZN425E**

The ZN425E system operation is outlined in Fig. 3. The counter may be clocked by negative going inputs and reset by applying a '0' level to the reset pin.

The digital inputs to the converter may be obtained either from an external source when the 'logic select' pin is at logical '0', or from the counter when it is set to logical '1'. In the latter case the state of the counter appears at the digital input terminals as '0' or '1' levels on open collectors with 15kΩ pull up resistors. In the D-A mode the digital input terminals may be considered as low power TTL inputs.

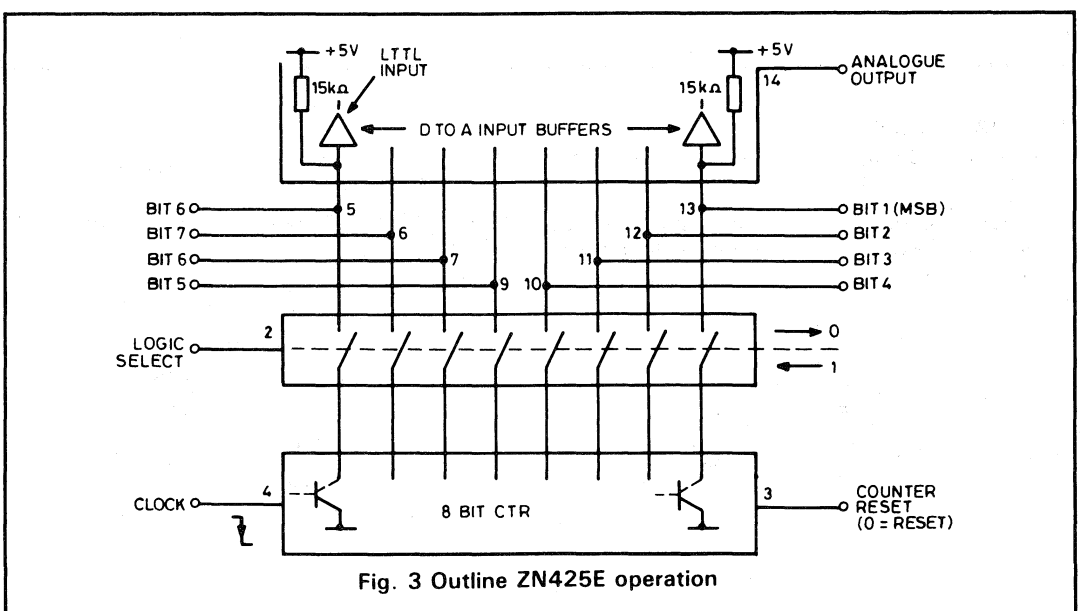



**Fig. 3 Outline ZN425E operation**

## 1.1 Definitions

Various terms commonly used when discussing D-A and A-D converter operation are defined below.

### Resolution

The resolution is determined by the number of digital inputs, i.e. an 8-bit ADC, (digital to analogue converter), is said to have 8-bit resolution. No particular level of accuracy is implied

### Staircase/Ramp

As the binary code is increased step by step, the analogue output also increases in discrete steps. If the input code increases at a constant rate the resulting output will be a staircase.

Since the number of discrete steps is normally large, e.g. 255 for 8 bits, the staircase is frequently termed a ramp, though this is not strictly accurate.

### Monotonicity

A DAC is said to be monotonic if an increase in the applied binary coded digital number always produces an increase in the analogue output. Waveforms produced by a D-A 'staircase' generator illustrated in Fig. 4a shows the effect of non monotonicity.

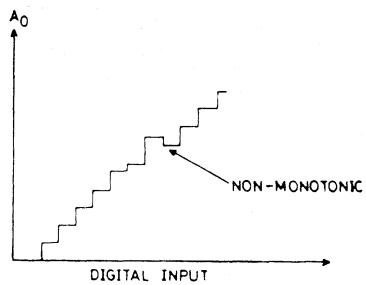



Fig. 4a Non-monotonicity

### Ideal DAC Output

The ideal DAC output of a staircase generator is shown in Fig. 4b.

The output is defined as a set of points on a straight line between zero and full-scale. For an ideal 8-bit DAC:

$$V_{out} = \frac{n}{2^8 - 1} \times V_{FS}$$

$$= \frac{n}{255} \times V_{FS}$$

and $$V_{FS} = \frac{255}{256} \times V_{REFinput}$$

$$\therefore \quad V_{out} = \frac{n}{256} \times V_{REFinput}$$

where 'n' is the number represented by the digital input.

For example

$$01101100 = 2^6 + 2^5 + 2^3 + 2^2$$
$$= 108$$

gives an output $$V_{out} = \frac{108}{256} \times V_{FS}$$

$$= \frac{108}{256} \times V_{REFinput}$$

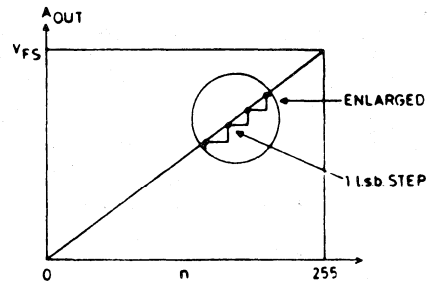



**Fig. 4b Ideal DAC output**

**Linearity error**

A DAC may deviate from the ideal as shown in Fig. 4c. The error is usually specified as a maximum deviation of the analogue output from the ideal output, as a fraction of the least significant bit'. The ZN425E has a linearity better than ± ½LSB, and

$$\tfrac{1}{2}\text{LSB} = \tfrac{1}{2} \times \frac{V_{FS}}{255}$$

**Relative accuracy**

The error expressed as a percentage of the full-scale voltage, $V_{FS}$, is termed the relative accuracy.

The ZN425E, an 8-bit converter with ± ½LSB linearity, has a relative accuracy of $\frac{1}{510} \times 100\%$, i.e. approximately 0.2% accuracy.

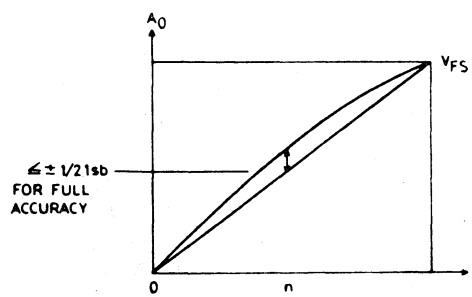



**Fig. 4c Error definition**

## 2. D-A/A-D CONVERTER SYSTEM

### 2.1 8-bit D-A and calibration procedure

The ZN425E gives an analogue voltage output directly from pin 14, so that the usual current to voltage converting amplifier is not required. However, in order to buffer the resistive ladder output impedance, to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary. Figs. 5a and 5b show a typical scheme with either the ZN424P or 741 as the buffer amplifier. The internal voltage reference source ($V_{REF\ out}$) is used, and to minimise temperature drift the source resistance to the inverting input of the buffer amplifier should be approximately 6kΩ. Calibration procedure is as follows:

procedure is as follows:

(i) Set all bits to LOW and adjust R2 until $V_{out} = 0.000V$

(ii) Set all bits to HIGH and adjust R1 until $V_{out}$ = nominal full-scale reading - LSB

(iii) Repeat (i) and (ii)

e.g. Set F.S.R. to +3.840V -1LSB = 3.825V.

$$(1LSB = \frac{3.84}{256} = 15mV)$$

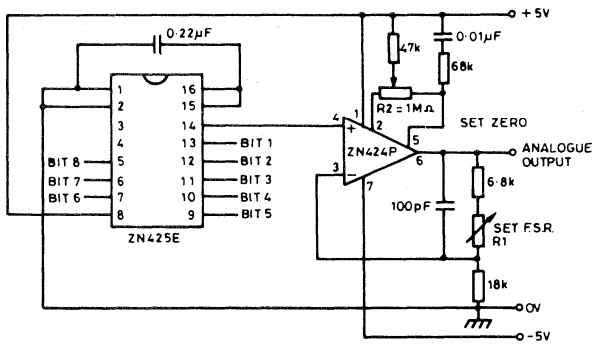



Fig. 5a 8-bit DAC using ZN424P

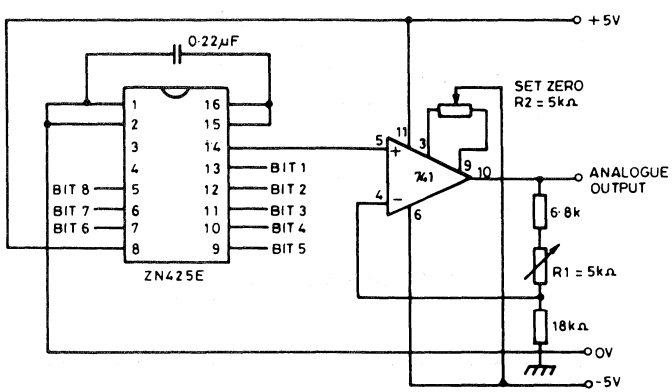



Fig. 5b 8-bit DAC using ZLD741CP

## 2.2 8 Bit A-D and calibration procedure

Fig. 6 shows the ZN425E in a counter type ADC which comprises a comparator and a latch and requires an external clock. Upon application of a convert command pulse (15$\mu$s minimum) the counter is set to zero and at the same time the state of the latch is altered.

The gate is opened, enabling clock pulses to be fed to the counter input (Pin 4) of the ZN425E. The analogue output of the ZN425E begins to ramp up until its amplitude equals that of the analogue voltage at the non-inverting input of the comparator. At this point the comparator changes state, altering the latch to its initial resting state, thus inhibiting further clock pulses. Hence the digital number stored in the respective bits of the ZN425E is a true representation of the analogue input voltage. The diode is included so that when the comparator changes state, its output is effectively clamped at zero (LOW).

Operating clock frequencies can be as high as 400kHz. Improved results may be obtained by using narrow clock pulses to avoid the trailing edge affecting ramp settling. At frequencies above 100kHz a faster comparator than the ZN424 should be used for optimum linearity around zero.

The conversion time is dependent upon the analgoue input and for full-scale reading (F.S.R.) is given by the clock period multiplied by the number of counts.

If $F_{clock} = 256kHz$,

$$T_{Convert} = \frac{2^8}{256 \times 10^3} \text{ seconds} = 1ms$$

The calibration procedure is as follows:

(i) Apply continuous CONVERT COMMAND PULSES

(ii) Apply full-scale minus 1 ½LSB to analogue input and adjust F.S.R. pot until the converter LSB just switches between 0 and 1 with all other bits at 1.

(iii) Apply zero + ½LSB to analogue input and adjust zero pot until the converter LSB just switches between 0 and 1 with all other bits 0.

(iv) Repeat step (ii).

E.g. Full-scale = 4 volts.

$$1LSB = \frac{\text{Full-scale}}{256} = \frac{4V}{256} = 15.63mV$$

Input for zero setting = ½LSB = 7.82mV

Input for full-scale setting = 4V − 1½LSB = 3.97656 volts.

After conversion is complete the analogue input is available from the ZN425E in digital and analogue form and therefore the ADC may be used as a sample and hold with infinite hold time. The convert command is replaced by a sample command.

**A peak detect circuit may also be constructed using similar techniques, and is described in section 3-4.**

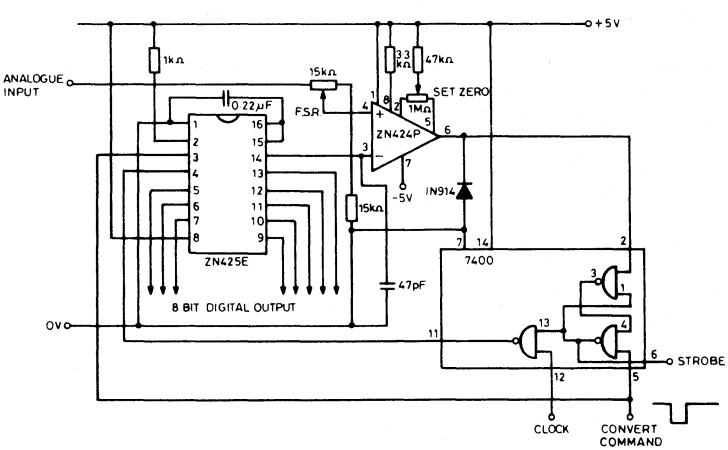



Fig. 6 8-bit A-D converter

### 2.3 Bipolar operation

Previous circuits described have entailed the use of a uni-polar buffer amplifier (using ZN424P and 741) following a DAC as a means of removing the offset voltage, minimising temperature drift and calibrating the DAC. A natural sequal to this is the derivation of a bipolar buffer amplifier which fulfils these conditions. This entails buffering the output of a DAC such that the amplifier output from the buffer is symmetrical about zero. To effect this, the conditions that have to be satisfied are:

(i) When the DAC output $= \frac{V_{REF}}{2}$ (digital input = 10000000) then the buffer amplifier output = zero.

(ii) Gain can be easily selected and suitable resistor values calculated. Actual gain and offset must be capable of fine adjustment.

The circuit of Fig. 7a was first devised as a possible solution.

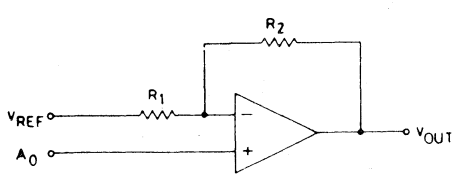



Fig. 7a Bipolar operation, starting point

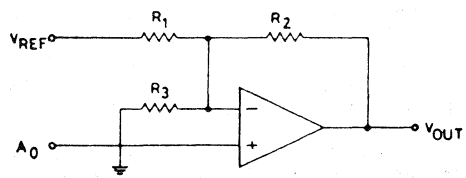



Fig. 7b Bipolar operation, concept progression

If $F_N$ = non-inverting feedback return $= \frac{R1}{R1 + R2}$ and $F_I$ = inverting feedback return $= \frac{R1}{R2}$

Then $V_{out}$ is given by:

$$V_{out} = \frac{A_O}{F_N} - \frac{V_{REF}}{F_I} = A_O\left(\frac{R1 + R2}{R1}\right) - V_{REF}\frac{R2}{R1} \quad \text{. . . equation 1}$$

If $A_O = \frac{V_{REF}}{2}$ and R1 = R2 the $V_{out}$ = 0 satisfying condition (i).

However Gain $\left(\text{defined as } \frac{V_{out}}{A_O}\right) = \frac{R1 + R2}{R1} = 2$ and condition (ii) would not be satisfied since adjusting R1 or R2 would upset the gain on offset. To minimise these disadvantages therefore the circuit of Fig. 7b was devised using an additional resistance, with its Thevenin equivalent of Fig. 7c. Using equation 1 then an expression for the output voltage $V_{out}$ can be shown as:

$$V_{out} = A_O\left[1 + \frac{R2(R1 + R3)}{R1\,R3}\right] - V_{REF}\frac{R2}{R1}$$

For $A_O = \frac{V_{REF}}{2}$ (Condition (i)) then $V_{out} = 0$

and $R1 = \frac{R2\,R3}{(R2 + R3)}$ i.e. R1 = parallel combination of R2 and R3.

Substituting this expression for R1

then Gain $G = \left[1 + \left(\frac{2R2 + R3}{R3}\right)\right] = \left[2 + \frac{2R2}{R3}\right]$

If we let say $R2 = \lambda R3$ the $G = 2(1 + \lambda)$ and $\lambda = \left(\frac{G - 2}{2}\right)$

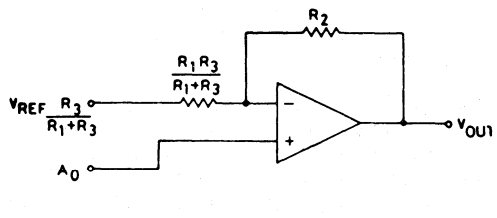



**Fig. 7c Thevenin equivalent of Fig. 7b**

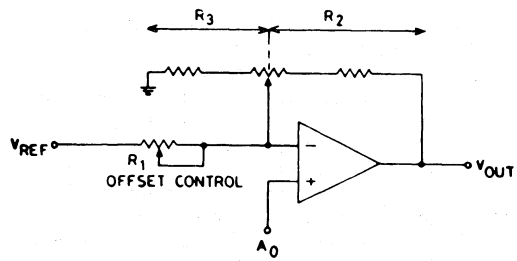



**Fig. 7d Bipolar operation, control schematic**

i.e. $G \geqslant 2$ from which $R2 = \left(\frac{G-2}{2}\right) R3$

And $R1 = \left(\frac{R2\ R3}{R2 + R3}\right) = \left(\frac{\lambda}{1 + \lambda}\right) R3 = \left(\frac{G-2}{2}\right) R3$

Furthermore the buffer amplifier input impedance =

$$\frac{R1R2\ R3}{R1R2 + R2R3 + R1R3} = \left(\frac{G-2}{2G}\right) R3$$

All the above expressions and relationships form a basis for development of the circuit of Fig. 7d whereby by defining a certain gain (G) all resistor values can be appropriately calculated as illustrated.

e.g. Let $G = 4$, then $R_{in} = \left(\frac{4-2}{8}\right) R3 = \frac{R3}{4}$

If $R_{in} = 10k\Omega$ (the value required for minimum offset taking into consideration $R_{out}$ of ZN425E DAC $\simeq 10k\Omega$) then $R3 = 40k\Omega$.

$$R2 = \left(\frac{G-2}{2}\right) R3 = \left(\frac{4-2}{2}\right) R3 = R3 = 40k\Omega$$

$$\text{And } R1 = \left(\frac{G-2}{G}\right) R3 = \left(\frac{4-2}{4}\right) R3 = \frac{R3}{2} = 20k\Omega$$

It has been shown that $R1 = \frac{R2\ R3}{R2 + R3}$. The simplest approximation ensuring this relationship is by using a potentiometer as a gain control.

The finalised circuit is shown in Fig. 8.

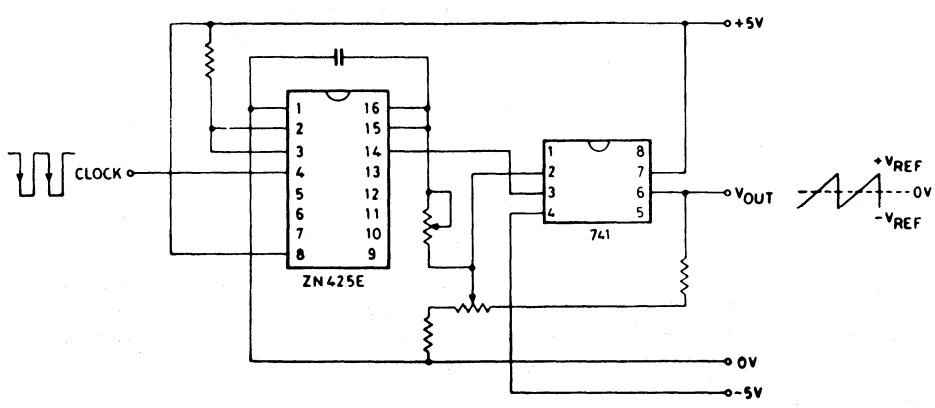



**Fig. 8 Bipolar operation, circuit diagram**

### 2.4 Applications

Applications for the use of the ZN425E in its D-A or A-D mode are those where 8-bit accuracy suffices. This is the majority of transducer applications, particularly as system hierarchy is tending to change with the advent of microprocessors, taking the conversion near to the point of measurement. For example, in data acquisition monitoring say 100 channels, it is feasible and economic to use one D-A per channel and multiplex one A-D per 8 channels using a single microprocessor.

If one reference is required to power several converters, additional source current may be provided by an external parallel resistor from supply to reference providing 1.2mA per additional converter in excess of three. In this case the additional earth pin current causes an offset due to a pin resistance of around 0.1Ω.

Specific applications of 8-bit A-D are in conjunction with stress or strain gauges, and many temperature applications. 8-bit D-A may be used for driving chart recorders, programmable power supplies and actuators.

## 3. RAMP GENERATION

The counter in the ZN425E is very convenient for feeding in a clock to generate a staircase. This facility is used in the majority of applications detailed below.

The count rate which may be used to obtain full ramp accuracy, determined by the worst case settling time of 2μs, is 500kHz, giving a cycling time of around ½ms. However, the counters are capable of being clocked at up to 5MHz, though there will be a loss in staircase accuracy at this speed.

### 3.1 Continuous

This is illustrated by the circuit of Fig. 9 and is simply accomplished in the normal DAC mode by applying clock pulses to the on chip counter (pin 4) of the ZN425E, which produces a staircase waveform. When the counter is full it returns to its empty state and counting recommences resulting in a continuous ramp.

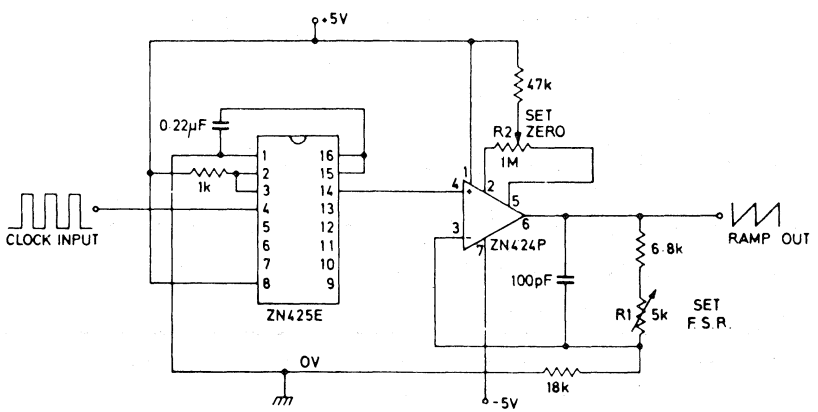



**Fig. 9 Precision ramp generator**

In order to remove the offset voltage and to calibrate the converter a buffer amplifier is necessary as previously described for the DAC.

The ramp period for 8 bits will be equal to 256 times the clock period, and the maximum amplitude of the ramp from the ZN425E using the internal reference voltage will be $V_{REFout}$ − 1LSB. Therefore, the peak ramp amplitude from the buffer will be this value times the amplifier gain, which, with gain adjustment potentiometer set halfway is

$$2.5V \times \frac{3}{2} = 3.75V.$$

A duty cycle drive signal is sometimes required from an input voltage generated by a potentiometer, for example, for actuator drives, or general power control. This may be provided as shown in Fig. 10, where the ZN425E provides a continuous ramp, against which the voltage reference is compared using a ZN424P. The output from the comparator then provides the duty cycle signal directly.

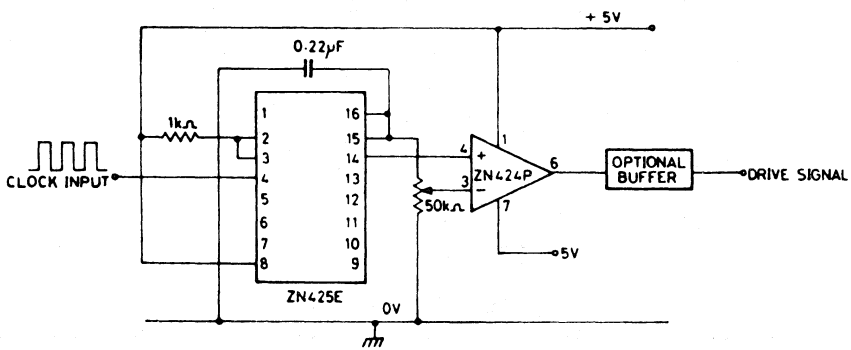



**Fig. 10 Duty cycle drive signal**

### 3.2 One shot

A single one shot ramp can be generated quite simply (Figs. 11a and 11b) by using a latch and two capacitors to control the counter reset of a ZN425E DAC. Operation is as follows:

The stationary states of the latch are shown, these being initially determined by the charging times of capacitors C1 and C2, which ensures the counter reset of the ZN425E (Pin 3) is LOW. Upon operating the START button the states of the latch are altered and a HIGH is fed to the counter reset enabling counting of the input clock pulses to commence. The analogue output begins to ramp up until the counter is full at which point the MSB goes LOW altering the latch to its initial resting states. This resets the counter and terminates the ramp. It should be noted that even if the start button is held down at the commencement of the operation, only a one shot ramp results, and not a periodic function.

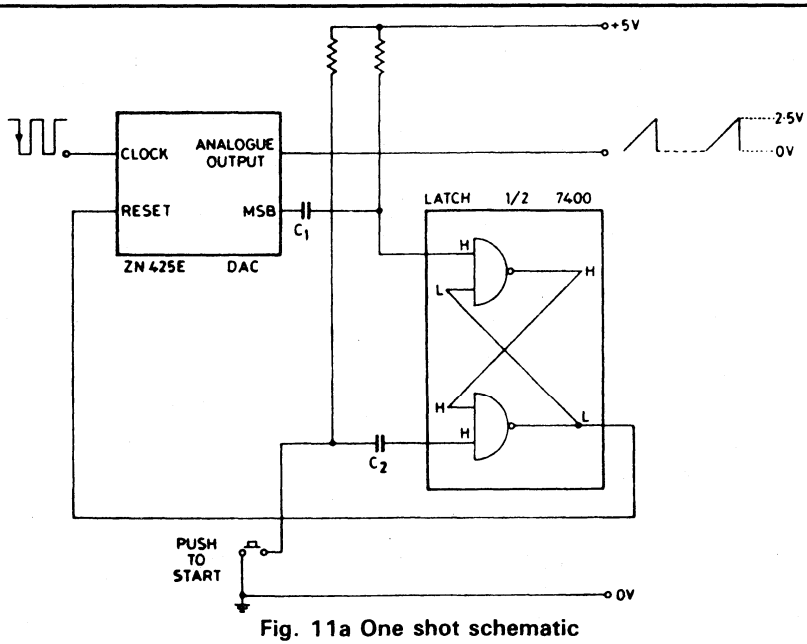



**Fig. 11a One shot schematic**

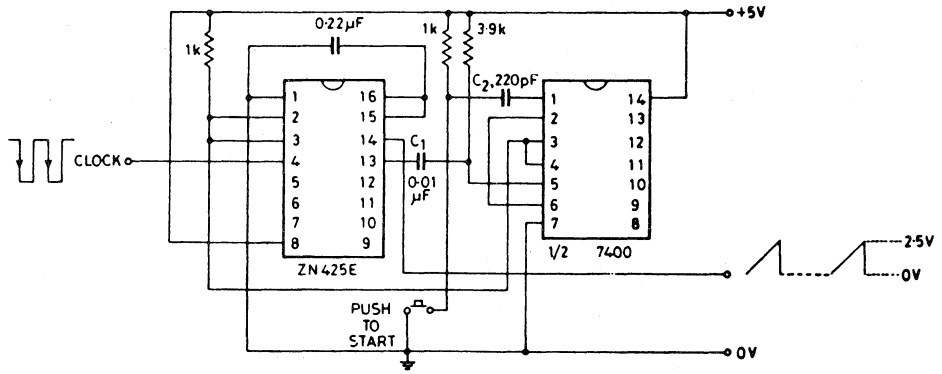



**Fig. 11b One shot circuit**

A more sophisticated alternative method performing the same function, which replaces capacitors by logic, is outlined in Figs. 11c and 11d. Stationary states of the various logic elements are as indicated. The initial state of the flip-flop is determined by the relative states of the PRESET and CLEAR inputs. Upon switching on the supply the PRESET is held LOW with respect to CLEAR because of the charging time associated with C1 and R1. This results in Q = HIGH, $\overline{Q}$ = LOW, therefore, the counter reset on the ZN425E is LOW.

When the start button is pressed, a pulse from the monostable clears the flip-flop, the counter reset goes HIGH enabling the counter of the input clock pulses to commence. The ZN425E analogue output begins to ramp up until the counter is full, at which point the MSB goes LOW. This is fed to the CLOCK input of the flip-flop which then toggles, reverting to its orginal state, thereby resetting the counter and terminating the ramp. As with the previous circuit only a one shot ramp will be generated even if the start button is held down.

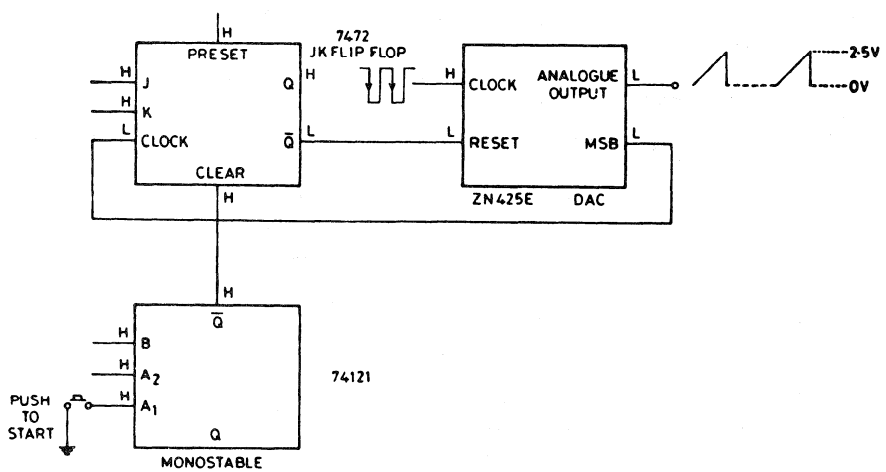



**Fig. 11c Alternative one shot schematic**

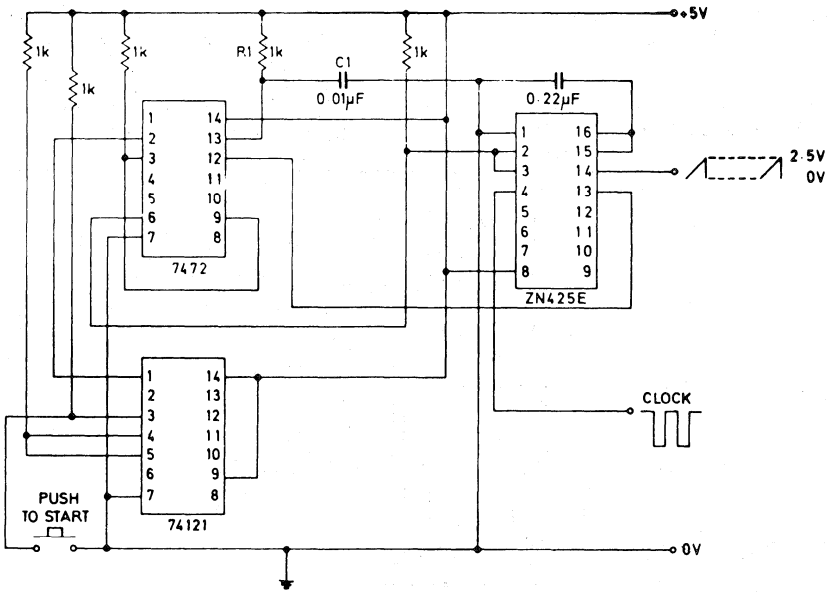



**Fig. 11d Alternative one shot circuit**

### 3.3 Weighing and auto zero

The system to be described is intended for either static or on-vehicle load indicating applications and employs integrated circuits from the Plessey Standard Product range. Variations of the scheme are indicated which increase its range of applications. The overall system is shown in the circuit diagrams of Figs. 12a to 12e.

The basic measuring function is a 3½ digit DVM using the dual slope analogue to digital converter principle. This displays an analogue input of up to ±1999mV which is scaled as required. All the DVM digital and control functions are carried out by a ZNA116E.

The DVM input is driven from a separate unity gain summing amplifier which accepts inputs from any number of channels each consisting of transducer and pre-amplifier.

Included in the system is a push button auto-zeroing circuit which automatically sets the output of the summing amplifier to zero. This facility eliminates any small zero errors which may have accumulated in the transducer and pre-amplifier chain or any false zero readings which can appear when on-vehicle systems are operated on uneven ground. For this function the ZN425E 8-bit digital to analogue converter is used. This monolithic integrated circuit also includes an 8-bit binary up-counter and a reference voltage generator and by clocking the counter a voltage ramp of 256 discrete steps is generated. This ramp is level shifted to become symmetrically bipolar with respect to 0V and then applied to the virtual earth of the summing amplifier. This forces the amplifier output through 0V and a comparator circuit detects the 0V condition and inhibits the clock pulses to the counter. The selected ramp output level is therefore held indefinitely unless the auto-zero is switched off when the system reverts to the original zero conditions.

Additional facilities include B.C.D. outputs for data logging purposes and an overload alarm system with warning indications.

The alarm system uses two comparators, into which are set two analogue levels, one corresponding to a preset percentage of full load and the other to full load. When the load reaches the first level a 1Hz square wave output is available and a separate output gives a continuous signal at the second level. These outputs may be wire-ORed or used separately to drive visual or audible alarms.

It is not essential for the DVM function to be fully bipolar in this application because negative readings occur only as small zero errors. A minor modification enables the circuit to display lower accuracy negative readings at the same time eliminating one of the ZN423 reference generators.

Further modification, appropriate for some applications, results in a 3 digit display with a 1Hz flashing leading zero to indicate a small negative zero error.

This approach, using a mix of standard function integrated circuits gives maximum system flexibility. For example, an on-vehicle application may require separate auto-zero functions on a number of axles or an overload alarm indication may require duplication. By adding the appropriate integrated circuits the system can be tailored to suit a range of vehicle requirements with a minimum of chip function redundancy and therefore minimum cost.

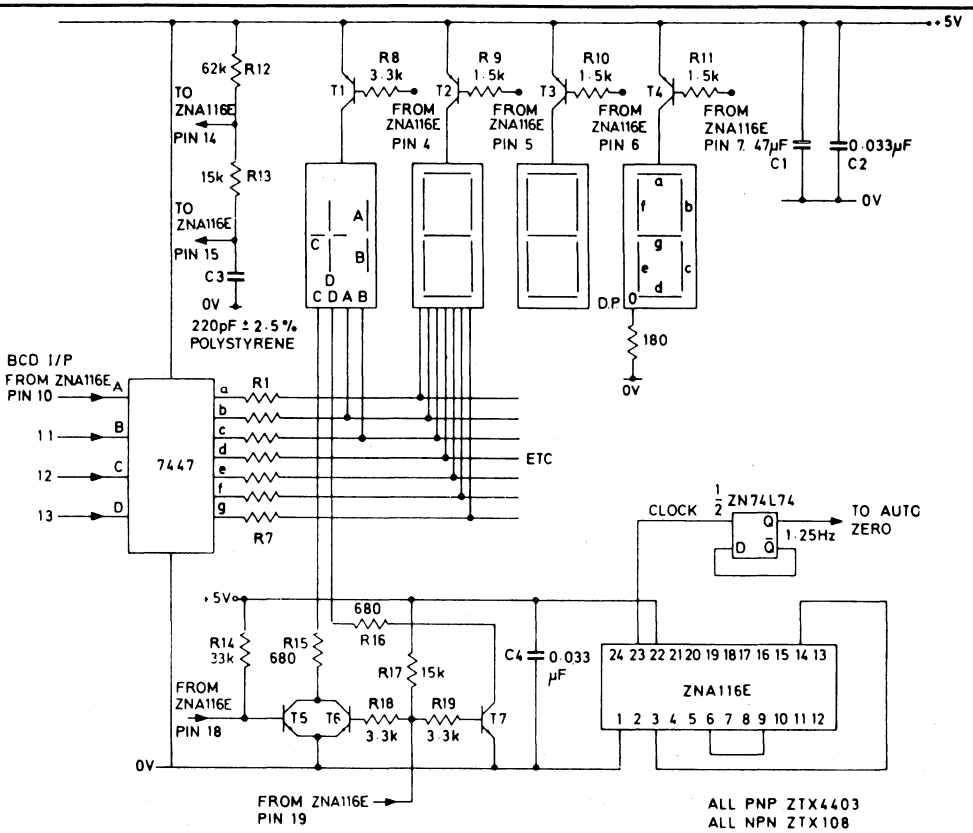



**Fig. 12a Display/digit circuit**

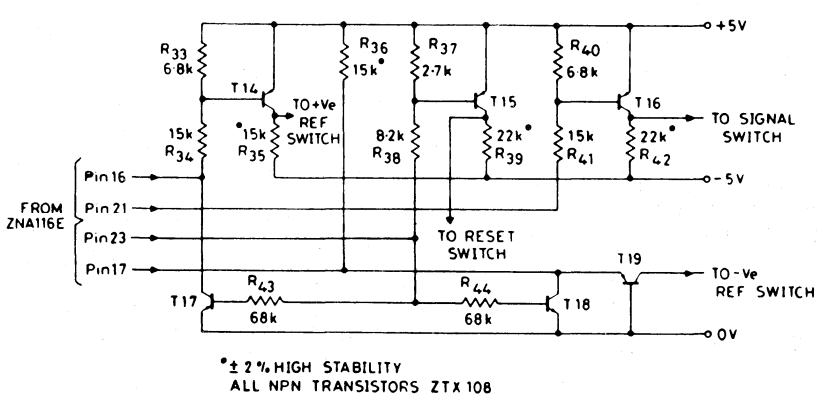



**Fig. 12b Analogue switch**

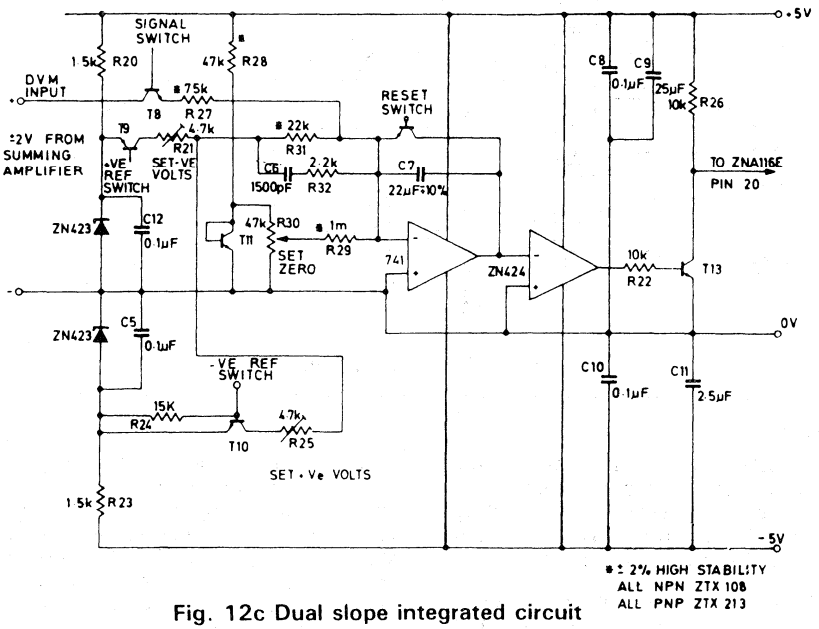



Fig. 12c Dual slope integrated circuit

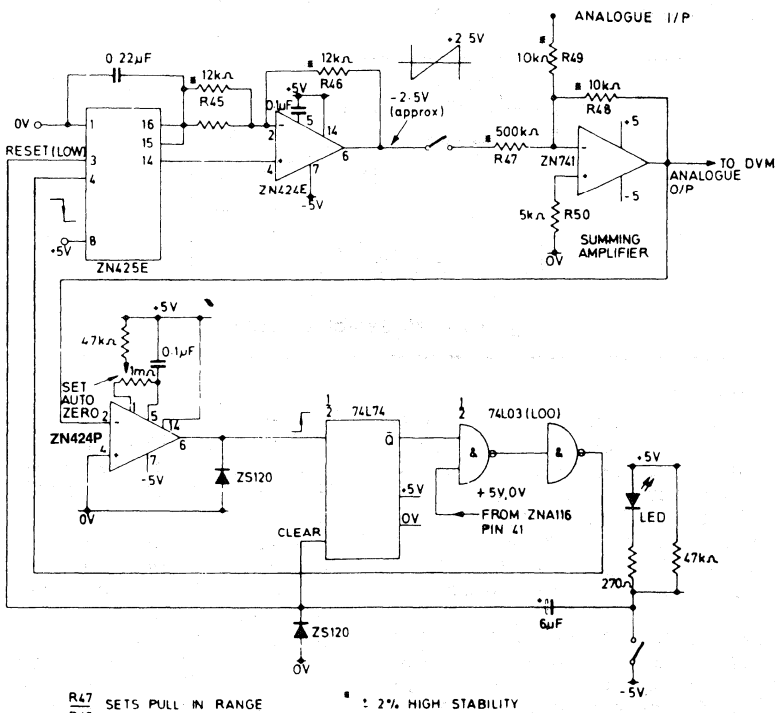



Fig. 12d Auto zero circuit

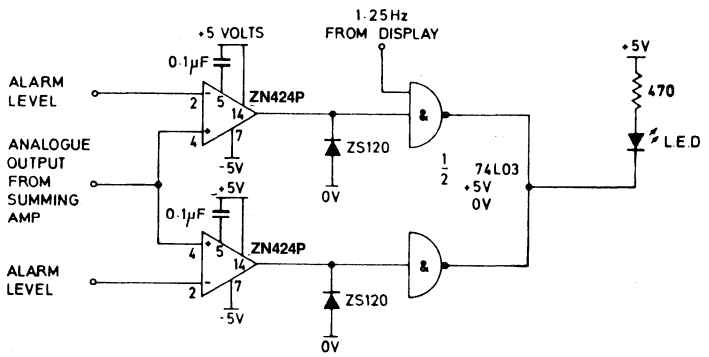



Fig. 12e Alarm circuit

### 3.4 Peak detect

A peak detect circuit may be constructed simply using the form of A to D system shown in the schematic of Fig. 13. When left running continuously it will hold the maximum input signal level it is able to track i.e. peak detect.

After application of a reset pulse, the state of the comparator enables clock pulses from the Schematic trigger circuit to be fed to the counter of the ZN425E. The analogue output begins to ramp up until it attains the level of the analogue input voltage at which point the comparator changes state and inhibits further clock pulses. Therefore, the analogue output is held and stored digitally in the bits of the converter. It will continue to hold this level until a further increase in analogue input voltage changes the comparator state, enabling the clock, and the sequence is repeated.

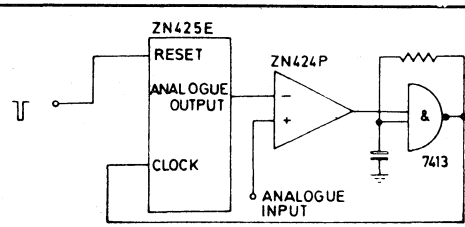



Fig. 13 Peak detect schematic

### 3.5 Channel Selector

Another interesting application of the A-D principle is for a channel selector in communications, e.g. citizens or amateur band. In effect it replaces a multiway switch, mechanically limited to 24 or 30 channels, by a 10 turn potentiometer which can be used with the system of Fig. 14 to generate many more discrete steps, typically 64 but up to 256.

The ZN425E with internal counter, provides the A-D conversion function, using a single 7400 package for external logic, and a high performance ZN424P op-amp as comparator. A 7413 dual Schmitt trigger provides the necessary clock and conversion oscillators, no sync is needed here. Channel selection is by the 10 turn potentiometer 'Main Tune' or, optionally, by preset potentiometers, to preferred channels. Resistance values for the pots are not critical.

The binary output is converted to BCD by the 74185 and latched to provide a steady output signal i.e. when a particular channel has been selected no jumps occur during cycling. The conversion oscillator periodically checks the state of the input voltage, by a fresh conversion on the ZN425E, and updates the latches when the status command indicates that the conversion is complete. The BCD signals drive

7-segment indication of channel number and provide the drive outputs for either a modulo-N digital synthesiser, a crystal-bank synthesiser, or a crystal selector. Features of the system are:

1. Bi-directional, quasi-continuous tuning on a single control.
2. Electronic tuning lock.
3. Simple switching between 'tune' and 'preferred channel' operation.
4. Preferred channels selected by preset potentiometers operating through to the synthesiser. Channels are user-alterable.
5. Inherent non-volatile 'memory' on potentiometers.
6. Channel number indication shows channel actually in use, particularly suitable for non-co-channel working, repeaters, etc.

In addition, a scanning facility can be easily added if the receiver used has a squelch switched output.

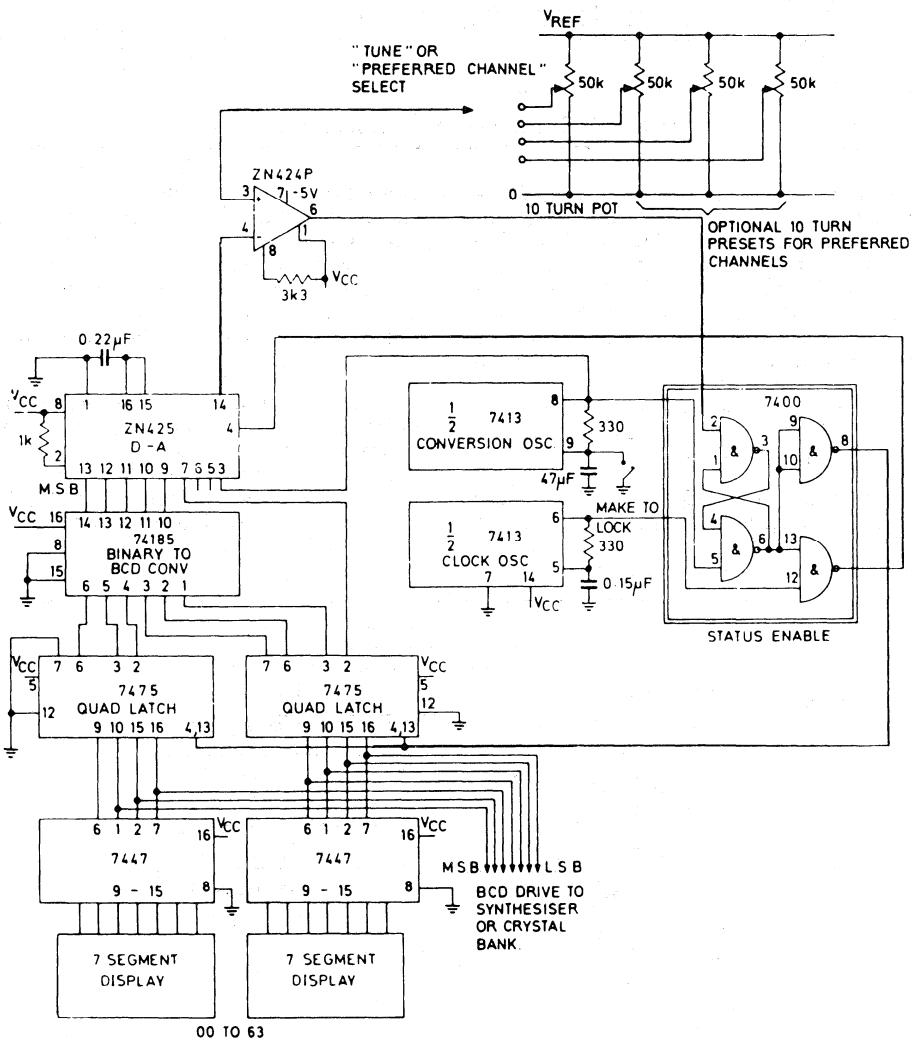



Fig. 14 Channel selector, 64 way

### 3.6 Bargraph display drive system

The ZN425E may be used in its continuous ramp mode very advantageously in conjunction with linear light emitting diode (LED) displays, e.g. Bargraphs. This is because the LED displays lend themselves to being accessed in a matrix fashion using a time sharing or multiplexing technique. This allows a reduction in the number of connections required, to m + n in an array of m n diodes (Fig. 15a). This reduction in connections also allows a simplification of the drive system, as described below.

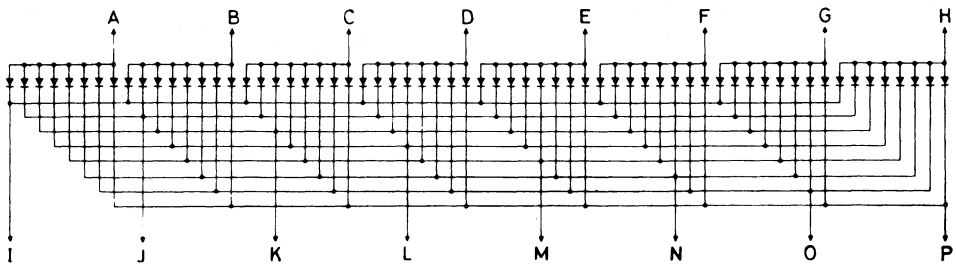



**Fig. 15a Diode matrixing connections**

The simplest techniques for providing for a bar output whose length is proportional to an analogue input is shown in Fig. 15b. The ZN425E is driven in its continuous ramp mode. The six most significant digits from the counter are then decoded into two lots of 1 out of 8 drives. These drives then access the LEDs in a multiplexed fashion, so that the 64 LEDs are accessed once each in turn in a complete scan cycle. A high clock frequency is selected which ensures that the flicker rate is fast enough and therby indistinguishable to the eye.

At the same time as the LED scan cycle is taking place, the ZN425E provides a staircase analogue output, as shown. This is compared with the analogue input in a comparator, whose output controls the display enable. Thus while the ramp is less than the analogue input, the LEDs being scanned are enabled (the start of the Bargraph line), while once the ramp output is larger than the analogue input, the drives to the LEDs further along the line are inhibited. This, therefore, provides an illuminated bar length proportional to the analogue input.

This system as it stands suffers from a minor disadvantage, in that the duty cycle for accessing each LED is 1/m n, or 1/64 for the case of Fig. 15b. Although the LEDs become more efficient with pulsed operation, 1/64 duty cycle does not provide adequate brightness for some applications.

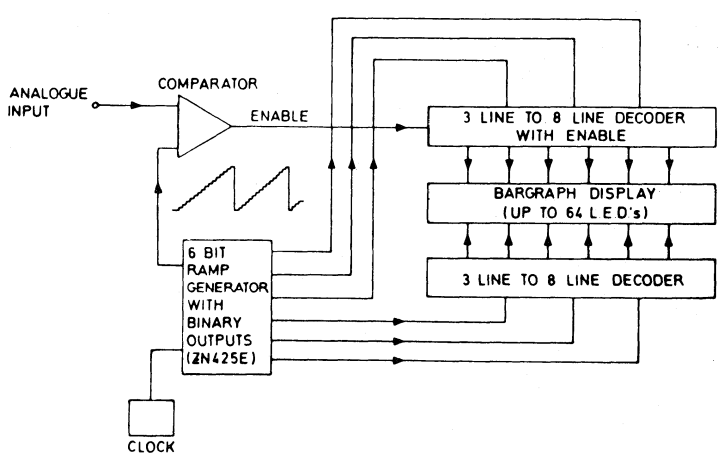



**Fig. 15b Simple bar display schematic drive system**

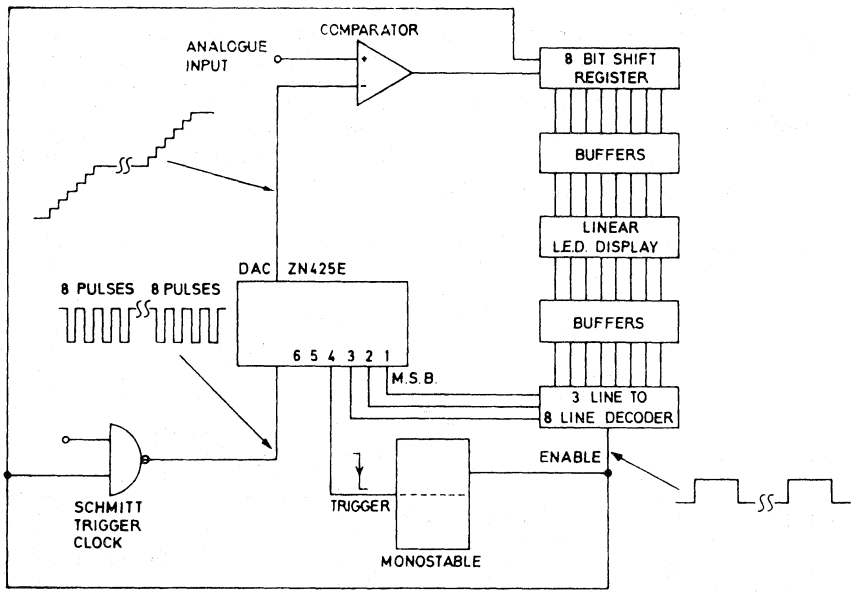



**Fig. 15c Improved bar display schematic drive system**

A technique to overcome this objection is shown in outline in Fig. 15c. The technique used here is to load a shift register rapidly serially, and subsequently use this register to provide LED multiplex drives in parallel. This means that the duty cycle for accessing the LEDs is improved (for a 64 LED array) from 1/64 to just less than 1/8. This is quite sufficient for acceptable brightness in virtually all applications.

This system operates as follows. While the monostable is in its mode of loading the shift register, the ZN425E staircase output increases in 8 discrete steps. Simultaneously the shift register is loaded with the comparator output to provide serial to parallel conversion. The comparator output is thus effectively changed from serial access to parallel access of the linear LED array.

When the monostable changes over to its (longer period) display mode, the LED array is accessed, and the LEDs are driven or otherwise according to the enable or disable information stored in the shift register. The display is incidentally disabled while the mono is loading the register.

To provide an example of operation, suppose the bar is to have the first 37 LEDs displayed, with the rest blanked. Starting from the ZN425E being reset and the mono in its register load state, operation is as follows.

The mono allows eight clock pulses through the gate to the ZN425E, after which the ZN425E count pulse retriggers the mono. These eight pulses generate the first eight steps from the analogue output, which produce from the comparator a continuous display enable (say logic 1). These are loaded into the shift register which thus finishes with 11111111 in parallel to the LED display.

At this point the mono is tripped into its display mode, and the counter has reached 8 (or 001 000). However the decoder must access the first eight LEDs, so that the second decoder output is connected to the first set of LEDs. These are all illuminated.

During the second register load period, the cycle is repeated, with again all ones being loaded into the register which subsequently brightens up the second eight LEDs (9-16). The same occurs during the third and fourth mono cycles, lighting up the first 32 LEDs.

During the fifth register load period, the analogue output goes up a further eight steps. However after the fifth step the comparator changes over to load zero for the remainder of this period into the shift register. If loaded from the left the register will then finish up as 00011111. Subsequently during the mono display period LEDs 33 to 37 inclusive will be lit, but 38 to 40 will be blanked off.

The sixth to eighth mono cycles will load zeros into the shift register, blanking off LEDs 41 to 64. The full LED scan cycle is therefore completed with the desired effect.

Typical system clock rates are 400kHz, and typical monostable periods 500$\mu$s for the values shown.

An actual circuit to achieve this is shown in Fig. 16 and it may be seen that this is elegant and simple. The type of display which may be accessed in this way is the Bowmar Microstic R1M-053-66A, which is connected in eights on its common anodes. This has 64 red LEDs and a further two LEDs at the ends, one to show the display is working, and the other for over-range. Similar techniques may be used with the 106 LED version.

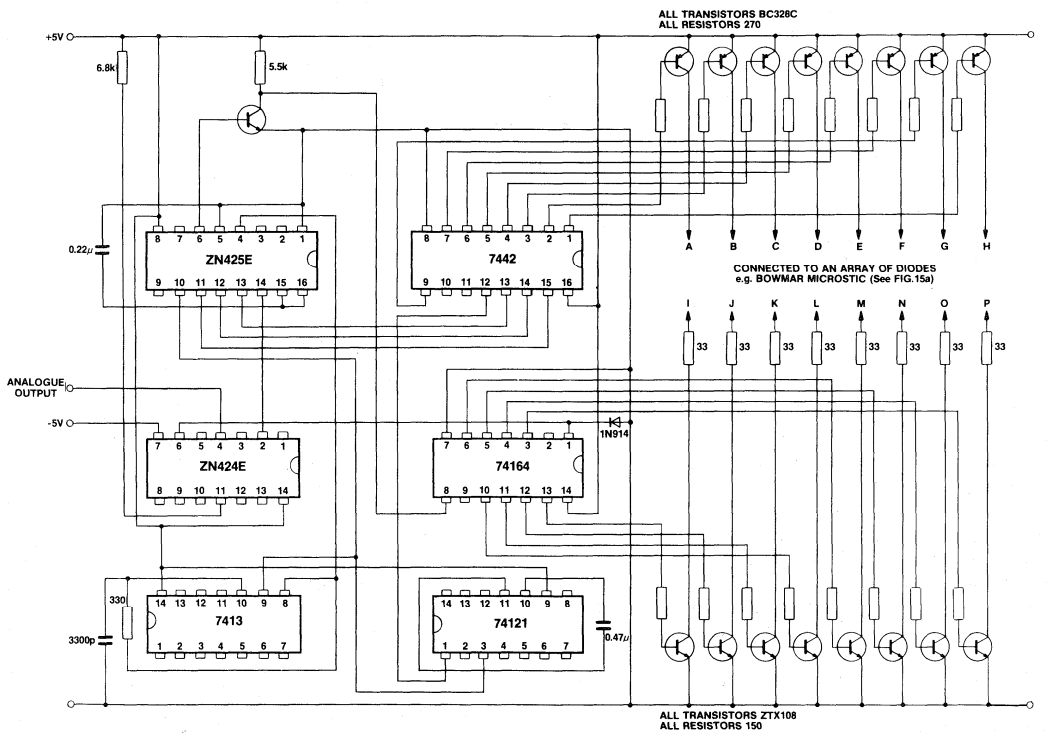



**Fig. 16 Column display drive system**

### 3.7 Up down or tracking

The counter on the ZN425E is only an up counter, and some systems, e.g. tracking converters or servos, amy require an up/down counter. This is conveniently provided externally, e.g. the 74193 using the ZN425E purely in its D-A converter mode and ignoring the counter (Fig 17). While this may appear to be inelegant it is nevertheless economically sound.

The reference supply to the D-A section of the ZN425E has been purposely left on an uncommitted terminal, so as to allow connection either from its own reference or from an external reference. The point about an external reference is that it allows a multiplying effect, in that the analogue output is proportional both to the binary code and the reference voltage. For this reason this type of DAC is called a multiplying DAC.

Practical limits in multiplying voltages are 0 and 3V.

## 4. MULTIPLY/DIVIDE

### 4.1 Multiplier

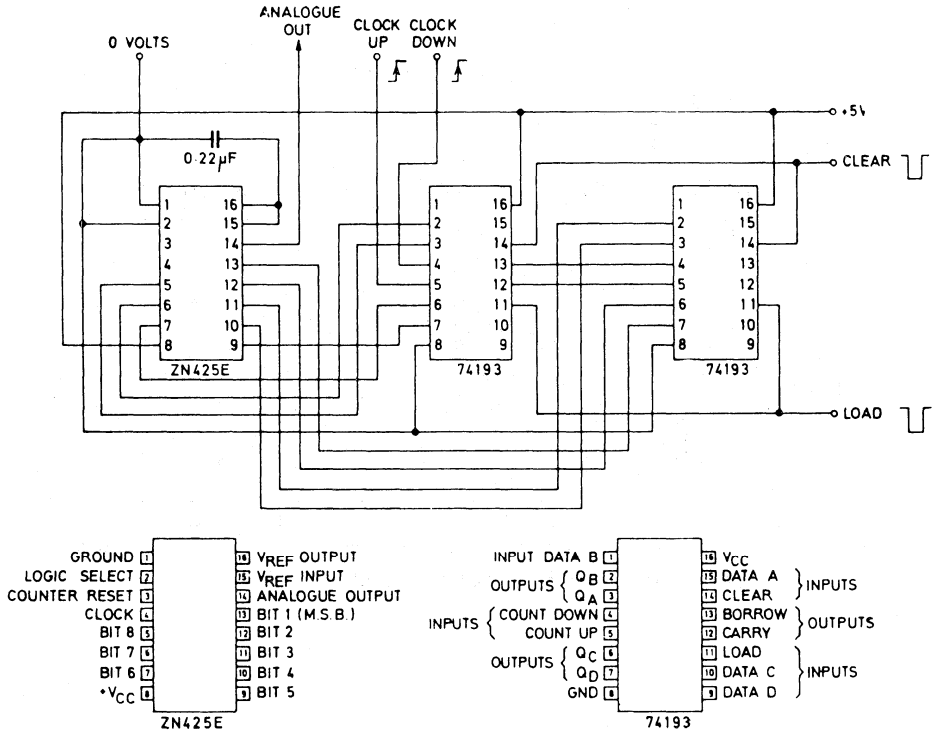



**Fig. 17 Up/down counter or tracking DAC circuit**

### 4.2 Variable frequency divider

If a ZN425E is operated in its continuous ramp mode in conjunction with a comparator whose output is fed back to the counter reset, a variable frequency divider can be constructed as shown in Fig. 18a. Here an analogue voltage can be used to control the number of steps before reset is applied, the overall effect being to provide variable frequency division under the control of a potentiometer.

### 4.3 Voltage controlled oscillator

The schematic of Fig. 18a may also be used as a voltage control oscillator. However the frequency is the inverse of the applied voltage, though the period is, of course, proportional. The corresponding circuit of Fig. 18b gives an output frequency or pulse rate which is inversely proportional to applied voltage as shown in Fig. 18c. It is, however, in some cases more desirable to produce an output frequency directly proportional to applied voltage. This is accomplished by the circuit depicted in Figs. 19a and 19b and involves the use of an inverse scaler described in the next section, for which a brief mention is necessary to understand the basic operation of the VCO.

By using a DAC in the feedback loop of an operational amplifier an output voltage is derived which is inversely proportional to a digital input number to the DAC. Clock pulses applied to the DAC counter will produce a repetitive output waveform which is a hyperbolic $\frac{1}{n}$ function. This waveform is applied to the inverting input of a comparator whilst the analogue input voltage to be frequency converted is applied to the non-inverting input. At the instant they become equal the comparator changes state and operates the Schmitt trigger which resets the DAC counter. The result is a train of negative going pulses whose frequency is directly proportional to the applied input voltage. This follows simply because if $F_{Clock}$ = clock frequency to the DAC counter, and $F_{out}$ = output frequency, then $F_{out} = \frac{F_{Clock}}{n}$ where n = digital input number and analogue input voltage to the comparator $V_{in} \propto \frac{1}{n}$

Therefore, $F_{out} \propto V_{in}$ and the appropriate characteristic is shown in Fig. 19c.

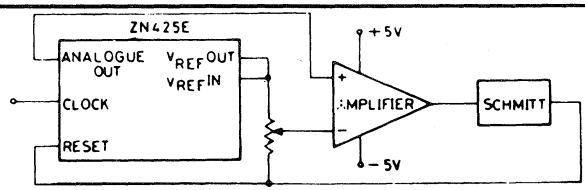



Fig. 18a Variable frequency divider or VCO schematic

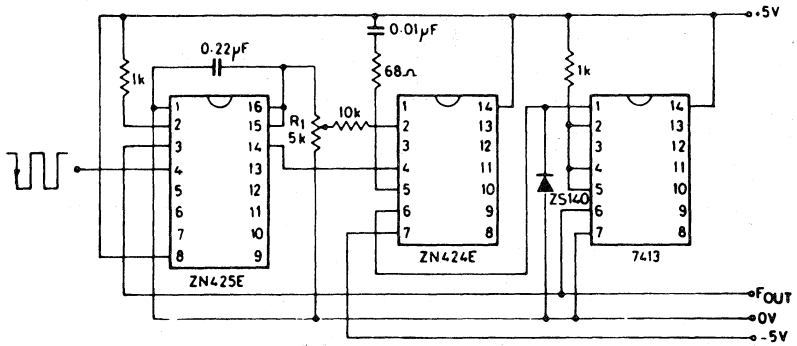



Fig. 18b Variable frequency divider or VCO circuit

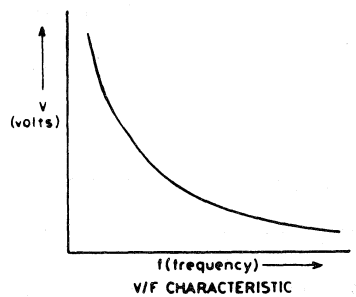



Fig. 18c VCO characteristics

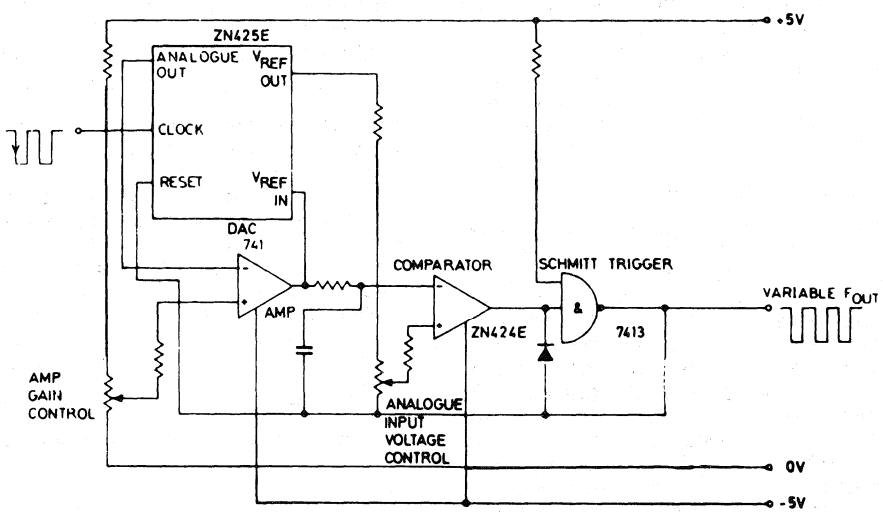



Fig. 19a Schematic of VCO giving frequency proportional to voltage

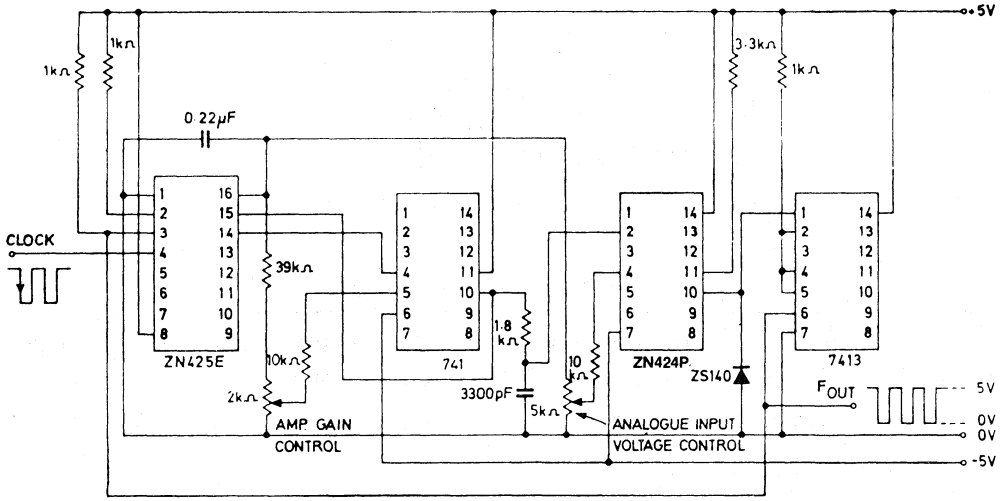



Fig. 19b Circuit of VCO giving frequency proportional to voltage

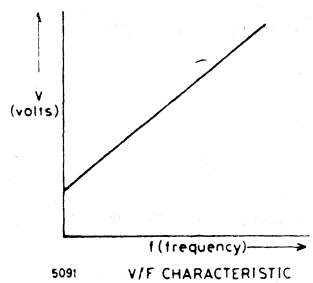



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Fig. 19c VCO characteristics

## 5. FUNCTION GENERATION

By virtue of the multiplying function, the ZN425E may also be used for function generation as described below.

### 5.1 Inverse scaler

If a DAC is operated in the feedback loop of an operational amplifier then the amplifier gain is inversely proportional to the input digital number or code to the DAC. The version giving scaling inversely proportional to positive voltage is shown in the schematic of Fig. 20a and the practical circuit of Fig. 20b.

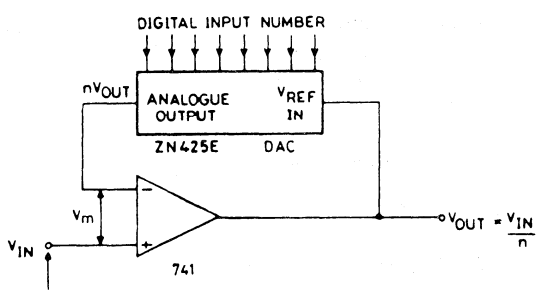



Fig. 20a Inverse scaler schematic

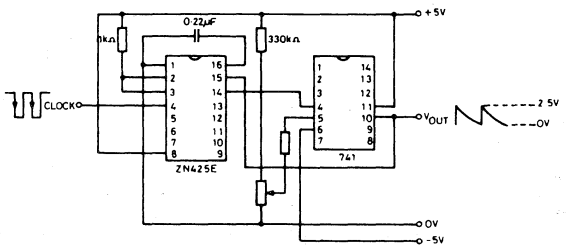



**Fig. 20b Inverse scaler circuit**

If A = open loop gain of the operational amplifier, and n is a fractional number representing any digital input (00000000 to 11111111 for 8 bits), that is a fractional number between 0 and $\frac{255}{256}$ then from the diagram $V_{out} = AVm$, and $Vm = (V_{in} - n\,V_{out}) \therefore V_{out} = A(V_{in} - n\,V_{out})$ from which

$$V_{out}(1 + An) = AV_{in} \quad \frac{V_{out}}{V_{in}} = \frac{A}{1 + An}$$

Since $An \gg 1$, $(A \simeq 100{,}000)$ then $\frac{V_{out}}{V_{in}} = \text{Gain (G)} \simeq \frac{A}{AN} = \frac{1}{n}$

For $n = 1LSB = \frac{1}{256}$ then the maximum allowable input voltage $V_{in}$ to prevent saturation

$(V_{sat} \simeq 4V) = \frac{4}{256} \simeq 15mV.$

If n = 0 then G = A and for a fixed input level the amplifier output will normally be equal to the saturation voltage since $A \simeq 100{,}000$.

The complementary mode (scaling inversely proportional to negative voltage) is shown in Fig. 20c (schematic) and Fig. 20d (practical circuit).

$$V_m = \left[V_{in} - \left(\frac{V_{in} - n\,V_{out}}{R_1 + R_F}\right)\right], \text{ and } V_{out} = -AV_m$$

If $\frac{R_I}{R_F} = F_I$ = inverting feedback return then

$$V_{out} = -A\left[V_{in} - \left(\frac{V_{in} - n\,V_{out}}{1 + F_I}\right) F_I\right]$$

From which

$$V_{out} = -\left[\frac{A\,V_{in}}{1 + F_I + nAF_I}\right]$$

If the input voltage $V_{in}$ is negative with respect to ground, then

$$\text{Gain (G)} = \left[\frac{A}{1 + F_I + nAF_I}\right]$$

If we make $F_I = 1$, i.e. $R_I = R_F$ then $G = \left[\frac{A}{2 + nA}\right]$

But $nA > 2$ (since $A \simeq 100{,}000$)

and $G = \frac{A}{nA} = \frac{1}{n}$ as with the non-inverting circuit.

Figs. 20a and 20c illustrate both types of inverse scalers, where a repetitive waveform of a $\frac{1}{n}$ function is generated by feeding clock pulses to the counter of the DAC.

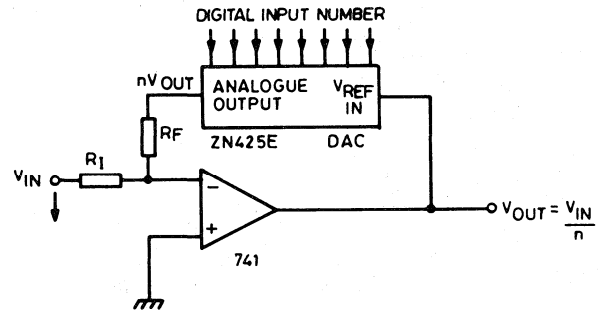



Fig. 20c complementary inverse scaler schematic

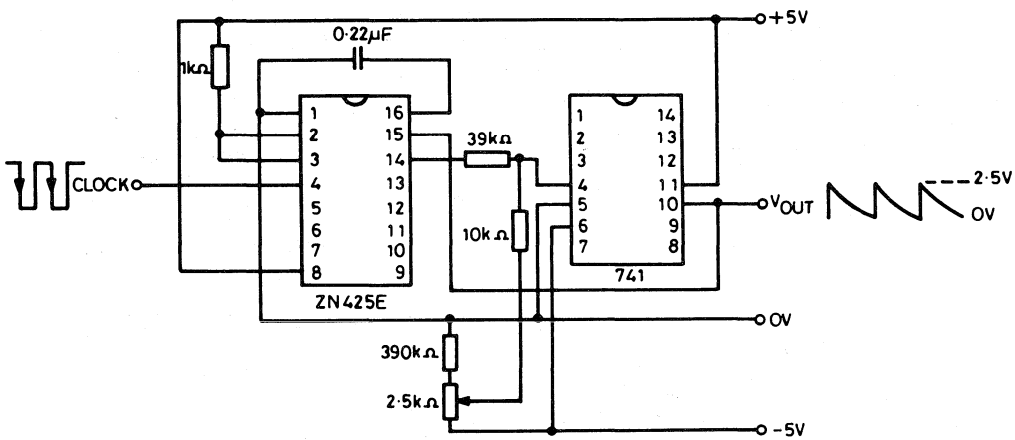



Fig. 20d Complementary inverse scaler circuit

### 5.2 Parabola

The multiplying action of the ZN425E may be used to generate a parabolic waveform shown schematically in Fig. 21a and a practical circuit Fig. 21b.

Basically the circuit operates as follows;

A continuous ramp output is generated by feeding clock pulses to the counter of a ZN425E DAC using its internal reference which is buffered, level shifted, and finally inverted using two operational amplifiers, so that the inverted ramp starts at a peak amplitude ($V_{1\ REF}$ = 2.5V) and decreases linearly to zero. This is then used as an external reference supply for a second ZN425E DAC whose bits are connected to the first DAC for synchronous clocked operation. The resulting analogue output from the second DAC is a repetitive parabolic waveform whose peak amplitude is equal to $\frac{V_{1\ REF}}{4} = \frac{2.5}{4} = 0.625V$.

This follows because,

If N = a fractional number representing the digital input to both DACs then the analogue output voltage from the first DAC = An (where A = $V_{1\ REF}$ = 2.5V).

This is then inverted and level shifted to provide the reference voltage to the second DAC = (A − An) = $V_{2\ REF}$.

Therefore the analogue output from the second DAC = n (A-An) = An − $An^2$ which is the equation of a parabola about the x axis of the form $y = ax^2 + bx + c$.

Peak amplitude of the parabola occurs when n = $\frac{1}{2}$

for which $V_{out} = \frac{1}{2}\left|A - \frac{A}{2}\right| = \frac{A}{4} = \frac{V_{1\ REF}}{4}$ as stated.

It should be noted that the ramp output from the non-inverting buffer amplifier will inherently have a gain greater than unity, and therefore its peak amplitude will be some factor in excess of $V_{1\ REF}$. However the ramp inverter and level shifter introduces corresponding attenuation to compensate this so that gain and level shift controls provide adequate adjustment in obtaining the desired inverted ramp output of peak amplitude.

$A = V_{1\ REF} = 2.5V.$

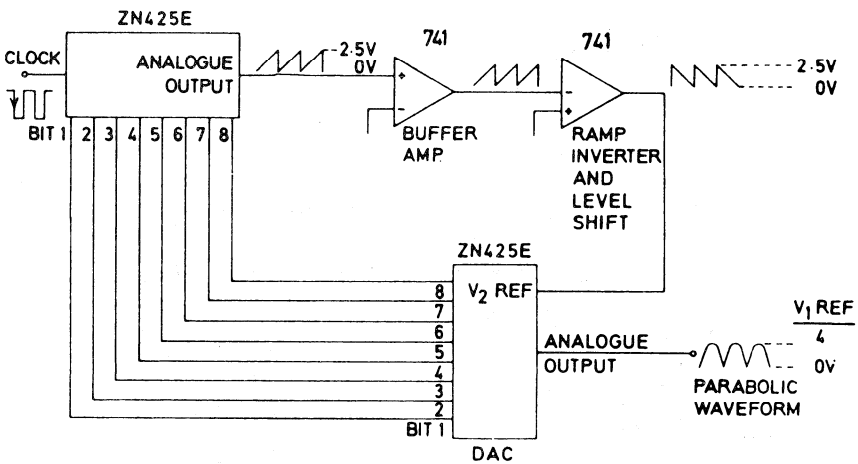



Fig. 21a Parabolic waveform generator schematic

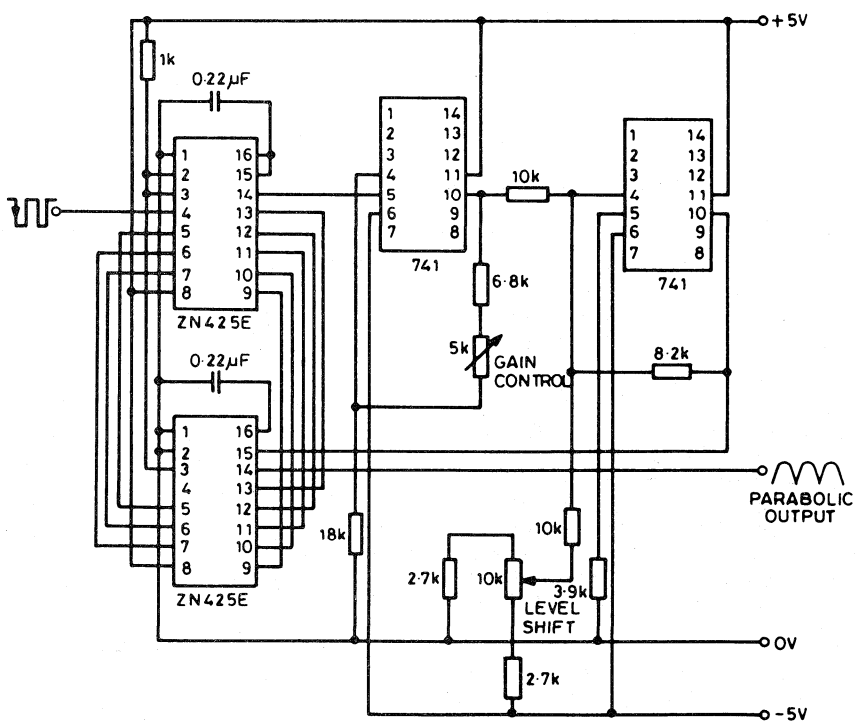



Fig. 21b Parabolic generator circuit

### 5.3 Log Approximation

A more complex function y = log n can be performed with the aid of previously described building blocks. A schematic arrangement as shown in Fig. 22a and the corresponding practical circuit of Fig. 22b provides a repetitive logarithmic relationship. The basic method is as follows.

An inverse scaler is used to generate an output voltage which is inversly proportional to a digital input number n to a ZN425E DAC. This voltage is then converted to a frequency or pulse rate using a VCO whose output frequency is proportional to an applied voltage. The derived train of pulses of varying mark to space ratio are then fed into the counter of a final ZN425E DAC, these are integrated and a logarithmic output

$$\left(\frac{1}{n}\,dn = \log n\right) \text{ is obtained.}$$

The period of the analogue $\frac{1}{n}$ function is dependent upon the input frequency to the inverse scaler. To rapidly convert this function to a pulse train and to generate a sufficient number of pulses for integration during this period, the clock frequency to the VCO derived from the Schmitt trigger must be high. The lower input frequency to the inverse scaler in synchronism with this clock frequency is obtained by using two 7493 dividers and equals the clock frequency divided by 256. For the CR values indicated in the Schmitt trigger $F_{Clock} \simeq 512kHz$ therefore the input frequency to the inverse scaler $= \frac{512 \times 10^3}{256} Hz = 2000Hz.$

And the output repetition frequency of the $\frac{1}{n}$ function $= \frac{2000}{256}$ Hz, for which the period $= \frac{256s}{2000} = 128ms.$

Some means must be incorporated of resetting the counter on the final ZN425E DAC and thereby the logarithmic analogue output to zero at the completion of a full cycle of input pulses. Otherwise the analogue output would continue to increase with each cycle of pulses until it equalled the internal reference voltage, resulting in a 3 cycle logarithmic waveform. This is accomplished by using the negative going edge from the 4th significant bit which in fact resets the counter on the final DAC the completion of a full cycle of input pulses. Whereas to be strictly correct resetting should be effected from the MSB; bit 4 having been selected purely for convenience as it allows the logarithmic characteristic to be more easily displayed on the oscilloscope, since it accounts for a greater proportion of the output waveform, with negligible loss in amplitude.

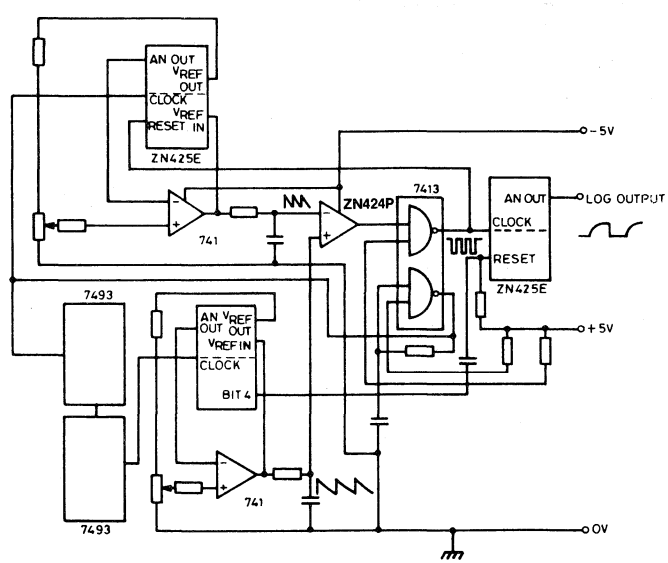



**Fig. 22a Logarithmic waveform generator schematic**

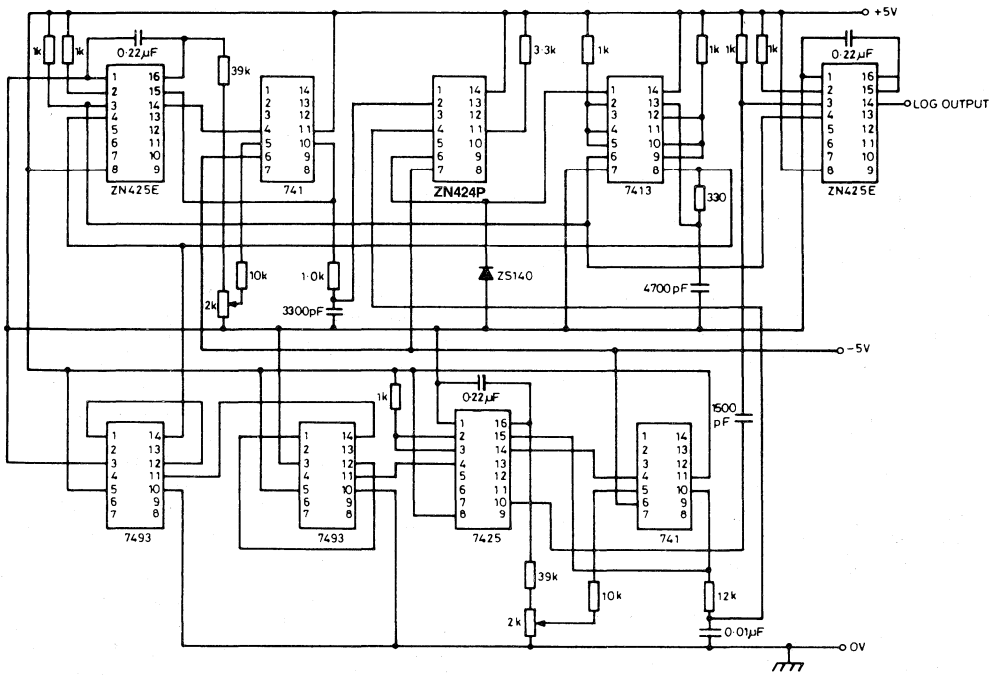



Fig. 22b Logarithmic waveform generator circuit

# Microprocessor Interfacing using the ZN427/ZN428 Data Converters

**Conventional analogue I/O systems for Microprocessors are generally high accuracy, high cost, hybrid module/P.C. board assemblies, available in only one fixed configuration of I/O channels, (i.e. 16 Input and 2 Output channels). This application note describes how a low cost analogue I/O system may be produced for the 6800 microprocessor using Plessey ZN427 A-D and ZN428 D-A converters with the 6820/6821 peripheral interface adaptor (PIA) I.C. This combination produces a versatile system which can be configured to the designer's particular I/O requirements, and which can also be expanded without major modifications to the hardware. The advantages of interfacing to the microprocessor via the PIA are that it provides a simple, easily expandable system, without additional address decoding and line buffering hardware, and it also simplifies timing problems associated with a direct bus interface.**

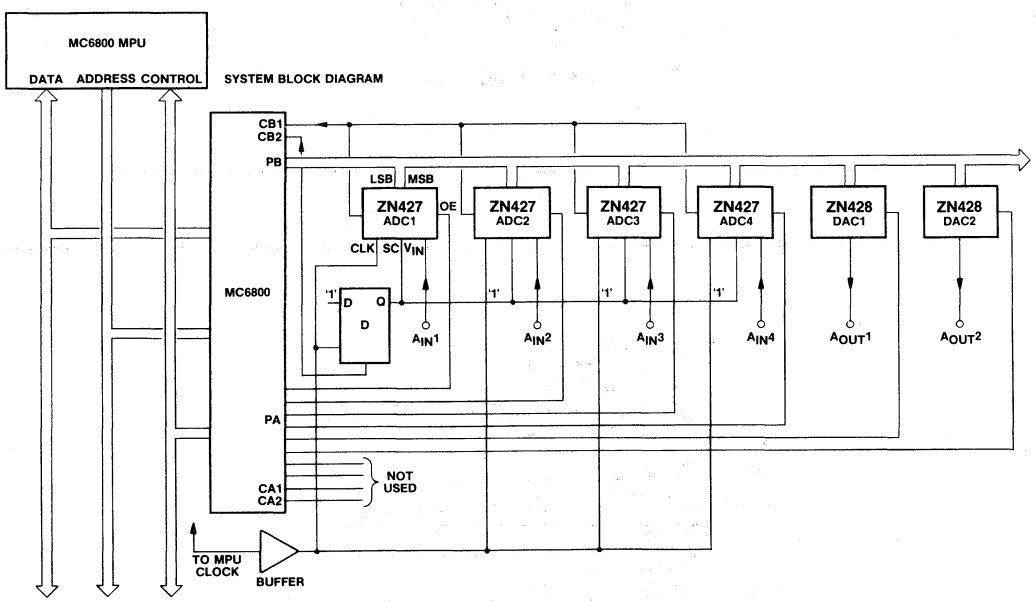



Fig. 1 System block diagram

### The ZN427 A-D converter

The ZN427 is an 8-bit, successive approximation A-D converter. It features fast 15$\mu$s conversion time, three-state outputs to permit bussing on common data lines and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D-A converter, a 2.5V precision band gap reference, a fast comparator, successive approximation logic, and three-state output buffers.

Operation of the ZN427 is best described with reference to the timing diagram - Fig. 3. Conversion is initiated by a START CONVERT (SC) pulse which can be applied asynchronously with respect to the ZN427 clock providing the following criteria are met.

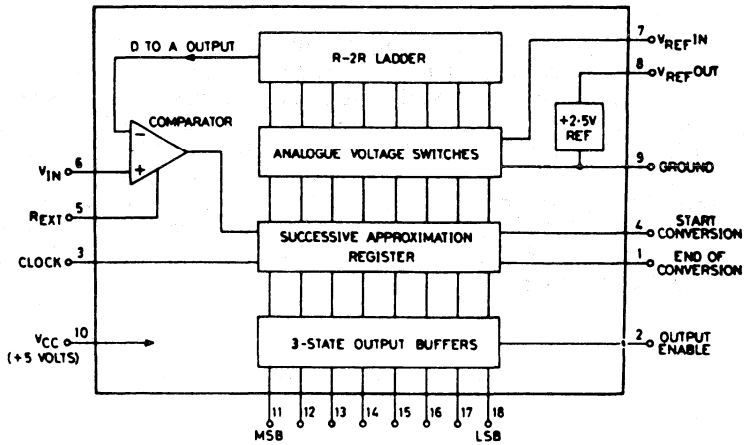



Fig. 2 ZN427 logic diagram

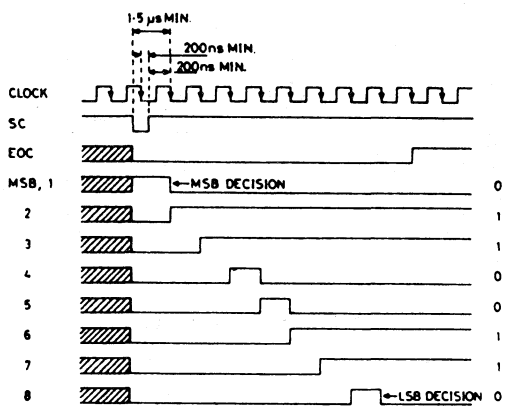



Fig. 3 Timing diagram

1. The leading edge of the SC-pulse should precede the first active (negative going) edge of the clock (after the trailing edge of the SC pulse) by at least 1.5$\mu$s to allow for MSB setting.

2. The trailing edge of the SC pulse must not occur within $\pm$ 200ns of a negative going edge of the clock.

3. As a special case of conditions (1) and (2) the SC pulse may be coincident with, and of the same duration as, a negative going clock pulse. Application of the SC pulse sets MSB to a '1' level and all other bits to a '0', which produces a voltage output from the D-A converter of $V_{REF\ IN/2}$.

This value is compared with the input voltage $V_{IN}$, and a decision is made on the first negative clock edge to set the MSB to '0' if $V_{REF\ IN/2} > V_{IN}$, or else to keep it at '1', Bit 2 is switched to '1' on the same clock edge, and on the next edge a decision is made about Bit 2, again by comparing the D-A output with $V_{IN}$. This process is repeated for all eight bits so that when the END OF CONVERSION (EOC) output goes high the digital output from the converter is a valid representation of $V_{IN}$. The binary output is latched until the next START pulse. The three-state data outputs are OFF (high impedance) when OUTPUT ENABLE (OE) is an '0' and are enabled when the OE input is taken to '1'.

**The ZN428 D-A converter**

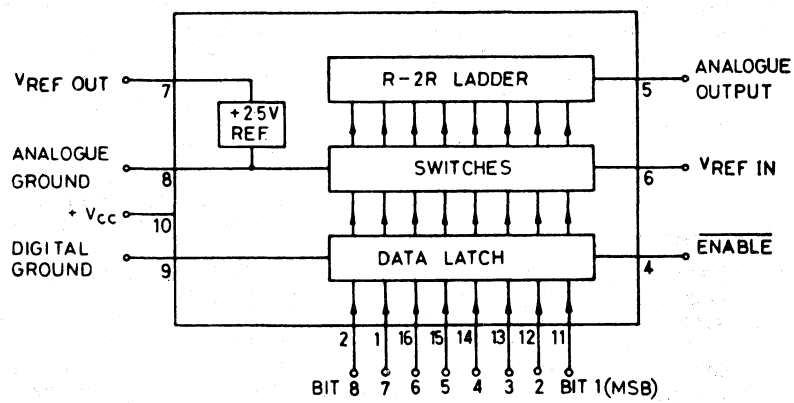



**Fig. 4 Logic diagram**

The ZN428 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when ENABLE is at logic '0' and the data is held when ENABLE is taken to logic '1'. The ZN428 features single + 5 volt supply requirements, fast 800ns settling time and is guaranteed monotonic over the full operating range. It also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted. The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network the nominal output range of the ZN428 being 0V to $V_{REF\ IN}$ through a 4k$\Omega$ resistance. Other output ranges can readily be obtained by using an external amplifier.

### The 6800 microprocessor system

It is assumed that the reader is fully conversant with the 6800 microprocessor family, information on which can be found in the Motorola M6800 microprocessor applications manual, so only a brief description is given here.

The 6800 is an 8-bit monolithic microprocessor which forms the central control function for the 6800 microprocessor family. Fully compatible with TTL the 6800 requires only a single + 5 volt power supply, it features an instruction set of 72 instructions with 7 addressing modes and full 65k byte memory addressing capability. The microprocessor communications with its external memory and all I/O devices via an 8-bit bi-directional data bus and a 16-bit address bus.

The 6820/21 peripheral interface adaption (PIA) provides a flexible means of interfacing byte-orientated peripherals to the microprocessor, through two 8-bit bi-directional peripheral data lines and four control lines. The functional configuration of the PIA is under the full control of the microprocessor. Each of the peripheral data lines can be programmed to act either as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

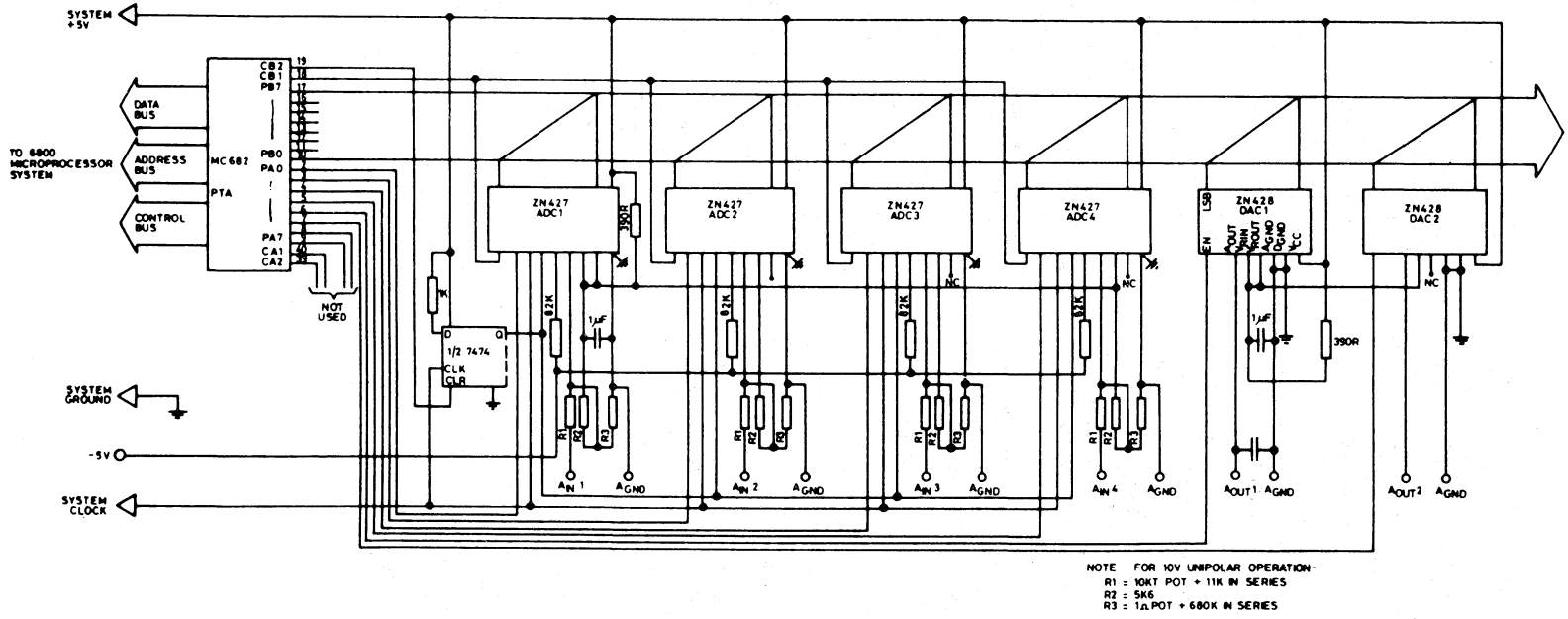
### The analogue I/O interface

The system described in this application note provides 4 analogue input and 2 analogue output channels - see the system block diagram Fig. 1 and the detailed circuit diagram Fig. 5. Other configurations can easily by produced - these are discussed later in this note.

The peripheral data lines PB0-PB7 of the PIA are connected to the binary data outputs of the ZN427s and the data inputs of the ZN428s to produce a common 8-bit data bus for the converters. Peripheral lines PA0-PA5 are programmed as OUTPUTS and provide individual OUTPUT ENABLE AND $\overline{\text{ENABLE}}$ signals for the ZN427 and ZN427 respectively. A common, simultaneous START CONVERT signal for the ZN427s is produced from the CB2 control line program in the SET/RESET output mode and used in conjunction with a 'D' type flip-flop. The END OF CONVERT outputs from the ZN427s are commoned together and drive the CB1 input of the PIA which can be programmed to generate a microprocessor interrupt signal. In this system configuration, the peripheral lines PA6, PA7 and the control lines CA1, CA2 are not used.

The ZN427 clock signal can be generated either asynchronously from an external source or from the microprocessor clock. If using the MC6871B microprocessor clock device (as supplied with the Motorola MEK6800D2 evaluation kit), which produces a 614.4kHz clock signal, then the ∅2 TTL output of this can be used directly. Note that the maximum lock frequency of the ZN427 is specified as 600kHz, although the device will function up to greater than 1MHz, but at reduced accuracy due mainly to the response time of the comparator. Therefore, if using a microprocessor with a clock frequency greater than 600kHz, then this can either be divided down to less than 600kHz, or it may be used directly up to approximately 1MHz if some loss of accuracy can be tolerated. The advantage of using the microprocessor clock over an external clock is that it allows an accurate calculation of the conversion time to be made in terms of the microprocessor machine cycles eliminating the need to use microprocessor interrupts.

The START CONVERT pulse is generated using a 'D' type flip-flop (½ SN74L74) in order to meet the timing requirements discussed earlier. A conversion cycle is initiated by outputting a logic '0' followed by a logic '1' from the CB2 line of the PIA. This drives the CLEAR input of the 'D' type and sets the START CONVERT (SC) input of each 427 to a logic '0' via the Q output. The first positive going clock edge after the CLEAR input is returned to a logic '1' will clock the 'D' type and set the SC input of each ZN427 at a '1' allowing the conversion cycle to proceed. Note that while the SC input of the ZN427 is at a logic '0' level the MSB output will be driven to a logic '1' and all other data outputs to a logic '0' and the conversion cycle will be held. On the 9th negative clock edge after the START pulse the END OF CONVERSION outputs will go to a logic '1' signifying the end of the conversion cycle. This can be detected by programming the PIA to set the microprocessor interrupt input on the positive going edge of the CB1 control line. The EOC outputs of up to four




NOTE FOR 10V UNIPOLAR OPERATION-
R1 = 10KT POT + 11K IN SERIES
R2 = 5K6
R3 = 1Δ POT + 680K IN SERIES

Fig.5

ZN427's can be 'wire-or'd' together to produce a common interrupt line as shown in Fig. 5. Alternatively, if using the microprocessor clock (at up to 1MHz), then the EOC output will always occur within 10 microprocessor machine cycles after the instruction setting the CB2 control line back to a logic '1'. A suitable fixed delay can therefore be built into the program to allow for the conversion time.

The binary output data of each ADC can be read by programming the peripheral lines PB0-PB7 as INPUTS and loading the data onto the converter bus by outputting a logic '1' on the appropriate PA peripheral line in order to enable the 3-state output buffers of the ADC. A microprocessor read instruction on the PIA peripheral register 'B' will then transfer the data to the microprocessor. Obviously the program should be so arranged that, in order to avoid bus connection problems, only one ADC is enabled at any one time.

The circuit diagram Fig. 5 shows the ZN427s connected for a unipolar input range of 0 to +10 volts. Other ranges, e.g. +5V, ±10V and ±5V, can readily be obtained by using a simple resistor network as shown in the ZN427 data sheet.

The negative supply shown for the ZN427 is from −5 volts through an 82kΩ resistor. By suitable choice of resistor value any negative supply between −3 and −30 volts may be used. For applications where only a single +5 volt supply is available, a simple diode pump circuit can be used to generate the negative supply. Further information on the negative supply and a diode pump circuit suitable for up to 5 ZN427s is shown in the data sheet.

Data is output from the system by programming the peripheral data lines PB0-PB7 as OUTPUTS and wiring the binary data from the microprocessor into the PIA peripheral register 'B'. The ENABLE input of the relevant ZN428 is driven to a logic '0' and back to logic '1' via the appropriate PA peripheral line, which will transfer the data from the converter bus to the input data latches of the ZN428. Again the programmer must ensure during an output data transfer that all the ZN427s and the other ZN428 are disabled.

The analogue outputs of the ZN428 are shown, taken directly from pins 5 and 8 which will provide an output range from 0 volts to $V_{REF\ IN}$ through a 4kΩ output resistance. A small capacitor can be connected across the output pins as shown in order to remove any "glitches" which may be present. The value of this capacitor depends on the system noise and the response time required, however for the minimum specified settling time it should not be greater than 100pF. An output buffer amplifier was omitted from the ZN428 design in order to allow optimum settling time, flexibility and lowest cost. Both unipolar and bipolar output ranges can readily be obtained by using an external amplifier, details of which are given in the ZN428 data sheet.

The ZN428 is provided with separate analogue and digital ground pins. These can normally be connected together close to the device and taken to signal ground. However for noisy systems or environments it may be advisable to keep the analogue ground pins for each individual ZN428 separate from the digital ground pin, and to connect each analogue ground to a single common earth point in the system away from sources of digital noise such as clock oscillators, digital buses, etc. The analogue output ground line or terminal should also be taken direct to this common earth point. (Note: The maximum voltage between analogue and digital grounds is limited to 200mV.).

Common reference voltage can be provided by connecting the $V_{REF\ OUT}$ pin of one converter to the $V_{REF\ IN}$ pins of up to five converters (i.e. either ZN427s or ZN428s). This useful feature saves power and gives excellent gain tracking between converters. Fig. 5 shows the four ZN427s driven from one internal reference and the two ZN428s from another.

Note that in this application the dynamic characteristic of the ZN427/428 (i.e. enable/disable delay times, etc.) should not present any problems since they are much less than the microprocessor instruction execution times and need not be considered in the programming.

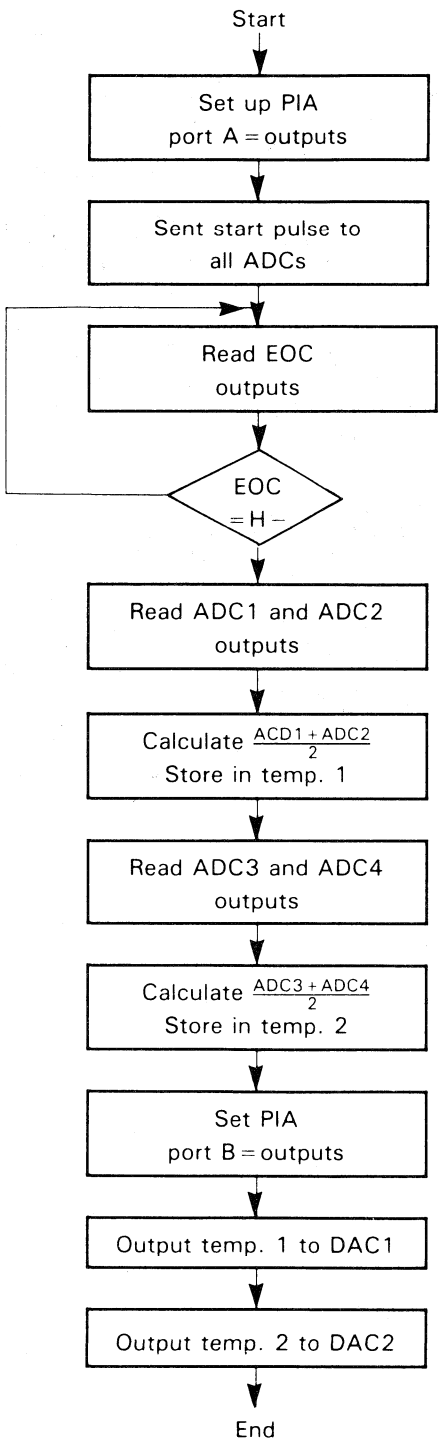
**Program example**

A simple program which illustrates the ease of controlling the ZN427/ZN428 with the PIA is shown with the flow diagram, Fig. 6. The object of the program is to read the analogue voltage inputs to ADCs 1 and 2, calculate the mean value and output this on DAC1. A similar operation is performed on the inputs of ADCs 3 and 4 and output on DAC2.

It is assumed that the PIA has been reset which has the effect of zeroing all the PIA registers. This sets all the peripheral and control lines as INPUTS and disables the interrupts. Initially the index register is loaded with the PIA base address in order that the indexed addressing mode can be used throughout the program to address the PIA. The peripheral lines PA0-PA7 are programmed as OUTPUTS and the control registers set so that control line CB2 operates in the SET/RESET output mode and the interrupt flag bit CRB-7 is set with a positive going edge on control line CB1. All the converters are disabled by outputting 30H and the PIA lines which sets the OUTPUT ENABLE inputs of the ZN427s to a logic '0' and the $\overline{\text{ENABLE}}$ inputs of the ZN428s to a logic '1'. A dummy read is made of the B data register to clear the interrupt flag bit CRB-7.

A START signal is then generated via control line CB2 by toggling bit CRB-3 in control register B. The end of the conversion cycle is detected by testing the interrupt flag bit CRB-7 and looping at this point in the program until it goes to a '1'. (Note: The microprocessor interrupt request lines IRQA, IRQB are disabled.) The output of ADC1 is now read by driving peripheral line PA0 to a logic '1', and the data is stored in the microprocessor accumulator B, ADC2 is read in a similar way by setting PA1 line to a logic '1' and storing the data in accumulator A. The mean value of the readings is found by adding the accumulators and rotating the result right, one bit through carry, this is equivalent to dividing by 2. The result is saved in the memory location labelled 'TEMP 1'. The process is repeated on ADC3 and ADC4, enabling the ADC outputs by setting lines PA2 and PA3 in turn to a logic '1', and storing the computed result in location 'TEMP 2'.

The data direction register B is now accessed and the peripheral line PB0-PB7 changed to OUTPUTS. The data stored in 'TEMP 1' is outputted onto the converter bus and DAC1 enabled by toggling line PA4 in a logic 1-0-1 sequence, which will transfer the binary data from the bus to the DAC input latches and hence to the analogue output. A similar sequence is performed on DAC2 with the data from 'TEMP 2', using PA5 line to drive the $\overline{\text{ENABLE}}$ input. The program is terminated with a software interrupt SWI, returning to the monitor program.




## PIA PORT ALLOCATIONS

### PORT A

| | |
|---|---|
| PA0 | ADC1 OE input |
| PA1 | ADC2 OE input |
| PA2 | ADC3 OE input |
| PA3 | ADC4 OE input |
| PA4 | DAC1 $\overline{EN}$ input |
| PA5 | DAC2 $\overline{EN}$ input |
| PA6 | NOT USED |
| PA7 | NOT USED |

### PORT B

| | |
|---|---|
| PB0 | BINARY DATA LSB |
| PB1 | BINARY DATA LSB + 1 |
| PB2 | BINARY DATA LSB + 2 |
| PB3 | BINARY DATA LSB + 3 |
| PB4 | BINARY DATA LSB + 4 |
| PB5 | BINARY DATA LSB + 5 |
| PB6 | BINARY DATA LSB + 6 |
| PB7 | BINARY DATA MSB |

### CONTROL

| | |
|---|---|
| CA1 | NOT USED |
| CA2 | NOT USED |
| CB1 | COMMON EOC OUTPUT |
| CB2 | COMMON START LINE |

### PIA ADDRESSES

| | |
|---|---|
| 8004 | PERIPHERAL/DATA DIRECTION REG. A |
| 8005 | CONTROL REG. A |
| 8006 | PERIPHERAL/DATA DIRECTION REG. B |
| 8007 | CONTROL REG. B |

**Fig. 6 Program flow diagram**

## 6800/6820 I/O INTERFACE - PROGRAM EXAMPLE

| Location | Object | | Comment | Source statement |
|---|---|---|---|---|
| 000 | CE004 | | LDX 8004 | Load PIA address to IX |
| 3 | 86FF | | LDA A FF | |
| 5 | A700 | | STA A 0, X | Set port A as outputs. |
| 7 | 863E | | LDA A 3E | |
| 9 | A701 | | STA A 1, X | Set control reg. A |
| B | A703 | | STA A 3, X | Set control reg. B |
| D | 8630 | | LDA A 30 | |
| F | A700 | | STA A 0, X | Disable converters |
| 11 | A602 | | LDA A 2, X | Dummy read to clear flag |
| 13 | 8636 | | LDA A 36 | |
| 15 | A703 | | STA A 3, X | Set CB2 low to |
| 17 | 863E | | LDA A 3E | generate start pulse |
| 19 | A703 | | STA A 3, X | Set CB2 high |
| 1B | A603 | TEST | LDA A 3, X | Read control reg. B |
| 1D | 8580 | | BIT A 80 | Test for CRB-7 high |
| 1F | 27FA | | BEQ TEST | ie End of conversion |
| 21 | 8631 | | LDA A 31 | |
| 23 | A700 | | STA A 0, X | Enable ADC1 O/Ps |
| 25 | E602 | | LDA B 2, X | Read ADC1 O/P |
| 27 | 8632 | | LDA A 32 | |
| 29 | A700 | | STA A 0, X | Enable ADC2 O/Ps |
| 2B | A602 | | LDA A 2, X | Read ADC2 O/P |
| 2D | 1B | | ABS | Add ADC1 + ADC2 readings |
| 2E | 46 | | RORA | Divide by 2 |
| 2F | 976E | | STA A Temp.1 | Save in temp.1 |
| 31 | 8634 | | LDA A 34 | |
| 33 | A700 | | STA A 0, X | Enable ADC3 O/Ps |
| 35 | E602 | | LDA B 2, X | Read ADC3 O/P |
| 37 | 8638 | | LDA A 38 | |
| 39 | A700 | | STA A 0, X | Enable ADC4 O/Ps |
| 3B | A602 | | LDA A 2, X | Read ADC4 O/P |
| 3D | 1B | | ABA | Add ADC1 + ADC2 readings |
| 3E | 46 | | RORA | Divide by 2 |
| 3F | 976F | | STA A Temp.2 | Save y in temp.2 |
| 41 | 8630 | | LDA A 30 | |
| 43 | A700 | | STA A 0, X | Disable ADC O/Ps |
| 45 | 863A | | LDA A 3A | |
| 47 | A703 | | STA A 3, X | |
| 49 | 86FF | | LDA A FF | |
| 4B | A702 | | STA A 2, X | Set port B as output |
| 4D | 863E | | LDA A 3E | |
| 4F | A703 | | STA A 3, X | |
| 51 | 966E | | LDA A temp.1 | |
| 53 | A703 | | STA A 2, X | Put x Data on bus |
| 55 | 8620 | | LDA A 20 | |
| 57 | A700 | | STA A 0, X | Enable DAC1 I/Ps |
| 59 | C630 | | LDA B 30 | |
| 5B | E700 | | STA B 0, X | Disable DAC1 I/Ps |
| 5D | 966F | | LDA A temp.2 | |
| 5F | A702 | | STA A 2, X | Put y data on bus |
| 61 | 8610 | | LDA A 10 | |
| 63 | A700 | | STA A 0, X | Enable DAC2 I/Ps |
| 65 | E700 | | STA B 0, X | Disable DAC2 I/Ps |
| 67 | 3F | | SWI | End |
| 006E | 00 | | Temp.1 | x data |
| 006F | 00 | | Temp.2 | y data |

## Summary

The system described in this report is by no means restricted to the configuration shown. Provided that the drive capability of the system components is not exceeded, the number and configuration of ZN427s and ZN428s which can be employed is limited only by the I/O lines available from the PIA, hence providing the design engineer with a wide degree of freedom in producing the system that best fulfils his requirements.

The major loading and drive characteristics of the various system components are shown in Table 1. Buffer gates can be employed where necessary to expand the drive capability of the components such as when utilising a long bus with high capacitive loading. Note that the peripheral lines from side B are used for the converter bus since these present a high impedance when programmed as inputs. Also the 6821 PIA is preferred to the 6820 because this has a 2-TTL drive capability on both A and B side peripheral lines. As stated previously up to 4 ZN427 EOC outputs can be 'wire-or'd' together; if using more than 4, then each group can be ANDed together using a SN7409 TTL gate to produce a single interrupt line.

If required separate START signals can be generated for each ZN427 hence allowing a microprocessor read of one ADC to be in progress while the other(s) are in a conversion cycle. However this configuration does require one peripheral line and one 'D' type flip-flop per START signal line. Since only one ZN427 or ZN428 should be enabled at any one time, then it is possible to incorporate one or more decoder types of I.C. such as the SN74154, 4 line to 16 line demultiplexer/ decoder in order to expand the system. This device could be connected with the 4 data inputs connected to 4 PA peripheral lines and the decoder enable input driven by CA2 line. Use of two such I.C's would provide 32 output lines allowing an analogue I/O system with a combination of up to 32 analogue input and output channels to be produced.

As a result of the low converter cost, low external component count and flexibility of this type of system, designs based on using one converter per analogue channel will be both a practical and economical solution to microprocessor data acquisition problems. This approach should find many new applications in areas which have previously been limited by the necessity of having to use the traditional data acquisition methods involving a single, high cost hybrid A-D converter utilising a sample/hold and multichannel multiplexing techniques.

**TABLE 1**

| MC6820 | PA0 - PA7/CA2 | PB0 - PB7/CB2 | CA1/CB1 |
|---|---|---|---|
| $I_{IL}$ | −1.6mA max. | 10μA max. | 2.5μA max. (at $V_{IN}$ = 0 to 5.25V) |
| $I_{IH}$ | −100μA min. | | |
| $I_{OL}$ | 1.6mA min | 1.6mA min | |
| $I_{OH}$ | −100μA min | −100μA min. | |
| MC6821 | | | |
| $I_{IL}$ | −2.4mA max | 10μA max | 2.5μA max. (at $V_{IN}$ = 0.5... 5.25V) |
| $I_{IH}$ | −200μA min | | |
| $I_{OL}$ | 3.2mA min | 3.2mA min | |
| $I_{OH}$ | −200μA min | −200μA min | |
| ZN427 | | | |
| $I_{IL}$ | −5μA max | | |
| $I_{IH}$ | 15μA max | | |
| $I_{IH\ (Clock)}$ | 30μA max | | |
| $I_{OL}$ | 1.6mA min | | |
| $I_{OH}$ | −100μA min | | |
| $I_{OHX}$ (Off state leakage) | 2μA max | | |
| ZN428 | All inputs | | |
| $I_{IL}$ | −5μA max | | |
| $I_{IH}$ | 20μA max | | |

**NOTE** Currents specified at 0.4 and 2.4V unless otherwise stated.

# Interfacing the ZN427 A-D Converter with the 8085A

**The growth of microprocessors has led to a demand for low cost, fast 8-bit A-D and D-A converters to interface between the real world of analogue values and the digital world of the microprocessor. Converter systems have, until recently, been mainly high cost, multiplexed, sample and hold systems usually built around a 12-bit A-D converter. The system described in this report is a low cost, expandable, one converter per channel system, based on the ZN427 8-bit A-D converter interfaced directly to the I/O Ports of the 8155 2K bit static 'RAM', which forms part of the basic 8085A microprocessor system.**

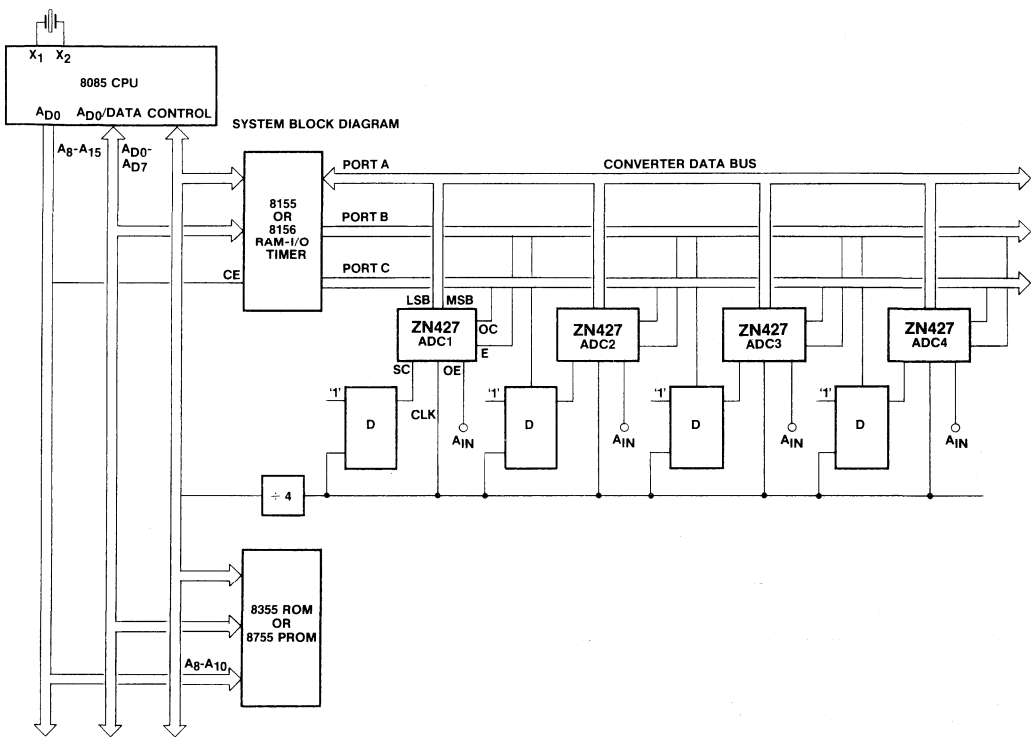



Fig. 1 System block diagram

### The ZN427 A-D converter

The ZN427 is a monolithic 8-bit, successive approximation A-D converter designed for microprocessor compatibility. It features fast 15$\mu$s conversion time, three-state outputs to permit bussing on common data lines and no missing codes over the full operating temperature range. The ZN427 contains a voltage switching D-A converter, a 2.5V precision band gap reference, a fast comparator, successive approximation logic, and three-state output buffers.

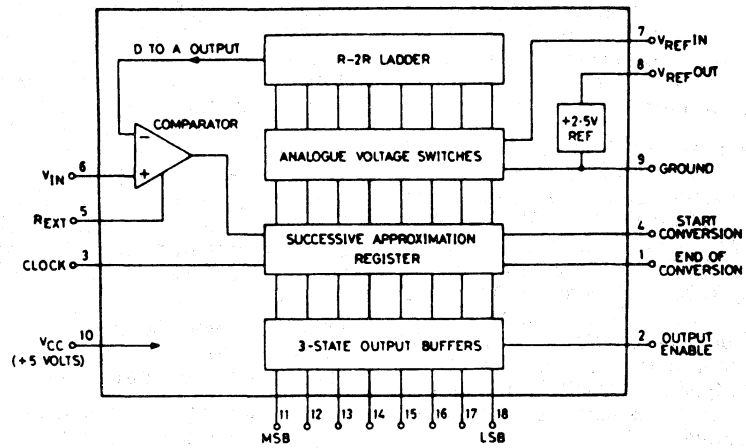



Fig. 2 ZN427 logic diagram

Operation of the ZN427 is best described with reference to the timing diagram - Fig. 3. Conversion is initiated by a start convert (SC) pulse which can be applied asynchronously with respect to the ZN427 clock providing the following criteria are met.

1. The leading edge of the SC-pulse should precede the first active (negative going) edge of the clock (after trailing edge of the SC pulse) by at least 1.5$\mu$s to allow for MSB setting.

2. The trailing edge of the SC pulse must not occur within $\pm$ 200ns of a negative going edge of the clock.

3. As a special case of conditions (1) and (2) the SC pulse may be coincident with, and of the same duration as, a negative going clock pulse. Application of the SC pulse sets MSB to a '1' level and all other bits to a '0', which produces a voltage output from the D to A converter of $V_{REFIN/2}$. This value is compared with the input voltage $V_{IN}$, and a decision is made on the first negative clock edge to set the MSB to '0' if $V_{REFIN/2} > V_{IN}$, or else to keep it at '1'. Bit 2 is switched to a '1' on the same clock edge, and on the next edge a decision is made about bit 2, again by comparing the D/A output with $V_{IN}$. This process is repeated for all eight bits so that when the END OF CONVERSION (EOC) output goes high the digital output from the converter is valid representation of $V_{IN}$. The binary output is latched until the next START pulse. The three-state data outputs are OFF (high impedance) when OUTPUT ENABLE (OE) is a '0' and are enabled when the OE input is taken to a '1'.

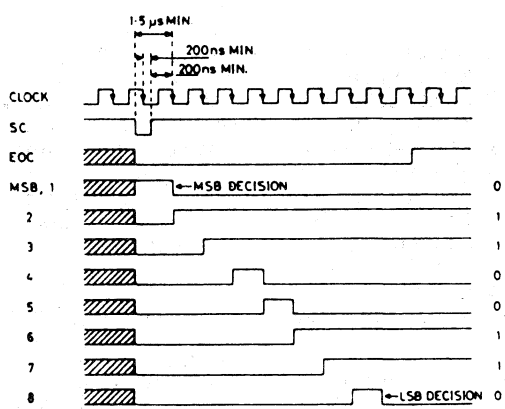



Fig. 3 Timing diagram

### The 8085A microprocessor system

It is assumed that the reader is totally familiar with the 8085A microprocessor system, information on which can be obtained from the MCS-85 users manual, so only a brief description is given here.

The 8085A is a complete 8-bit parallel central processing unit. A minimum component 8085 microcomputer system can be built from just three chips - the 8085A CPU, a 8355 or 8755 ROM or PROM, and a 8155 or 8156 RAM/TIMER/I-O chip. The 8155/8156 provides, in addition to 2k bits of Static RAM, two programmable 8-bit I/O Ports, one programmable 6-bit I/O Port and a programmable 14-bit binary timer counter. (The difference between the 8155 and the 8156 is that on the 8155 the CHIP ENABLE is active LOW, and on the 8156 it is active HIGH).

### The ZN427 interface

This application note describes how up to 4, ZN427 ADCs can be connected to the I/O ports of one 8155 RAM to provide 4 analogue input channels to the microprocessor system. Since most 8055 based systems include the SDK-85 system design kit will incorporate one or more 8155s, then the addition of analogue input channels would involve minimum additional hardware and design effort. An advantage of using the 8155 I/O ports is that no additional address decoding or bus demultiplexing and buffering hardware is necessary.

For existing systems, if spare I/O ports are available then analogue inputs can easily be added without any major modifications to the hardware. Also the expansion of the number of input channels to a system by addition of extra 8155s should be easily implemented since this device is directly bus compatible with the 8085A.

The 8155 I/O ports are allocated as shown in the logic diagram, Fig. 1. Port A is programmed as INPUTS and provides an 8-bit data bus which connects to the three-state binary data outputs of each ZN427. port B is programmed as OUTPUTS, the lower 4-bits provide the start convert and the upper 4-bits provide the output enable signals to each ZN427. The END OF CONVERT output of each ZN427 is connected to a port C pin, which are programmed as INPUTS to provide the individual BUSY FLAGS for each ZN427. Note that only 4- of the 6-bits available from port C are used.

The ZN427 clock can be supplied either from an external source or from the 8085A CLOCK OUTPUT. Since the 8085A clock will normally be at 3MHz, it will be necessary to divide this down by at least a factor of 4. This is achieved in the circuit, see Fig. 6, by means of a dual JK flip-flop (7473) connected as a 2-bit binary counter. (Note: This will provide a clock frequency of 750kHz which is a little higher than the ZN427 clock frequency spec. minimum of 600kHz. However, for most practical applications the loss in accuracy due to this will be minimal.) An external clock could be used for the ZN427 but the advantage of using the microprocessor clock is that it allows an accurate calculation of the ZN427 conversion time to be made in terms of the microprocessor CLOCK CYCLES (or 'T' states).

(Note: To avoid confusion, future reference to clock will mean the ZN427 clock signal unless specifically stated otherwise.)

The START CONVERT pulse is generated using a 'D' type flip-flop (½ 7474) in order to meet the timing requirements discussed earlier. A conversion cycle is started by outputting a '0' followed by a '1' from the appropriate port B output to the CLEAR input of the 'D' type which sets the SC input of the ZN427 to '0'. The first positive going clock edge after the CLEAR input is returned to a '1' clocks the 'D' type and sets the SC input to '1'. This sequence is illustrated in the start pulse timing diagram, Fig. 4.

On the 9th negative clock edge after the start pulse the END OF CONVERT output goes to a '1' signifying the end of the conversion process, this can be detected by an I/O read on port C. However, when generating the ZN427 clock from the microprocessor clock as shown, the EOC output will always occur within 35 microprocessor clock cycles after the OUT instruction returning the SC to a '1'. In this case it is not necessary to poll the EOC outputs, the ZN427 data outputs can be read after a suitable fixed delay in the program. For application where process time is at a premium or if immediate response is required to an EOC output, a microprocessor interrupt can be generated by connecting the EOC output direct to one of the 8085A restart inputs. The EOC outputs of two 4-ZN427s can be 'wire-OR'd' to produce a common interrupt line. Usually, however, the fast conversion time of the ZN427 (15$\mu$s) will make it not worth-while to employ microprocessor interrupts since the conversion time takes less than 6/7 typical microprocessor instructions.

The binary output data is applied via the converter data bus to port A of the 8155 by driving the OE output to a '1' from the appropriate port B bit. Obviously the program should be arranged so that the outputs of only one ZN427 are enabled at any one time, in order to avoid bus contention problems. Note that in this application the output enable and disable switching times (which are specified at 250ns

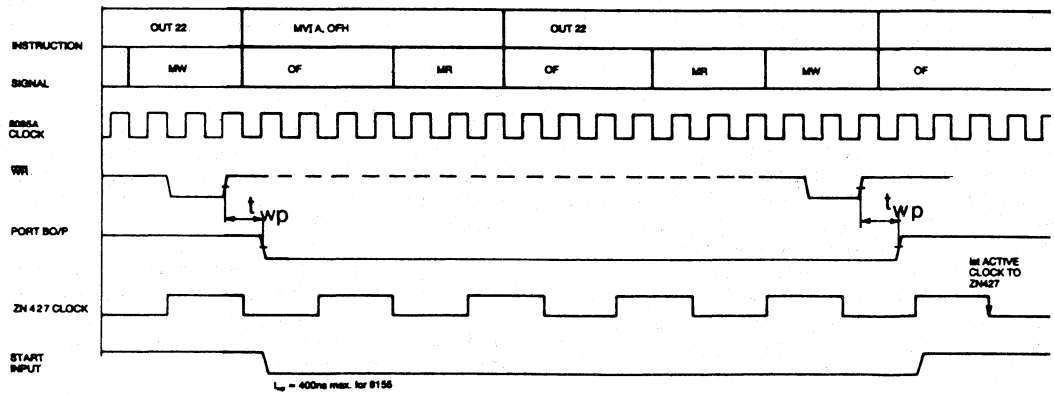



**Fig.4 Start pulse timing diagram**

max.), need not be considered since they are much less than the instruction execution times.

The circuit diagram, Fig. 6 shows the ZN427s connected for a unipolar input range of 0 to +10V. Other ranges, e.g. +5V, ±10V, and ±5V can be readily obtained by using the appropriate resistors as shown in the ZN427 data sheet. Note also that the reference, $V_{REF\ IN}$, of up to five ZN427s may be driven from one internal reference. This useful feature saves power, discrete components, and gives excellent gain tracking between the converters.

In the circuit the negative supply to the ZN427s is through an 82k resistor from −5V. By suitable choice of resistor any negative supply of −3 to −30 volts may be used. For applications where only a positive 5 volt supply is available, a simple diode pump circuit suitable for up to 5-ZN427s is shown in the ZN427 data sheet.

**Program example**

A simple program is given together with the flow diagram in Fig. 5, which illustrates the ease of controlling and reading the ZN427 with the 8155 I/O ports.

Following the flow diagram it is seen that after initialisation of the stack pointer the I/O ports of the 8155 are defined - ports A and C as INPUTS, port B as OUTPUTS. A simultaneous START CONVERT pulse is sent to all the ADCs by outputting logic '0' followed by logic '1' to the lower 4-bits of port B. The EOC outputs of the ADCs are then read via port C and tested for a logic '1' to check if the conversion process has finished. The microprocessor will loop on this part of the program until the EOC output of all the ADCs go to '1'. When this occurs the program proceeds by enabling the outputs of each ADC in turn and reading the binary data via port A. The ADC outputs are enabled in turn by outputting a logic '1' to each of the upper 4-bits of port B (keeping the other 3-bits at '0' and the lower 4-bits at a '1'). The data from each ADC is stored in consecutive memory locations, starting at the address labelled 'DATA'. The H and L register pair hold the memory address at which data is to be saved; these are incremented for each read of the ADC.

This program could easily be modified to act as a sub-routine for another main program. As mentioned previously a fixed delay could be substituted for the program loop which tests the EOC outputs. Also instead of generating a simultaneous START pulse separate START signals may be sent to each ADC at different times in a control cycle.

**Summary**

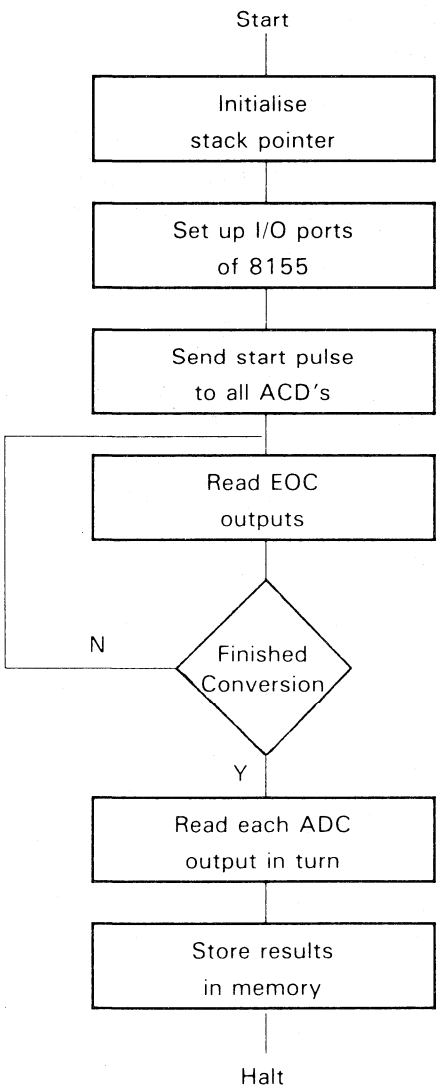
The system described in this report should be suitable for most applications since it allows complete control of each individual ADC. However, the configuration can easily by changed for particular requirements, - a few ideas are briefly described below.

1. If a simultaneous START pulse is adequate, then the START CONVERT inputs of the ZN427s can be commoned together and driven via one 'D' type from one port output.
2. The EOC outputs of up to 4-ZN427s can be commoned and either taken to one port input or used as a microprocessor interrupt signal.
3. Adoption of methods 1 and/or 2 above would use 8155 Port bits and hence allow more ZN427s to be connected to each 8155.
4. Instead of generating the START pulse from the 8155 it could be asynchronously produced externally by a process timer, photo transistor or proximity detector circuit etc., the only timing requirement being that the pulse width fed to the CLEAR input of the 'D' type is at least half a clock period. (i.e. 640ns with a 320ns microprocessor clock) or 1.5$\mu$s, whichever is smaller.
5. If D-A channels as well as A-D are required in one system then ZN428, 8-bit D-A converters can be mixed on the same converter data bus as the ZN427. This will allow a designer to tailor a system to his specific A-D and D-A requirements.

It is hoped that after reading this application note, the reader will have a much better insight into the operation and versatility of the ZN427, and into how it can easily be interfaced to a microprocessor system.

In order to avoid duplication only the relevant ZN427 characteristics were discussed in this report. For a full description and specification of the ZN427 please refer to the data sheet.

**Fig.5 Program flow diagram**




**8155 PORT ALLOCATIONS**

**PORT A**

| | |
|---|---|
| PA0 | BINARY DATA LSB |
| PA1 | BINARY DATA LSB + 1 |
| PA6 | BINARY DATA MSB – 1 |
| PA7 | BINARY DATA MSB |

**PORT B**

| | |
|---|---|
| PB0 | ADC1 SC INPUT |
| PB1 | ADC2 SC INPUT |
| PB2 | ADC3 SC INPUT |
| PB3 | ADC4 SC INPUT |
| PB4 | ADC1 OE INPUT |
| PB5 | ADC2 OE INPUT |
| PB6 | ADC3 OE INPUT |
| PB7 | ADC4 OE INPUT |

**PORT C**

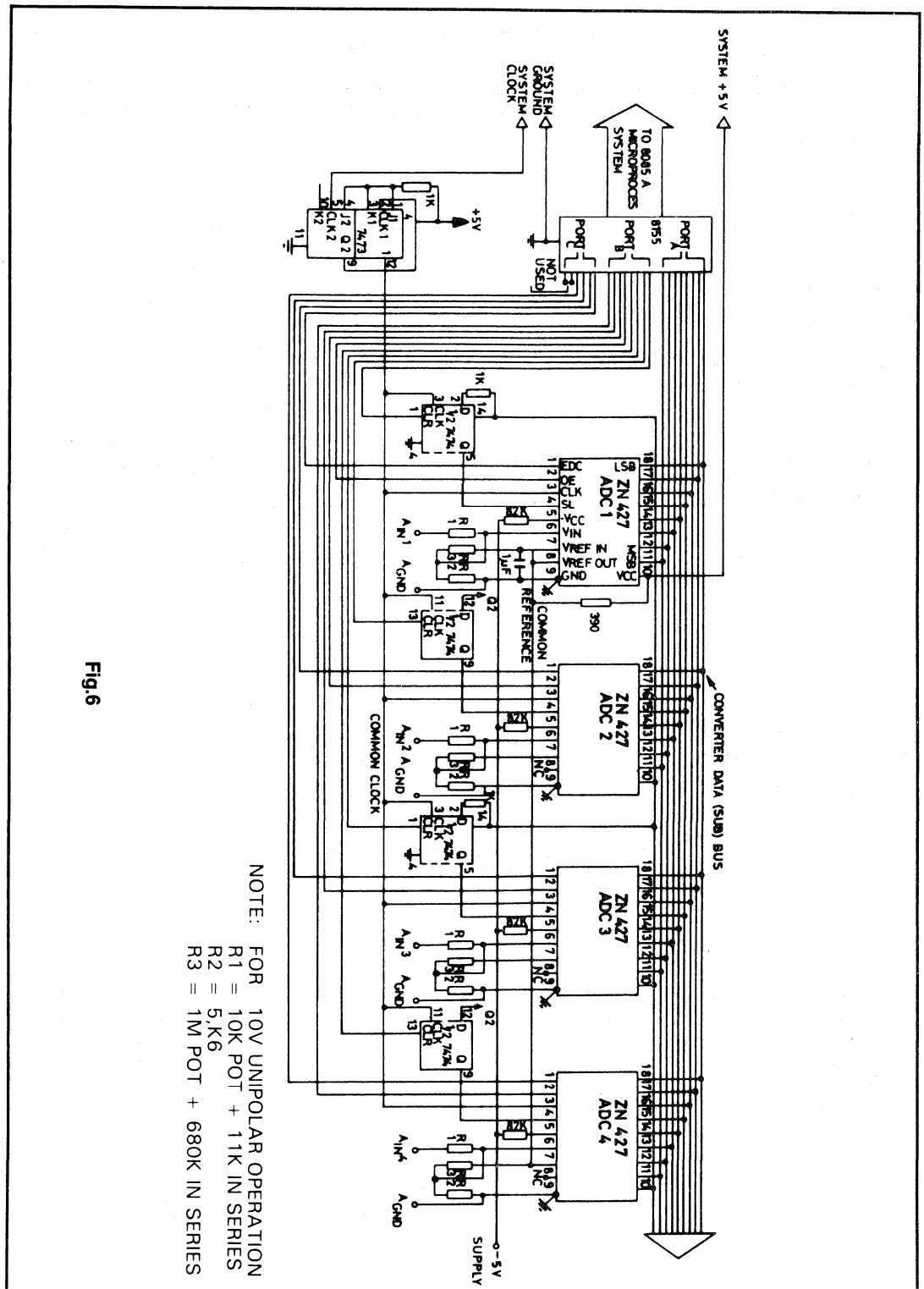
| | |
|---|---|
| PC0 | ADC1 EOC OUTPUT |
| PC1 | ADC2 EOC OUTPUT |
| PC2 | ADC3 EOC OUTPUT |
| PC3 | ADC4 EOC OUTPUT |

**I/P PORT ADDRESSES**

| | |
|---|---|
| 20 | COMMAND/STATUS REG |
| 21 | RAM PORT A |
| 22 | RAM PORT B |
| 23 | RAM PORT C |

## ZN427 - 8085A PROGRAM EXAMPLE

| Location | Object | | Source statement | Comment |
|---|---|---|---|---|
| 2000 | 31C820 | | LXI SP, 20C8 | Initialise stack pointer |
| 2003 | 3E02 | | MVI A, 02H | Define I/O ports |
| 2005 | D320 | | OUT 20 | |
| 2007 | 3E00 | | MVI A, 00H | |
| 2009 | D322 | | OUT 22 | Send start to ALL ADC's |
| 200B | 3EOF | | MVI A, OFH | |
| 200D | D322 | | OUT 22 | |
| 200F | 060F | | MVI B OFH | |
| 2011 | DB23 | LOOP: | IN 23 | Read EOC s |
| 2013 | AO | | ANA B | Strip upper 4 bits |
| 2014 | B8 | | CMP B | Test if ALL EOC s |
| 2015 | C21720 | | JNZ LOOP | are A '1' |
| 2018 | 213B20 | | LXI H, DATA | |
| 201B | 3EIF | | MVI A, 1FH | |
| 201D | D322 | | OUT 22 | Enable ADC 1 |
| 201F | DB21 | | IN21 | Read ADC 1 |
| 2021 | 77 | | MOV M, A | Save in Loc., DATA |
| 2022 | 23 | | INX H | Increment pointer |
| 2023 | 3E2F | | MVI A 2FH | |
| 2025 | D322 | | OUT 22 | |
| 2027 | DB21 | | IN21 | Read ADC 2 |
| 2029 | 77 | | MOV M, A | Save in Loc. DATA + 1 |
| 202A | 23 | | INX H | |
| 202B | 3E4F | | MVI A 4FH | |
| 202D | D322 | | OUT 22 | |
| 202F | DB21 | | IN 21 | Read ADC 3 |
| 2031 | 77 | | MOV M,A | Save in Loc. DATA + 2 |
| 2032 | 23 | | INX H | |
| 2033 | 3E8F | | MVI A 8 FH | |
| 2035 | D322 | | OUT 22 | |
| 2037 | DB 21 | | IN 21 | Read ADC 4 |
| 2039 | 77 | | MOV M, A | Save in Loc. DATA + 4 |
| 203A | 76 | | HLT | |
| 203B | | DATA: | | |
| 203C | | | | |
| 203D | | | | |
| 203E | | | | |




NOTE: FOR 10V UNIPOLAR OPERATION
R1 = 10K POT + 11K IN SERIES
R2 = 5,K6
R3 = 1M POT + 680K IN SERIES

**Fig.6**

# Interfacing the ZN428 D-A Converter with the 8085A

**This report describes a simple, low cost, expandable multichannel D-A system based on the ZN428, 8-bit D-A converter interfaced directly to the I/O ports of the 8155, 2K bit static RAM, which forms part of the basic 8085 microprocessor system.**

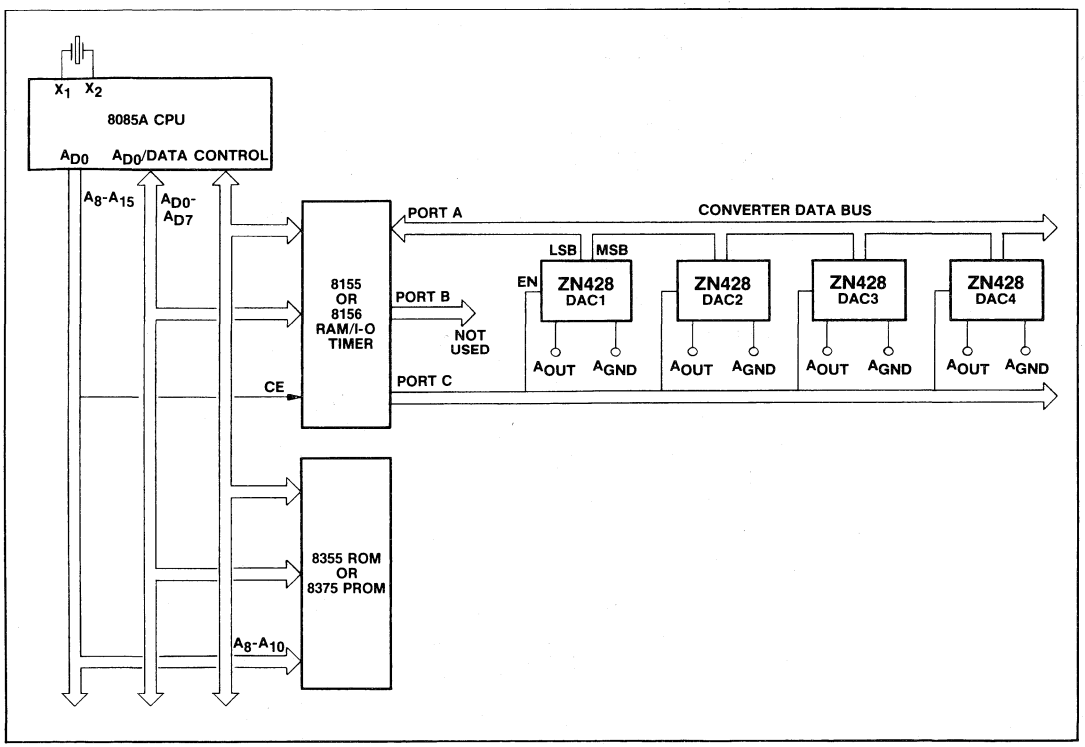



Fig. 1 System block diagram

### The ZN428 D-A converter

The ZN428 is a monolithic 8-bit D-A converter with input latches to facilitate updating from a data bus. The latch is transparent when ENABLE is at logic '0' and the data is held when ENABLE is taken to logic '1'. The ZN428 features single + 5 volt supply requirements, fast 800ns setting time and is guaranteed monotonic over the full operating range. It also contains a 2.5 volt reference the use of which is pin optional to retain flexibility. An external fixed or varying reference may therefore be substituted.

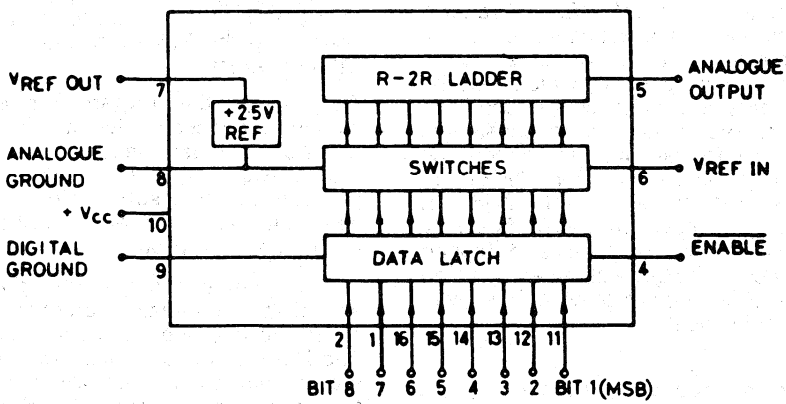



Fig. 2 ZN428 logic diagram

The converter is of the voltage switching type and used R-2R ladder network. Each 2R element is connected to the 0 volt or $V_{REF\ IN}$ by transistor voltage switches specially designed for low offset voltage (1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network the nominal output range of the ZN428 being 0 volt to $V_{REF\ IN}$ through a 4kΩ resistance. Other output ranges can readily be obtained by using an external amplifier.

### The 8085A microprocessor system

It is assumed that the reader is totally familiar with the 8085A microprocessor system, information on which can be obtained from the MCS-85 users manual, so only a brief description is given here.

The 8085A is a complete 8-bit parallel central processing unit. A minimum component 8085A microcomputer system can be built from just three I.C.s-the 8085A CPU, an 8355 or 8755 ROM or PROM, and a 8155 or 8156 RAM/TIMER/I-O I.C. The 8155/8156 in addition to 2K Bits of Static RAM, provides two programmable 8-bit I/O ports, one programmable 6-bit I/O port and a programmable 14-bit binary timer counter. (The difference between the 8155 and the 8156 is that on the 8155 the CHIP ENABLE is active LOW, and on the 8156 it is active HIGH.)

### The ZN428 interface

This application note describes how one or more ZN428 DACs can be connected directly to the I/O ports of an 8155 RAM to provide analogue output channels from the microprocessor system.

Since most 8085 based systems, including the SDK-85 system design kit, will incorporate one or more 8155s then the addition of analogue output channels can be made with the minimum of extra hardware and design effort. An advantage of using the 8155 I/O ports is that no additional address decoding or bus multiplexing and buffering hardware is necessary. For existing systems, if spare I/O ports are available then analogue outputs can easily be added without major modifications to the hardware. Also expanding the number of output channels by means of addition of extra 8155s should be easy to implement, since the 8155 is directly bus compatible with the 8085A. Fig. 3 shows 4-ZN428s connected to the I/O ports of one 8155. Port A is programmed as OUTPUTS and provides a common 8-bit data bus which is connected to the binary data inputs of each ZN428. The ENABLE inputs of each of the ZN428s are connected to separate pins on port C which is also programmed as OUTPUTS. Note that in this configuration only 4 of the 6 port C pins are used and port B is also unused.

The reference voltage of all converters, is provided by connecting the $V_{REF\ OUT}$ pin of one ZN428 to the $V_{REF\ IN}$ pins of all the ZN428s as shown. This useful feature saves power, components and gives excellent gain tracking between converters. Up to five ZN428s may be driven from one internal reference in this way.

The circuit, Fig. 3, shows the outputs of the ZN428s taken directly from pins 5 and 8. This will provide an output range of 0V to $V_{REF\,IN}$ through a 4kΩ output resistance. A small capacitor can be connected across the output pins as shown in order to remove any 'glitches' which may be present. The value of this capacitor depends on the noise in the system and the response time required, however, for the minimum settling time it should not be greater than 100pF. The output buffer amplifier was omitted from the ZN428 in order to allow greater system speed, flexibility and lowest cost. Both unipolar and bipolar output ranges can readily be obtained by using an external amplifier, details of which are given in the ZN428 data sheet.

The ZN428 is provided with separate analogue and digital ground pins. These can be connected together close to the I.C. pins. However, for noisy systems or environments it may be better to keep the analogue ground pins for each individual ZN428 separate from the digital ground, and to connect each analogue ground to a single common earth point in the system, away from sources of digital noise such as clock oscillators, digital buses etc. The analogue ground output line or terminals should also be taken direct to this common earth point. (Note: The maximum voltage between analogue and digital grounds is limited to 200mV.)

Data is fed to a converter simply by outputting the binary data onto the common bus from port A of the 8155. The appropriate output from port C is then driven to a logic '0' level then back to a logic '1'. This will transfer the binary data on the bus into the input latches of the ZN428. The $\overline{\text{ENABLE}}$ inputs of converters which are not being updated are held at logic '1'. The data from port A can now be changed and the next converter updated as and when required as determined by the controlling program of the microprocessor. Note that in this application the data set-up and data hold times and enable pulse widths need not be considered since they are much less than the microprocessor instruction execution times.

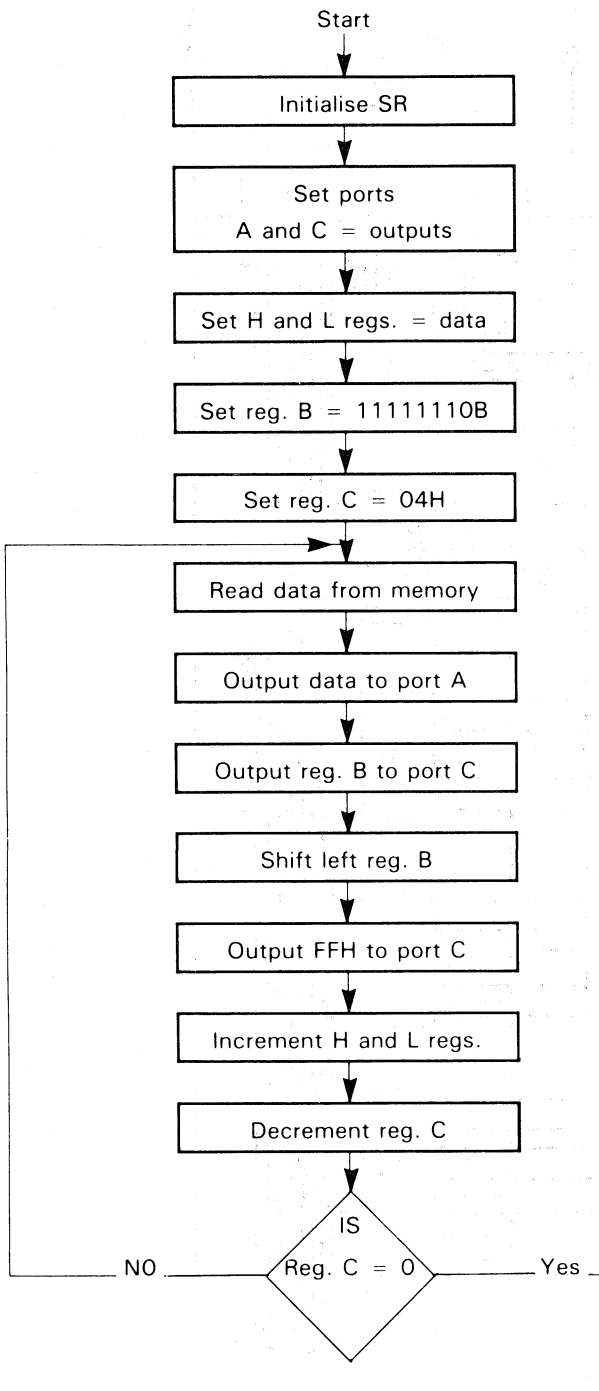
**Program example**

A simple program is given together with the flow diagram in Fig. 4, which illustrates the ease of controlling the ZN428 in conjunction with the 8155 I/O ports.

The object of the program is to read the binary data from four successive memory locations and to output this data sequentially to each of the four DACs. In practice this program would probably act as a sub-routine outputting data derived from some external source and operated on by the main program.

With reference to the flow diagram Fig. 4 it is seen that after initialisation of the stack pointer the I/O ports A and C are defined as OUTPUTS. The H and L register pair are loaded with the starting address in memory of where the data to be outputted is stored. Register B determines which ADC is to be enabled, this is set initially to 11 111 110; while register C, which acts as a loop counter is set to 4. Data is then read from memory into the accumulator using the H and L registers in the register indirect addressing mode. This data is outputted onto the converter data bus via port A by sending the contents of the accumulator directly to the 8155 with the 'OUT' instruction. DAC 1 is now enabled by transferring the contents of register B to the accumulator and outputting this via port C. The accumulator contents are rotated one bit left before being transferred back to register B, ready to enable the next DAC. Next $\overline{\text{ENABLE}}$ is removed by outputting all 1's via port C, H and L are incremented to address the next data byte and register C is decremented and tested for zero. In this case register C will contain 03 and the program will branch back to the address labelled 'LOOP' via a conditional jump instruction, and the data byte will be read into the accumulator. Since register B was shifted one bit left the new data will be loaded into DAC 2 on this cycle of the loop. The program cycles round the loop 4 times, reading the data from memory and outputting it to each DAC in turn until register C is decremented to zero, at which point the program halts.

Fig. 4 Program flow diagram




**8155 PORT ALLOCATIONS**

**PORT A**

| | |
|---|---|
| PA0 | BINARY DATA LSB |
| PA1 | BINARY DATA LSB + 1 |
| PA6 | BINARY DATA MSB – 1 |
| PA7 | BINARY DATA MSB |

**PORT B**

NOT USED

**PORT C**

| | |
|---|---|
| PC0 | DAC1 $\overline{\text{ENABLE}}$ INPUT |
| PC1 | DAC2 $\overline{\text{ENABLE}}$ INPUT |
| PC2 | DAC3 $\overline{\text{ENABLE}}$ INPUT |
| PC3 | DAC4 $\overline{\text{ENABLE}}$ INPUT |
| PC4 | NOT USED |
| PC5 | NOT USED |

**I/O PORT ADDRESSES**

| | |
|---|---|
| 20 | COMMAND/STATUS REG |
| 21 | RAM PORT A |
| 22 | RAM PORT B |
| 23 | RAM PORT C |

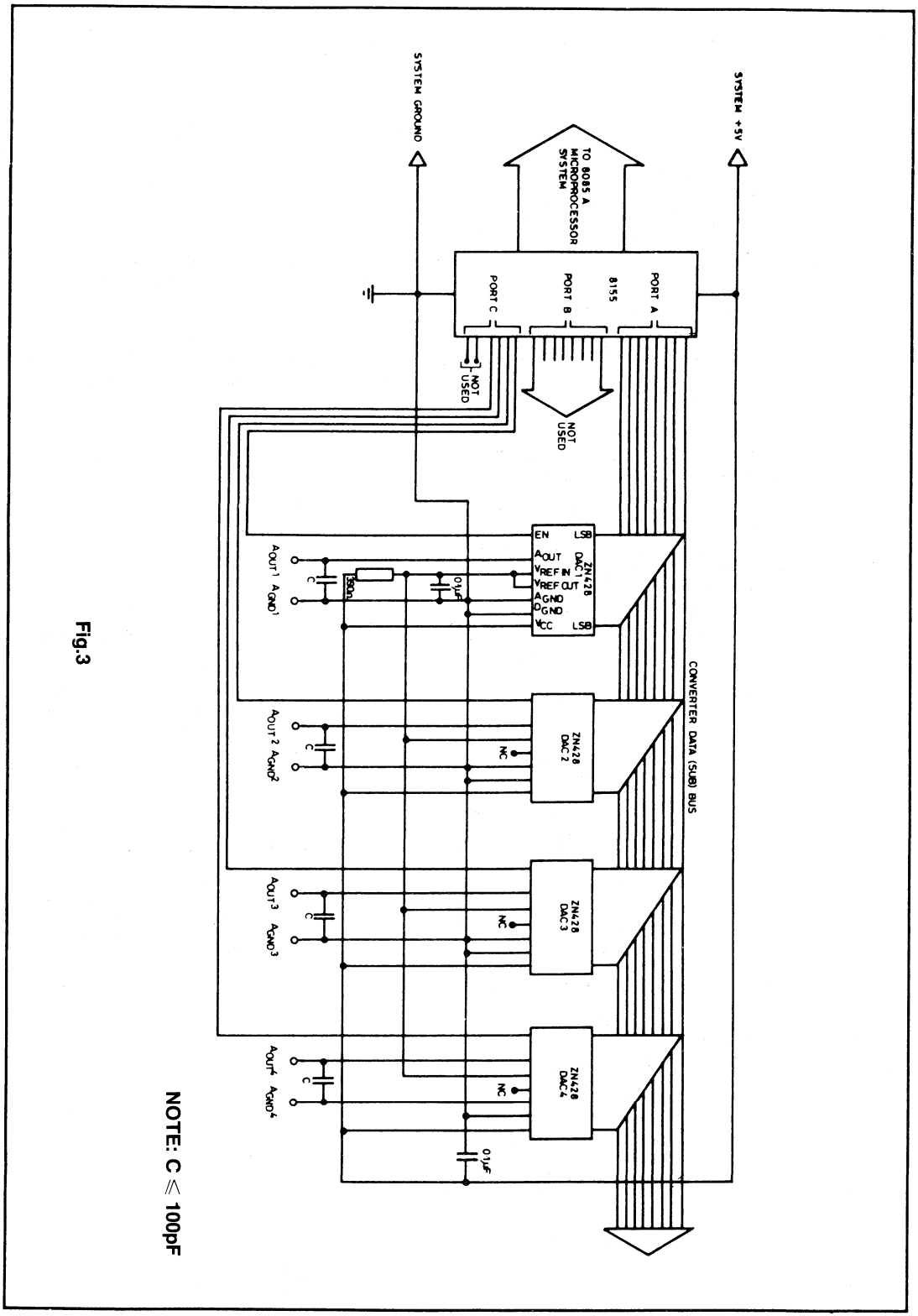



Fig.3

NOTE: C ⩽ 100pF

**Summary**

The system described in this report should be satisfactory for most applications, however, this configuration is by no means rigid, but is only intended as one example to demonstrate how easily the ZN428 can be used with the 8085A microprocessor system. A few ideas and notes are briefly described below, and it is hoped that these will help the design engineer to produce the most efficient system for his particular requirements.

1. The 8155 I/O ports can be allocated as dictated by system requirements and availability. In the example all of port A and four of the six port C I/O pins are used. Port B could have been used equally as well either for the converter data bus or to provide the $\overline{\text{ENABLE}}$ signals.

2. If I/O port pins are limited and only one DAC needs to be enabled at any one time, then a decoder I.C. (i.e. 8205, 1 out of 8 binary decoder) can be used to drive the $\overline{\text{ENABLE}}$ inputs. For example 4 I/O port pins, 3 for the address code and 1 for the decoder enable would drive 8 DAC ENABLE inputs.

3. In order to update 2 DACs simultaneously but with different data, then the binary inputs of one (or more) DACs could be connected to port A and the other DAC to port B. The relevant data could then be output on Ports A and B and then the ENABLE inputs of both DACs driven to logic '0' together, either by commoning the two inputs to one port C or by using separate I/O pins from port C but programming both bits to go low together.

4. The number of ZN428s which can be connected to a common data bus is limited only by the bus capacitance and the drive capability of the 8155 I/O Ports. Note the low inputs currents of the ZN428 –
$I_{IH} = 20\mu A$ at 2.4V, $I_{IL} = -5\mu A$ at 400mV.

5. When the ZN428 $\overline{\text{ENABLE}}$ input is held at logic '0' the input latches are held open and the data is transferred directly to the ladder switches. Therefore, if repeatedly updating only one DAC the $\overline{\text{ENABLE}}$ input can be held at logic '0' instead of returning to logic '1' after each update.

6. If A-D channels as well as D-A are required in one system, then ZN427, 8-bit A-D converters can be mixed on the same converter data bus as the ZN428. This will allow the design engineer to tailor a system to his specific A-D and D-A requirements.

It is hoped that after reading this application note the reader will have a much better insight into the operation and versatility of the ZN428, and into how it can easily be interfaced to a microprocessor system. In order to avoid duplication only the relevant characteristics of the ZN428 were discussed in this report. For a full description and specification of the ZN428 please refer to the data sheet.

## ZN428 - 8085A PROGRAM EXAMPLE

| Location | Object | | Source statement | Comment |
|---|---|---|---|---|
| 2000 | 31C8204 | | LXI SP. 20C8 | Initialise SP |
| 2003 | 3E0D | | MVIA, 0D | Define I/O ports |
| 2005 | D320 | | OUT 20 | |
| 2007 | 212020 | | LXI H, DATA | Set H & L = data |
| 200 A | 06FE | | MVI B, FEH | |
| 200 C | 0E0 4 | | MVI C, 04H | |
| 200 E | 7E | LOOP: | MOV A,M | Read data |
| 200 F | D321 | | OUT 21 | Put Data on bus |
| 2011 | 78 | | MOV A,B | |
| 2012 | D323 | | OUT 23 | Set $\overline{\text{Enable}}$ low |
| 2014 | 07 | | RLC | Rotate left for next DAC |
| 2015 | 47 | | MOV B,A | |
| 2016 | 3EFF | | MVI A, FF | Set $\overline{\text{Enable}}$ high |
| 2018 | D323 | | OUT 23 | |
| 201A | 23 | | INX H | |
| 201B | 0D | | DCR C | |
| 201C | C2 0E 20 | | JNZ Loop | Jump IF C = 0 |
| 201F | 76 | | HLT | |
| | | | | |
| 2020 | – | | DATA: | |
| 2021 | | | | |
| 2022 | | | | |
| 2023 | | | | |

# Direct Bus Interfacing using the ZN427/ZN428 Data Converters

**This application note introduces two converters and describes how they can easily be interfaced directly to most of the popular types of microprocessor with particular reference to the 6800 and 8085A.**

## The ZN427 A-D converter

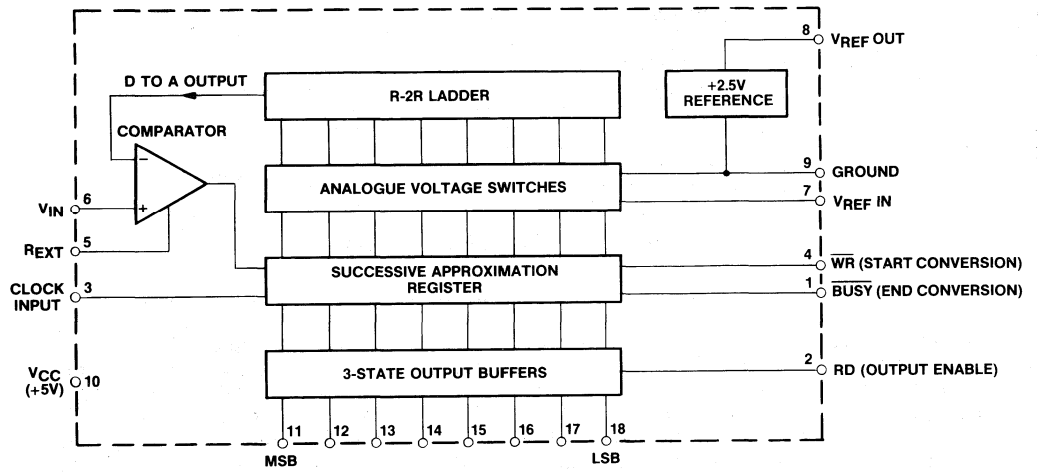



Fig. 1 ZN427 logic diagram

The ZN427 is an 8-bit, successive approximation A-D converter (ADC).

It features three-state output buffers to permit bussing on to common data lines, fast 15$\mu$s conversion time and no missing codes over its full operating temperature range. The ZN427 contains a voltage switching D-A converter, a fast comparator, successive approximation logic, three-state output buffers and a 2.5 volt precision bandgap reference.

The use of the on-chip reference is pin optional to retain flexibility, an external fixed or varying reference for ratiometric operation may, therefore, be substituted. Only a few passive external components are required. For basic operation these are an input resistor, a reference current resistor and stabilising capacitor, and a resistor from the $R_{EXT}$ pin 5 to the negative supply rail.

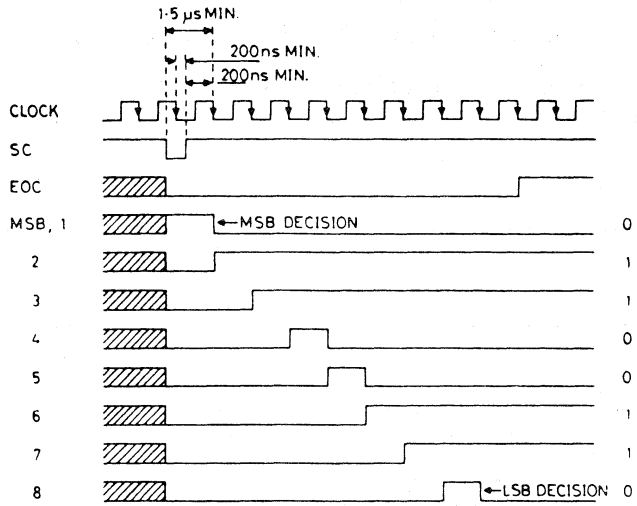



Fig. 2 ZN427 timing diagram

The conversion cycle is initiated by a negative going pulse applied to the START CONVERSION (SC) input, this sets the END OF CONVERSION (EOC) output to a logic '0' indicating that the converter is busy, see Fig. 2. On the ninth negative going clock edge after the start pulse the EOC output goes back to logic '1' signalling that the cycle is complete. The binary output data is latched until the next start pulse. The three-state data outputs are switched OFF (high impedance state) when the OUTPUT ENABLE (OE) input is at a logic '0', and they are enabled when the OE input is taken to a logic '1'.

**The ZN427 D-A converter**

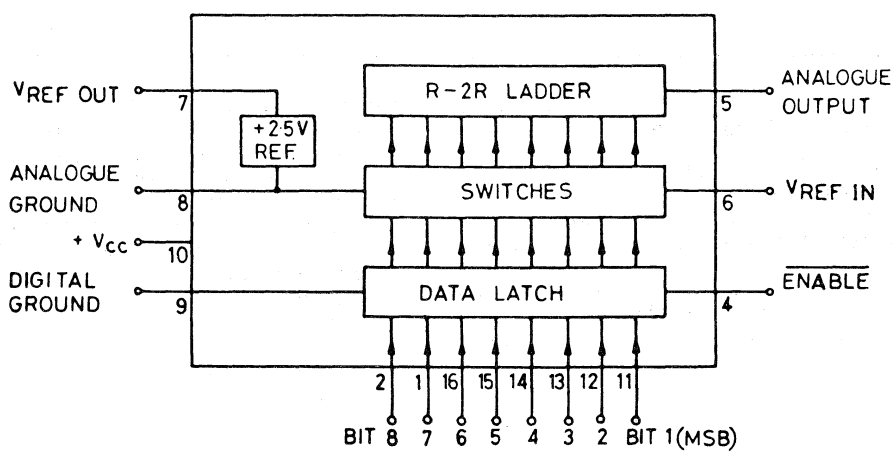



Fig. 3 ZN428 logic diagram

The ZN428 is a monolithic 8-bit D-A converter (DAC), with input latches to facilitate updating from a microprocessor data bus. The latch is transparent when the ENABLE (EN) input is at a logic '0' and the data is held when EN is taken to a logic '1'.

The ZN428 features single +5V supply requirements, fast 800ns settling time and is guaranteed monotonic over its full temperature range. It contains a pin optional 2.5V precision bandgap reference identical to the ZN427. The converter is of the voltage switching type and uses an R-2R ladder network. Each 2R element is connected to 0 volt or $V_{REF\ IN}$ by transistor logic switches especially designed for low offset voltage (< 1 millivolt). A binary weighted voltage is produced at the output of the R-2R ladder network, the nominal range being 0 - $V_{REF\ IN}$ volts with a 4kΩ resistance. Other output ranges can readily be obtained by the use of an external amplifier allowing complete versatility in its application.

**The ZN427 microprocessor bus interface**

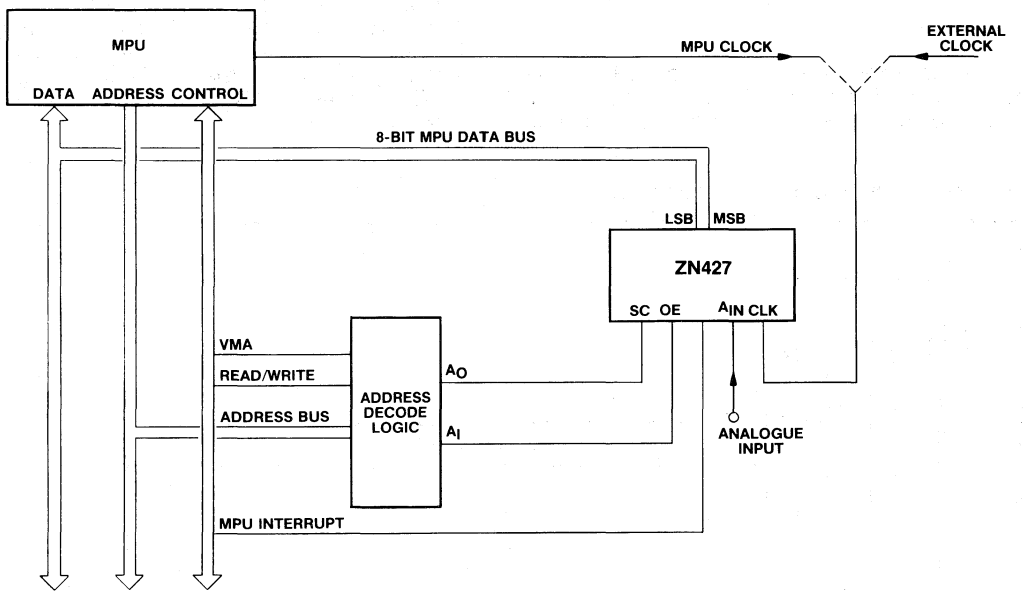



Fig. 4

Peripheral devices can be connected to a microprocessor system by two basic methods. The first and usually the simplest from the point of view of design effort required is to use a peripheral interface I/O device usually found as a support IC in most of the MPU families. With this method the peripheral device is simply connected to the I/O lines of the peripheral interface device and generally no considerations have to be made in terms of bus buffering, bus timing or address decoding.

The second method is to connect the peripheral device directly to the microprocessor data bus. This method is termed "memory mapped I/O" which as its name implies is to make each peripheral I/O function appear to the MPU as a normal memory location, in which case the MPU cannot tell whether it is addressing memory or I/O. This allows the full set of memory reference instructions to be used for I/O data transfer, but it does imply that the peripheral device must be capable of responding at least as fast as the MPU memory and hence it should be compatible with the bus timing characteristics. The disadvantages of memory mapped I/O are that it usually requires additional address decoding logic, and also, since the I/O device will be addressed as memory, then there will consequently be fewer addresses available for actual memory.

It is with this second method of interfacing that this application note is primarily concerned.

A variation of memory mapped I/O, sometimes known as "I/O mapped I/O" is available on some MPUs which overcomes the last disadvantage referred to. This allows a defined range of memory address also to be used for I/O by means of separate I/O instructions. A special control line is required to inform the memory and I/O device whether the address of the current READ or WRITE cycle refers to memory or to I/O. This technique however does restrict the freedom of the programmer to the use of these I/O instructions which normally only operate on data in the microprocessor accumulator.

Fig. 4 shows the basic memory mapped interface for the ZN427 where the 8 binary outputs of the ADC are connected directly to the MPU data bus. The control inputs, START CONVERSION and OUTPUT ENABLE are shown driven from address decoder logic, the function of which is to drive the appropriate input when the address which has been allocated to that particular input is present on the address bus and the control bus signals indicate a valid memory read or write operation. Note that the level of address decode logic used must ensure that the three-state data outputs of the ZN427 are disabled at all times except when the actual ADC data is required on the data bus, otherwise bus contention problems may occur with other devices using the bus. The END OF CONVERSION output can be connected directly to an MPU interrupt to signal the completion of the conversion cycle by the ADC. The ZN427 clock can be driven either from the MPU clock or from an external source. If however the former method is employed, it may simplify the design of the interface with regard to the timing criteria of SC input. (This is covered in more detail later.)

**The ZN428 microprocessor bus interface**

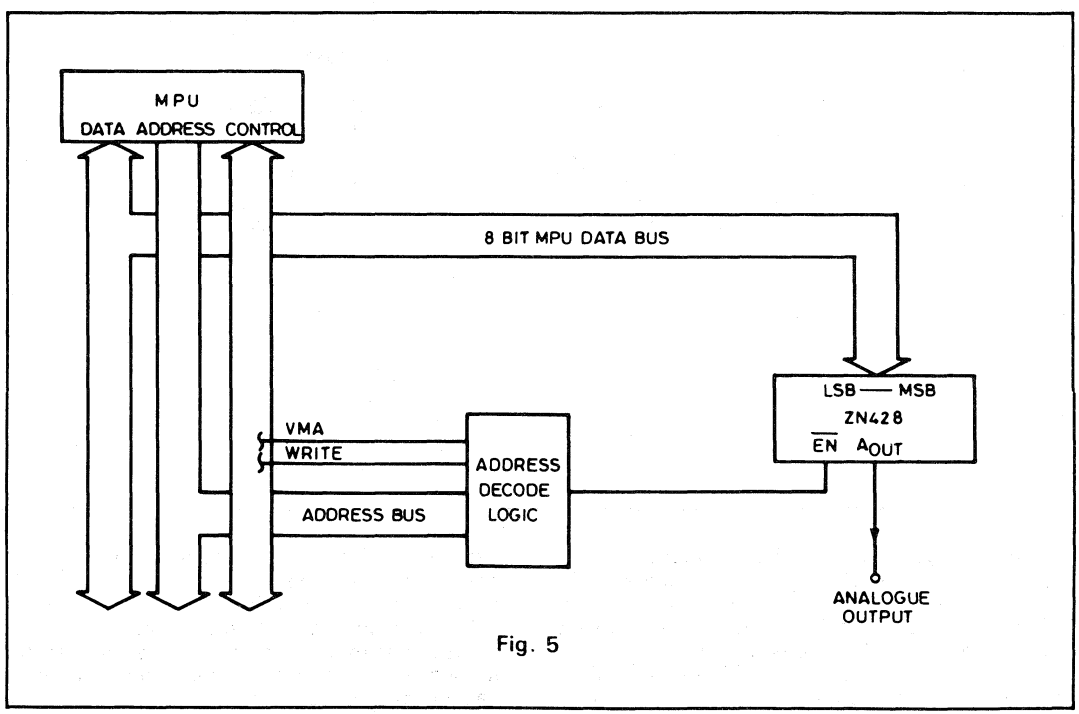



Fig. 5

The ZN428 data inputs can be directly connected to an MPU data bus when in the memory mapped configuration, this is illustrated in Fig. 5. For this application the address decode logic has only to generate the $\overline{\text{ENABLE}}$ signal for the DAC. This is accomplished by gating the MPU WRITE signal with the decoded address signal in order that when a memory write instruction to the DAC address location is executed, then a negative going pulse is applied to the EN input which will transfer the binary code from the data bus to the ZN428 input latches.

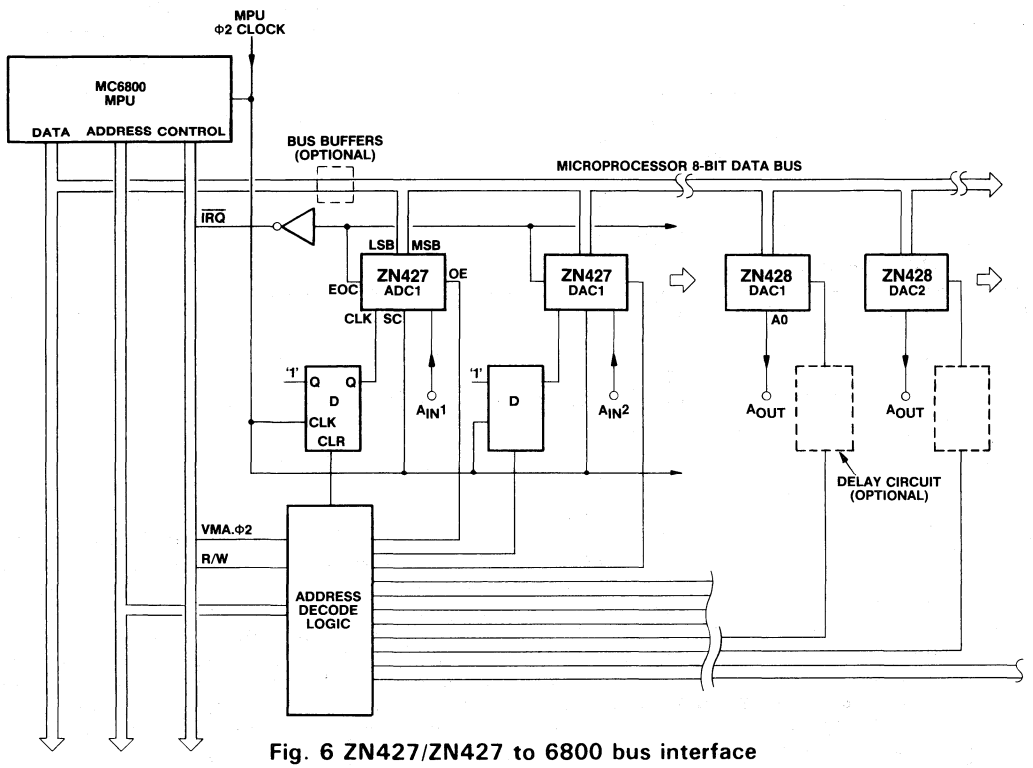



**Fig. 6 ZN427/ZN427 to 6800 bus interface**

With the ability of the ZN427 and ZN428 to be bus compatible it is possible to produce a complete analogue I/O system, specifically configured to the designer's own requirements with the converters connected directly to the MPU data bus. Such a system is illustrated in Fig. 6 build around a 6800 MPU.

The 6800 is an 8-bit monolithic microprocessor which forms the central control function for the 6800 microprocessor family. Fully compatible with TTL logic the 6800 requires only a single +5 volt power supply, it features a set of 72 instructions with 7 addressing modes and full 65K byte memory addressing capability. The microprocessor communicates with its external memory and all I/O peripherals over an 8-bit bi-directional data bus and a 16-bit address bus. (Full data on the 6800 microprocessor is readily available from its manufacturers and their distributors).

The number of ZN427s and ZN428s which can be hung on the data bus is not limited, the only restrictions being the total load presented to the data bus and the number of decoded address lines available. The loading and drive characteristics of the converters are summerised in Table I. Optional bi-directional bus buffers are shown in the diagram, these can be used to expand the system. Use of these will be dependent on the total number of converters used, other peripheral and memory devices on the data bus, and other loading factors such as physical length of bus required.

| ZN427 | | ZN428 | |
|---|---|---|---|
| Parameter | Specification | Parameter | Specification |
| $I_{IL}$ | $-5\mu A$ max. | $I_{IL}$ | $-5\mu A$ max. |
| $I_{IH}$ | $15\mu A$ max. | $I_{IH}$ | $20\mu A$ max. |
| $I_{IH}$ (Clock) | $30\mu A$ max. | | |
| $I_{OL}$ | 1.6mA min. | | |
| $I_{OH}$ | $-100\mu A$ min. | | |
| $I_{OHX}$ (Off state leakage) | $2\mu A$ max. | | |

(NOTE: Currents specified at 0.4V and 2.4V).

**Table 1 Loading characteristics of the ZN427 and ZN428**

The level of address decoding will depend on the overall MPU system design. This can range from merely using the upper address lines directly with no hardware decoding to provide the control lines for the converters - which rapidly depletes the number of address locations available for memory, through to full address decoding where all 65K addresses can be utilised. The address decode hardware can usually be produced from a few TTL gates in association with an address decoder I/C such as the 74154. In order to avoid addressing problems it is necessary on the 6800 to qualify the decoded address with the valid memory Address (VMA) and $\phi 2$ clock signals. The READ/WRITE control line can also be utilised to permit a single decoded address to control each ZN427, i.e. WRITE instruction to the specific address would generate the SC signal and a READ instruction of the same address would enable the converter outputs and read the data. The function of the 'D' type flip-flops shown in the diagram is to ensure that the timing criteria of the SC pulse are met. The requirements for this are that the SC pulse should start at least $1.5\mu s$ before the first active (negative going) clock edge after the SC pulse, and that the trailing edge of the SC pulse must not occur within $\pm$ 200ns of a negative going clock edge, see Fig. 2. By careful design of the address decode logic when deriving the converter clock from the MPU it is possible to produce the correct timing for the SC pulse and to dispense with the 'D' type flip-flops.

The other advantages of using the MPU clock is that it allows an accurate calculation of the ZN427 conversion time to be made in terms of the MPU machine cycles. Again with reference to Fig. 2 it can be seen that the conversion cycle always takes less than 10 clock cycles after the end of the SC pulse. Hence instead of using the EOC output to drive MPU $\overline{IRQ}$ input a simple programme delay loop can be substituted. Note that the EOC outputs of up to five ZN427s can be 'wire-anded' together to form a common interrupt line.

The clock frequency of the standard 6800 is 1MHz which can be used directly to drive the ZN427's if a small loss of accuracy can be tolerated. The 6871B MPU clock generator is produced in a version with a 614.4kHz clock signal. This is only marginally higher than the specified ZN427 clock rate of 600 kHz and the $\phi 2$ TTL output of this can be used directly for the converter clock if full accuracy is essential.

With the 6800 it may be necessary to delay the decoded address enable signal to the ZN428 converters if glitch free operation is desired. This is due to the fact that during a write operation on the 6800 the address and address qualifying control signals become valid before the data bus signals are valid, thereby enabling the DAC before the data is established on the data bus.

The analogue output can be taken directly from the ZN428 output pin which provides a nominal output range from zero volts to $V_{REF\ IN}$ with a 4k$\Omega$ output resistance. For most applications higher output ranges or drive will be required. This can easily be accomplished on the ZN428 by the addition of an external buffer amplifier which can be chosen for the specific characteristics required. The ZN428 is provided with separate analogue and digital ground pins which should normally be connected together close to the I.C. For noisy systems or environments an improvement may be obtained, in some cases, by running the two ground pins to supply ground separately, taking the analogue ground of each ZN428 to a single common earth point in the system away from the sources of high noise such as clock oscillators, digital buses, etc. Note that the maximum voltage between the analogue and digital ground pins should not be allowed to exceed 200mA.

Both the ZN427 and ZN428 contain a nominal 2.5V internal bandgap voltage reference. Use of this on-chip reference is pin optional to retain flexibility and an external reference can be substituted which allows ratiometric operation over the range of typically 1.5 to 3V. The on-chip reference is capable of supplying the reference voltage for up to five ZN427s and ZN428s. This useful feature saves power, discrete components and gives excellent gain tracking between the converters in a system. The tail current for the comparator on the ZN427 is derived via an external resistor from a negative supply. By suitable choice any negative supply of between $-3$ and $-30$ volts may be used. Since the negative current is only of the order of 65 microamps per converter then for applications where only a positive supply is available a simple diode pump circuit can be used.

With a memory mapped interface the full range of memory reference instructions are available to the programmer in order to control the converters, and programming becomes a relatively simple matter of reading and writing data to the addresses allocated to the converters. For example, for the ADCs a conversion cycle could be initiated by a store accumulator command (STA A) to address location ALOC 1, where ALOC 1 is the address of the ADC to be accessed. The contents of the MPU accumulator 'A' at this time are irrelevant since we only want to generate a memory write cycle to produce a pulse at the SC input. Now one can either enable the MPU interrupt and wait for the EOC output to generate an interrupt signal if this is the method used or alternatively a simple programme delay loop can be entered to produce a delay of $\geqslant 9$ converter clock cycles (i.e $\geqslant 15\mu$s if a 600kHz clock is used). Upon receipt of an interrupt or completion of the delay a load accumulator command (LDA A) can be performed on address ALOC 1. This will read the binary data from the converter into the MPU accumulator 'A'. It is even simpler to programme the DACs. All one needs to do is to load the value to be outputted to say accumulator 'A' in binary format. A store accumulator command (STA A) is then programmed to address location ALOC 2, where ALOC 2 is the address allocated to the DAC. Upon execution of this the data will be transferred from the accumulator via the data bus to the DAC input latches and be present at the DAC output in analogue form within 1.25 microseconds of the enable pulse.

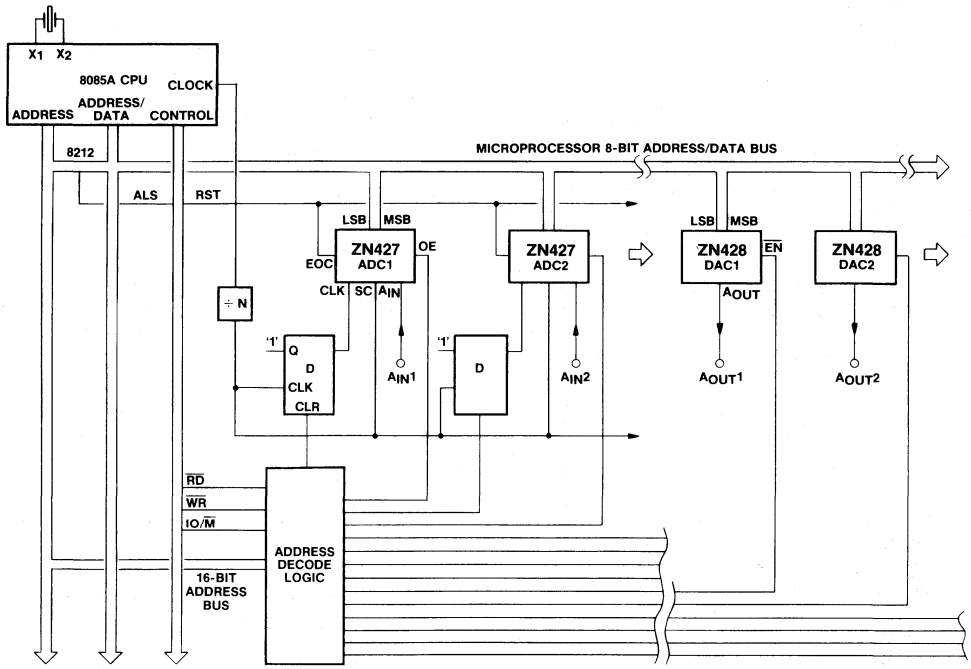



**Fig. 7 ZN427/ZN428 to 8085 bus interface**

An analogue I/O system for the 8085A microprocessor is shown in Fig. 7. This is similar to the 6800 system but the following exceptions should be noted.

The 8085A is another popular 8-bit microprocessor. However, unlike the 6800 this MPU uses a multiplexed data bus whereby the lower 8 address bits A0-A7 are time shared with the 8 data bits. The address bus contains the upper 8 bits A8-A15. If the lower 8 address bits are to be used for address decoding then it is preferable to de-multiplex the bus using an 8 bit latch, such as the 8212, strobed with the address latch enable (ALE) signal from the MPU. The 8085A offers either memory mapped I/O or I/O mapped I/O by means of a separate control line (IO/$\overline{M}$). This allows use of the 'IN' and 'OUT' instructions to control I/O data transfers and the retention of the full 65K memory locations. If using this method then it is unnecessary to de-multiplex the address/data bus, since only the lower 256 addresses are used for I/O transfers, and the address in the lower 8 bits is mirrored into the upper 8 address bits during this operation.

The standard 8085 clock frequency is 3MHz. Hence it is necessary to divide the output from the 8085A CLK output pin down by a factor of at least 4 to produce an acceptable ZN427 clock. Because of this it is more difficult to synchronise the decoded address signals with the ZN427 clock in order to meet the start pulse timing criteria, and one will usually have to incorporate the 'D' type flip-flops as indicated to generate the SC pulse.

Note that with the 8085A the common EOC line can be used directly to generate an interrupt via one of the 3 restart interrupt inputs. The decoded address input to the ZN428s $\overline{EN}$ input can also be used without any additional delay since, with this MPU the bus data is valid during the time that the WRITE signal is established.

Again programming is very straightforward. With a memory mapped I/O configuration the data transfer commands - move (MOV), load (LDA) and store (STA) can be used to control data transfers between the converters and the MPU. If an I/O mapped I/O configuration is adapted then the input (IN) and output (OUT) commands are used to transfer data between MPU accumulator and the converters.

**Summary**
The analogue I/O systems described in this report are intended only as a guide to illustrate to design engineers the ease and versatility with which these two converters can be used to produce analogue I/O channels for popular 8-bit microprocessors. As a result of the low cost, low external component count and flexibility of these converters, designs based on the 'one converter per channel concept' will be both a practical and economical solution to microprocessor data acquisition problems. This approach should find many new applications in areas which have previously been limited by the necessary usage of traditional data acquisition methods involving a single high cost hybrid ADC utilising sample and hold and multichannel multiplexing techniques.

# A Serial Interface for the ZN427 A-D Converter

**In many data acquisition applications it is advantageous to situate the A-D converter close to the transducer and to transmit the digital data in serial form back to the data collection centre of the system. The serial data link uses less conductors and provides better noise immunity than a parallel data bus. This application note describes a RS-232C compatible serial data interface for the ZN427 8-bit A-D converter using an industry standard 6402 UART. A simplified block diagram is shown in Fig. 1.**

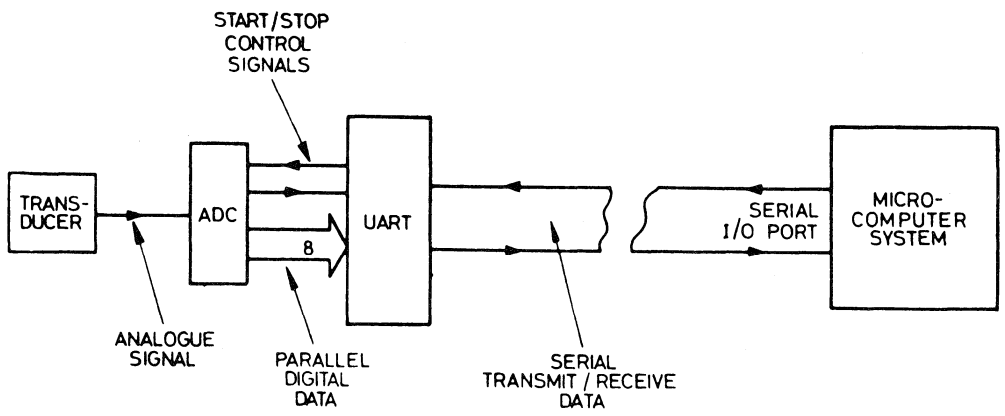



Fig. 1 Serial data interface

In order to initiate a conversion cycle a character is transmitted by the microcomputer. Upon receipt of this character by the UART its DR (data received) output goes to a high level which generates a start pulse for the A-D converter triggering a conversion cycle. At the end of the cycle the EOC (end of convert) output is used to load the converted data into the UART which performs a parallel to serial conversion and transmits the data back to the microcomputer.

The ZN427 is an 8-bit successive approximation A-D converter. It features three-state output buffers to permit bussing onto common data lines, fast 10$\mu$s conversion time and no missing codes over the full operating temperature range.

The ZN427 contains a voltage switching D-A converter, a fast comparator, successive approximation logic, three-state output buffers and a 2.5V precision bandgap reference. A logic diagram of the converter is shown in Fig. 2. Only a few passive external components are required. For basic operation these are an input resistor, a reference current resistor and stabilising capacitor, and a limiting resistor for the negative supply current. This will provide a nominal input voltage range of 0 to $V_{REF\,IN}$. Other input ranges both unipolar and bipolar can be obtained by connecting a simple resistor network to $V_{IN}$ (pin 6) as illustrated in Figs. 3a and 3b. Further information on the ZN427 can be found in the data sheet.

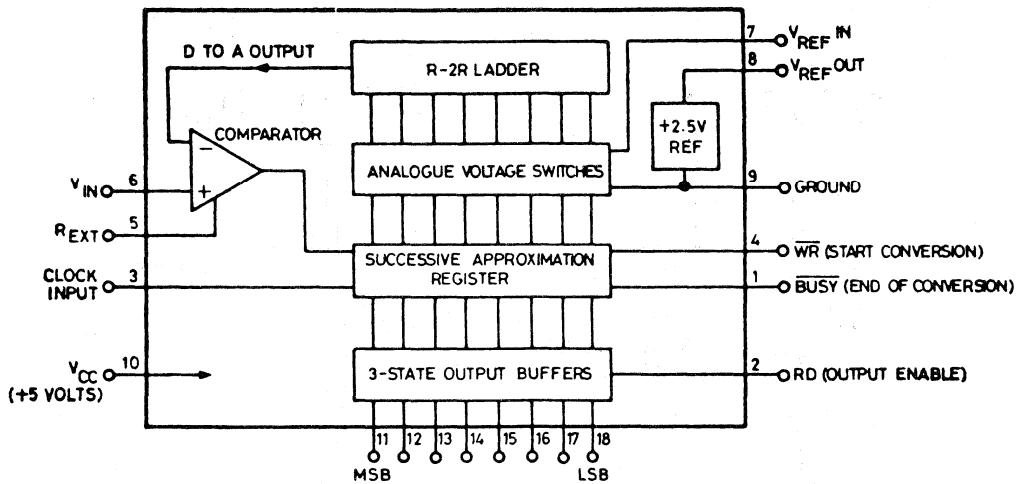



Fig. 2 System diagram

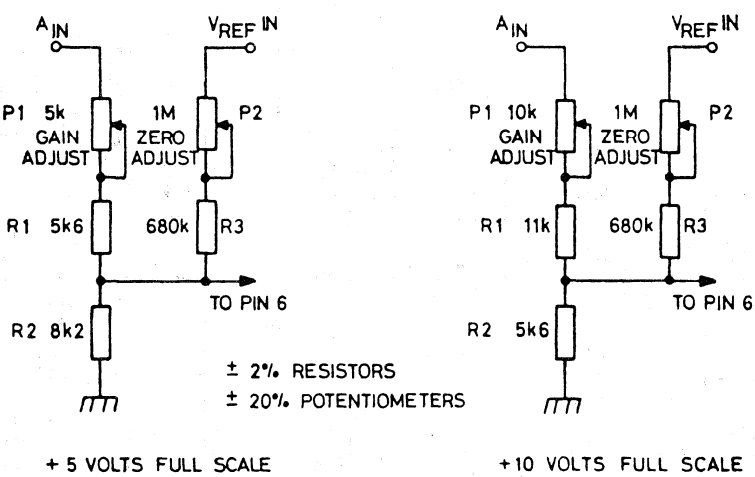



Fig. 3a Unipolar operation - component values

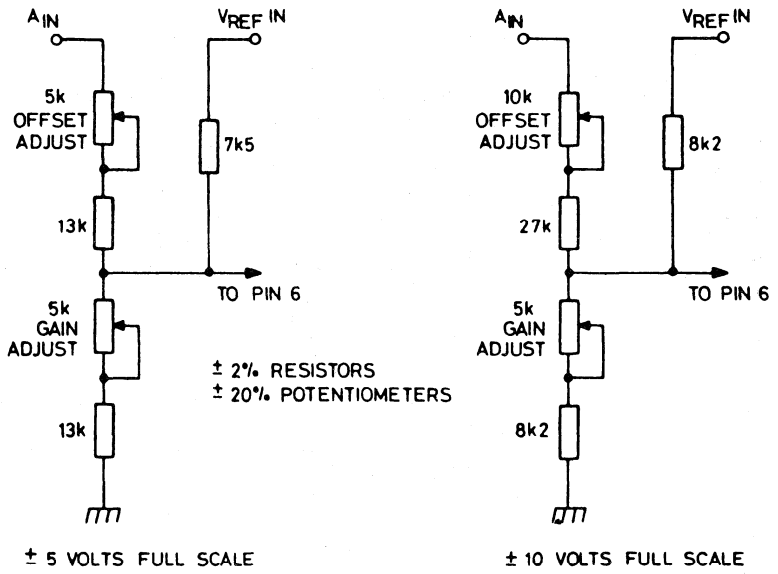



Fig. 3b Bipolar operation - component values

A detailed circuit diagram of the converter interface is shown in Fig. 4.

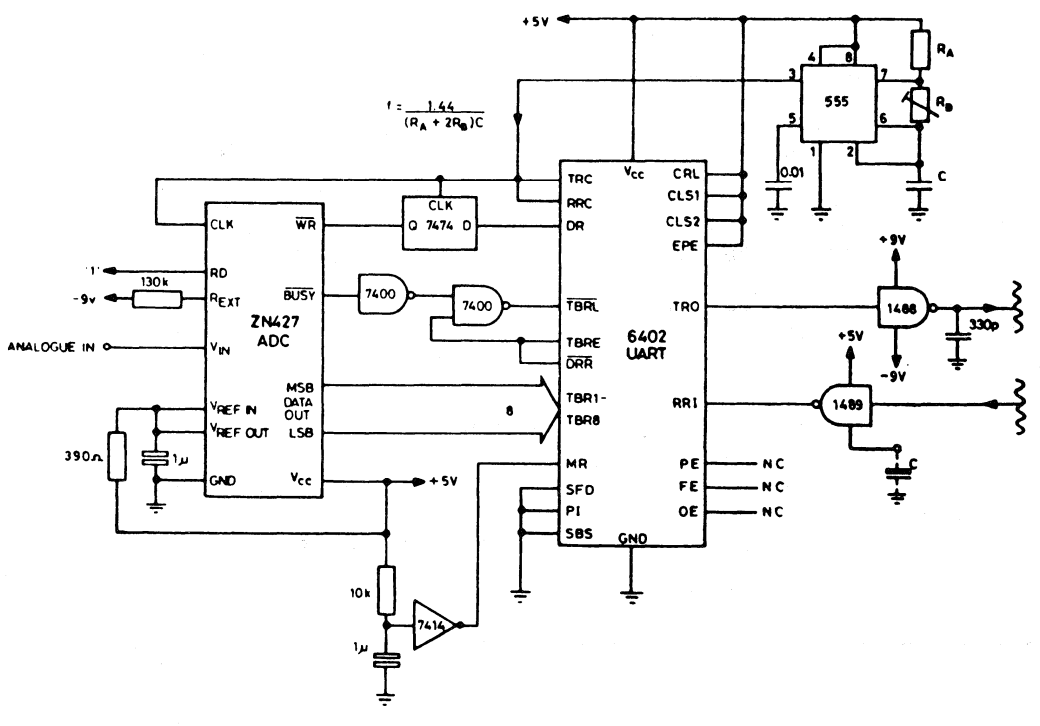



Fig. 4 ZN427 UART interface

The DR output of the UART is connected to the 'D' input of the 7474 latch, the 'Q' output of which drives the $\overline{WR}$ (start convert) input of the ADC. The use of this ensures that the timing of the $\overline{WR}$ pulse with respect to the converter clock input is correct. On the ninth negative clock edge after the $\overline{WR}$ pulse the $\overline{BUSY}$ output goes to a high level signalling that the conversion cycle is complete. This low to high transition is used to load the data into the UART via the TBRL (transmitter buffer register load input). The signal is gated with the TBRE (transmitter buffer register empty) signal which holds the TBRL input high until the UART transfers the data to its transmitter register. If TBRL were allowed to return low before TBRE went high the converter data would be overwritten since the TBR (transmitter buffer register) is a transparent latch. The TBRE signal is also used to drive the DRR (data received reset) input which clears the DR output to a low level allowing another character to be received.

The waveforms associated with this operation are shown in Fig. 5. A simple oscillator using a 555 I.C. is shown which generates both the ADC clock and the transmit/receive clocks for the UART. The external clock is 16 times the data rate, the signal being divided internally by the UART. If a more stable data rate is an important factor then the 6403 UART, which is functionally similar but which uses a crystal oscillator as the timing source, may be substituted. In this case the ADC clock would still be generated by the 555 since it is not necessary for the converter and UART clocks to be synchronised. The UART control inputs CLS1, CLS2 (character length select); PI (parity inhibit); EPE (even parity enable); SBS (stop bit select) are hard wired for whatever data format is wanted.

The MR (master reset) input is driven via a 7414 Schmitt trigger I.C. from a R-C delay circuit to generate the recommended reset pulse after power-up.

The 1488 and 1489 I.C's shown buffering the UART TRO (transmitter register output) and RRI (receive register input) pins are RS-232C compatible line drivers and receivers.

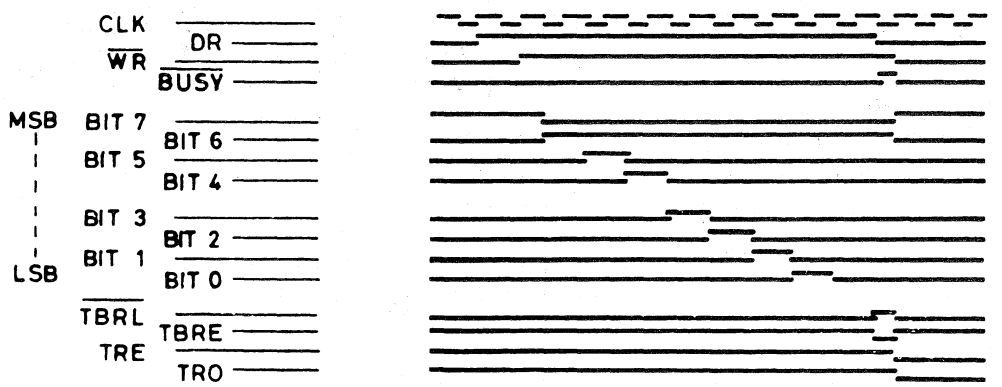



Fig. 5 ZN427 UART interface waveforms

In some applications incorporating microcomputers with RS-232S serial I/O ports no additional interfacing at the data collection centre end will be necessary. However if only a parallel I/O port is provided than another UART to convert the serial data back to parallel will be needed. An interface for the PET microcomputer which connects to the Parallel User Port on connector J2 is shown in Fig. 6. This uses the eight I/O data lines. PA0-PA7 and two control lines CA1 and CB2 which originate from a 6522 versatile interface adaptor I.C. The data lines PA0-PA7 are connected to the RBR (receive buffer register) outputs of the UART. The CA1 input is driven by the UART DR output and is operated in the latched mode which stores the received data within the VIA on a positive transistion of this pin. In order to initiate a new reading from the ADC the remaining control pin CB2 is used. This is connected to the UART inputs DRR and TBRL. When programmed to produce a negative pulse the DR output is reset and a character is transmitted to the converter UART to start a new conversion cycle.

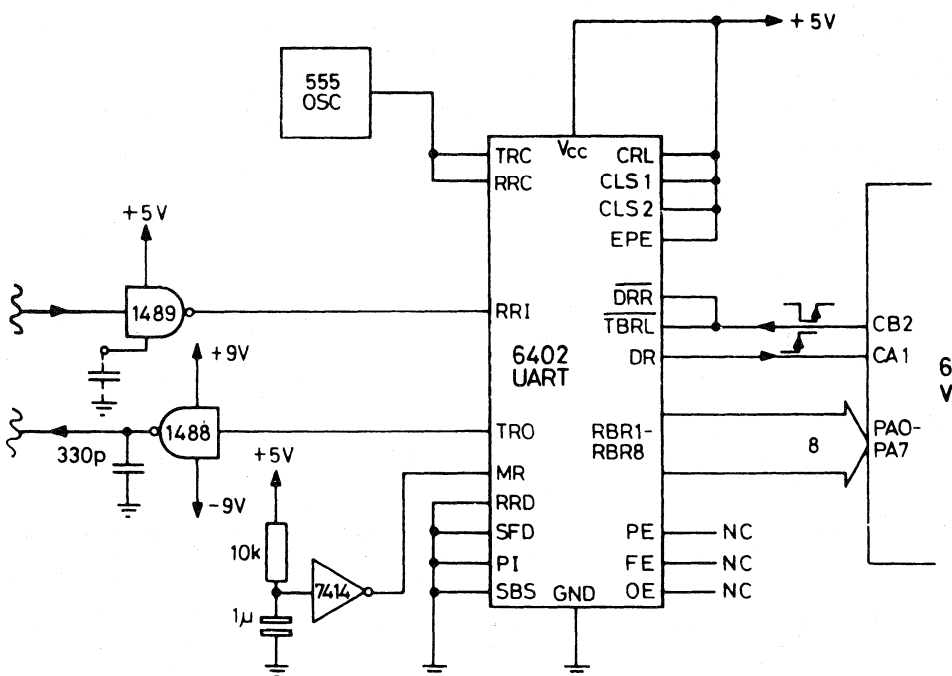



**Fig. 6 6522 VIA UART interface**

A simple program example in PET basic is shown below.

## PROGRAM EXAMPLE

```
 10 REM UART INTERFACE REV. 3
 20 REM SET PORT A TO INPUTS
 30 POKE 59459, 0
 40 REM DISABLE CA1 INTERRUPT
 50 POKE 59470, 2
 60 REM SET PCR TO 111XXXX1
 70 POKE 59468, PEEK (59468) OR 225
 80 REM SET ACR TO XXX000X1
 90 POKE 59467, PEEK (59467) AND 227 OR 1
100 REM CLEAR CA1 FLAG IN IFR
110 A = PEEK (59457)
120 REM PULSE CB2 LOW-HIGH
130 POKE 59468, PEEK (59468) AND 31 OR 192
140 POKE 59468, PEEK (59468) OR 225
150 REM WAIT FOR +TRAN ON CA1
160 REM TEST CA1 FLAG IN IFR
170 IF (PEEK (59469) AND 2) THEN 190
180 GOTO 170
190 REM READ IRA AND CLEAR CA1 FLAG
200 A = PEEK (59457)
210 PRINT A
220 GOTO 120
```

Initially the appropriate VIA internal registers are set up then a negative going pulse is produced on the CB2 pin. This starts a conversion sequence and when the new data is received the CA1 input goes high, latching the data in the VIA, and setting the CA1 flag bit in the interrupt flag register. This flag is tested by the program and when set the data is read and printed out. CB2 is again pulsed low and the sequence repeated.

For 6502 based microcomputer systems where all I/O lines of a 6522 VIA are available the CA2 pin can be used in the read handshake mode in place of the CB2 pin, simplifying the program. Also the status flag of the UART can be monitored by other I/O port lines for error checking purposes.

# Microprocessor Interfacing using the ZN432 10-Bit Data Converter

**This application note describes a monolithic 10-bit accurate analogue to digital (A-D) converter integrated circuit and explains the different techniques of interfacing this to common 8-bit microprocessors using the minimum of external discrete components and standard TTL logic elements.**

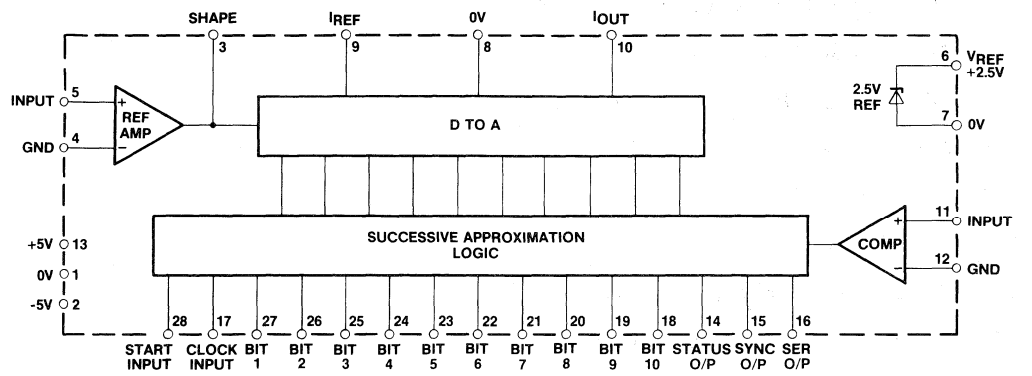



Fig. 1 ZN432 logic diagram

### The ZN432 A-D converter

The ZN432 is a 10-bit A-D converter produced in monolithic form by a silicon bipolar process. The converter is of the successive approximation type and includes an on-chip precision reference, reference amplifier, comparator, successive aprroximation logic and a D-A converter. The D-A converter operates on the unit current source principal with a current switching array using a

matrix of diffused resistors. As a result of incorporating several design and layout innovations and the use of highly developed processing and photomask techniques, 10-bit accuracy is obtained without the need for post diffusion trimming operations. Only a few external components are required, including two capacitors, to shape the internal reference and reference amplifier outputs, and several resistors which define the input voltage range of the converter, which can be either unipolar or bipolar whichever range is required by selecting suitable external resistors. The ZN423 is available in 3 temperature ranges, including full military temperature range, and in either 8, 9 or full 10-bit accurate versions, packaged in a 28 lead hermetically sealed ceramic D.I.L. encapsulation.

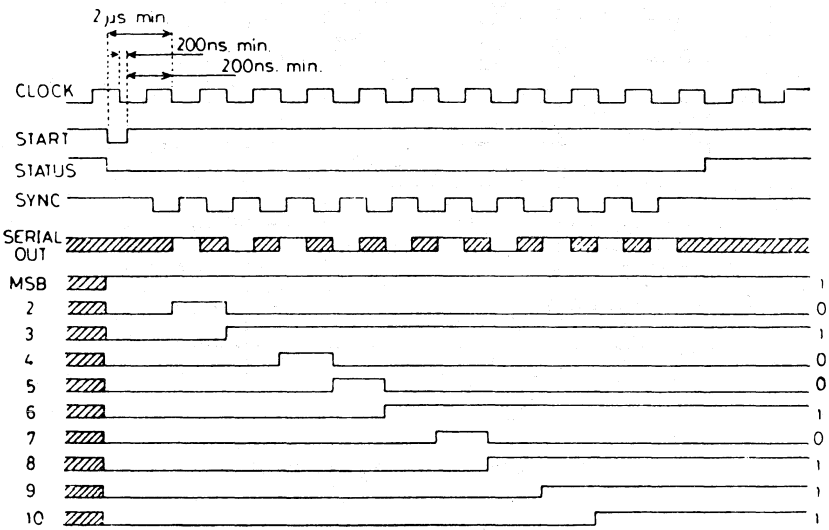



**Fig. 2 Timing diagram**

The operation of the converter can best be described by reference to the timing diagram, Fig. 2. Conversion is initiated by a negative going START pulse which sets the MSB to a logic '1' and all other bits to a logic '0'. The STATUS output is also set to a logic '0' at this time indicating that the converter is busy. The leading edge of the START pulse should occur at least 2$\mu$s before the 1st active negative going edge of the clock and the trailing edge of the START pulse must not occur within $\pm$ 200ns of a negative going clock edge. On the next negative going clock edge a decision is made on whether to set the MSB back to a logic '0' if the input current is less than the D to A output or, if not, it is left at a logic '1'. Bit 2 is switched to a logic '1' on the same clock edge and on the next negative edge a decision is made about bit 2, again by comparing the input current with the internal D to A output. This process is repeated for all 10 bits so that when the STATUS output goes to a logic '1' on the 11th negative clock the digital output from the converter is a valid representation of $V_{IN}$. A SERIAL DATA output is also provided on the ZN432, this data is outputted during the conversion cycle and is valid on the positive going edge of the pulses on the SYNCH output.

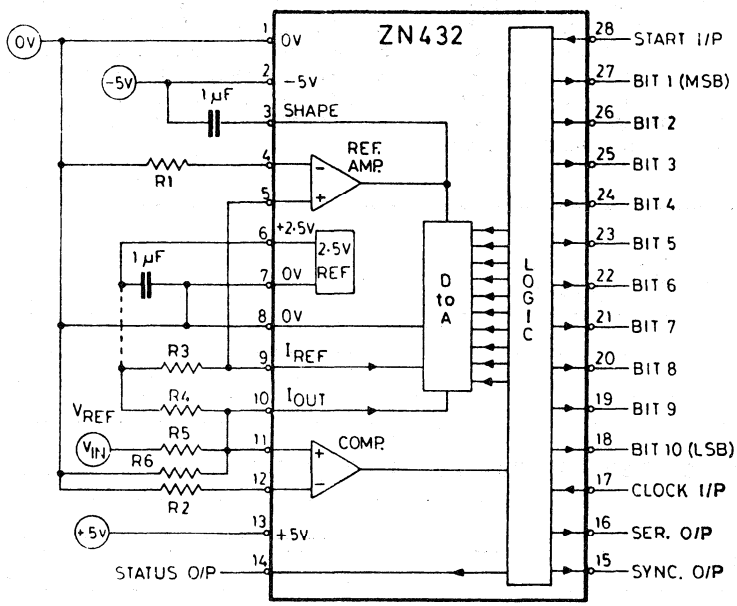



**Fig. 3 Typical external components**

A diagram showing typical external components for the ZN432 is shown in Fig. 3. The capacitor on pin 3 is used to stabilise the reference loop whilst that on pin 6 is for stabilisation and decoupling of the voltage reference output. Resistors R1 and R2 control the bias current of the reference amplifier and compartor, R3 defines the D-A reference current, R4 and R5 set the input voltage range and R6 is selected to obtain a suitable D-A time constant. For setting up, R3 will adjust the converter gain and R4 the offset. As an example, the resistor values for a ±10 volt input range are:

R1 = 5kΩ
R2 = 1.25kΩ
R3 = 5kΩ
R4 = 2.5kΩ
R5 = 10kΩ
R6 = 3.33kΩ

Resistors R3, R4 and R5 affect gain and offset and hence high stability types should be used whereas the nearest preferred values may be chosen for R1, R2 and R6. Refer to the ZN432 series data sheet for more information on the selection of external components.

**Interfacing data converters to microprocessors**

Peripheral devices can be interfaced to microprocessor systems by two basic methods. The first and simplest is to use a general purpose I/O device, (also known as peripheral interface adapters, versatile interface adaptors or programmable peripheral interfaces, etc.). Most microprocessor systems on the market usually include one or more of these components in their microprocessor systems family. They normally consist of one or more data ports, usually of 8 bits which can be programmed to function either as inputs or outputs. With some devices the complete port has to be programmed to function either as all inputs or all outputs, but the more useful I/O devices allow the individual pins of each port to be programmed separately as inputs or outputs. In addition most devices also feature several control lines for the purposes of generating handshake signals with peripherals and generating microprocessor interrupts etc.

The second interface method is to connect the peripheral device directly to the microprocessor data bus. This method is termed memory mapped I/O which as its name implies, is to make each peripheral I/O function appear to the microprocessor as a normal memory location. This allows the full set of memory reference instructions to be used for I/O data transfer, but also implies that the peripheral device must be capable of responding at least as fast as memory, and hence it should be compatible with the MPU bus timing characterisitics. With 10-bit converters a problem exists when using this method in that the 8-bit data bus is not wide enough to handle the converter data as a single word. It is therefore necessary to split the data into two words usually of 8 and 2 bits which are fed to the data bus in two separate bytes by means of appropriate gating on the converter outputs. Naturally when using a 16-bit microprocessor this problem does not arise, as converter data can then be read as a single word on the data bus. The disadvantages of memory mapped I/O are that it usually requires additional address decoding logic and also, since the I/O will be addressed as memory, there will consequently be fewer addresses available for actual memory. A variation of memory mapped I/O commonly referred to as I/O mapped I/O or isolated I/O is available on some microprocessors which overcomes this last disadvantage. This allows a defined range of memory addresses to be used also for I/O by means of separate input and output instructions. A special control output is used to tell the memory I/O devices whether the address of the current read or write cycle refers to memory or to I/O. This technique, does, however, restrict the freedom of the programmer to the use of these input/output instructions which usually operate only on data in the microprocessor accumulator.

So far we have dealt with interfacing to the ZN432 using the parallel binary outputs, alteratively the serial output can be used in applications which demand that the number of lines to the converter need to be kept to a minimum. Two schemes are briefly described here although other variations are possible. The first would be to connect the serial output to one I/O pin of an I/O device and to use the status output to generate microprocesor interrupts via one of the I/O device control inputs, thereby reading the serial data from the I/O device on the positive going edge of each pulse on the status output. The other method is to use a microprocessor with a direct serial input port such as the 8085A. This would either involve synchronising the converter clock to a sub-multiple of the microprocessor clock and programming the microprocessor to read the data at the correct time, or by again using the status output to generate an interrupt. Unfortunately both these methods restrict the maximum converter clock period to a minimum of at least several instruction execution times i.e. the time needed to interrupt the microprocessor, read the data and store it in memory. Another option open to the designer would be to use a cascadeable shift register with three-state outputs (i.e. a TTL 74LS395A) at the microprocessor and to convert from 10-bit serial to parallel data which would then be applied direct to the data bus in 2 words via the three-state outputs.

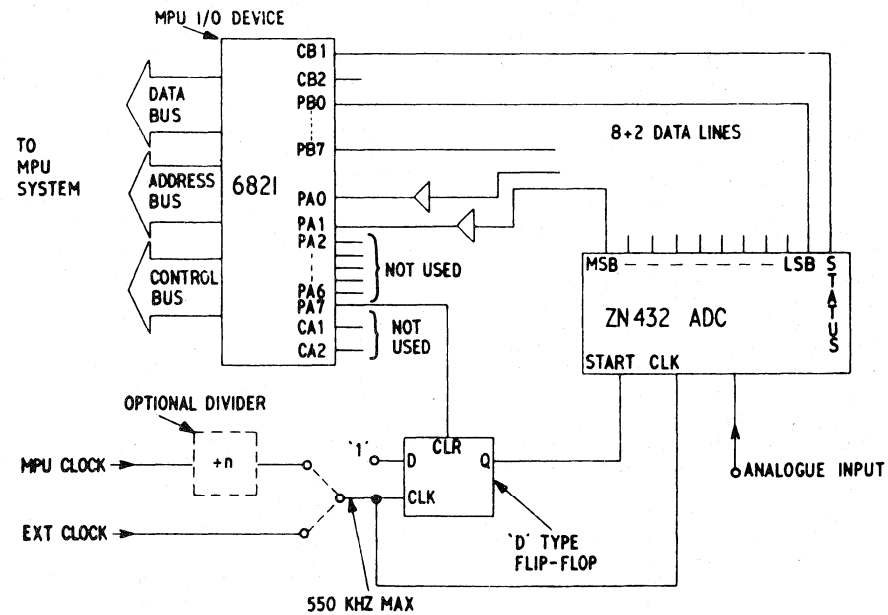



Fig. 4 ZN432 - 6800 I/O interface

Fig. 4 illustrates one configuration of interfacing the ZN432 to an I/O device; in this case the 6821 peripheral interface adaptor (PIA) device of the 6800 microprocessor family.

The PIA provides a flexible means of interfacing byte orientated peripherals to the microprocessor through two 8-bit bi-directional peripheral data lines and four control lines. The functional configuration of the PIA is under the full control of the microprocessor. Each of the peripheral data lines can be programmed individually to act either as an input or an output and each of the four control lines may be programmed for one of several control modes.

The diagram shows all 8 lines from port B and two lines from port A connected to the binary outputs of the ZN432. These lines are programmed as inputs and allow the microprocessor to read the converted data by the execution of a microprocessor read peripheral data operation. Note the use of the two buffers on data lines PA1 ad PA2, these are necessary due to the higher input current of the port A inputs.

The converter clock can be supplied either from the microprocessor clock or from the external source. Use of the microprocessor clock is preferrable since this allows a precise calculation to be made of the conversion time in terms of microprocessor machine cycles. If, however, the microprocessor clock is greater than the maximum converter clock rate of 550kHz then it must be divided down to an acceptable level.

The 'D' type flip-flop is used to generate the start pulse for the converter from the PA7 line, programmed as an output. The function of this flip-flop is to ensure that the start pulse timing criteria with respect to the clock are met as explained earlier.

The STATUS output from the ZN432 is connected to CB1 control line. This can be programmed to set the interrupt flag bit-7 in control register B of the PIA, on occurance of a positive transition of the CB1 input signal. The contents of this register can be read by the mciroprocessor and the state of this bit tested to determine the completion of the conversion

cycle. Alternatively the PIA can be programmed to generate a direct microprocessor interrupt from the status signal on CB1. In this case, an interrupt routine in the program would be accessed on completion of a conversion and this would transfer the converter data via the PIA to defined storage locations in microprocessor registers or memory. This method is really only necessary if maximum utilisation of microprocessor time or converter data throughput is required. For situations where this is not critical the converter clock can be synchronised to the microprocessor clock as previously described, and a delay loop built into the program to allow for the conversion time. Since this is only 20$\mu$s when running at the maximum clock rate a delay loop of only a few instructions will be sufficient to produce adequate delay.

A typical program to control the converter may be organised as follows:

Initially the PIA would be set-up with PB0-PB7, PA0 and PA1 as inputs, PA7 as an output and control register B set to generate a microprocessor interrupt on a positive transition of the CB1 input. Note that the remaining lines PA2-PA7, CA1, CA2 and CB2 are unused. A logic '0' followed by a logic '1' is then written to PA7; this clears the 'D' type and sets the START input, via the Q output, to a logic '0'. On the first positive going clock edge after PA7 returns to logic '1' the Q output is clocked to a logic '1' allowing the ZN432 conversion cycle to proceed. (Note that it is not important if the START input is held low for several clock cycles, it will simply hold the converter with the MSB at a logic '1' and all other bits at a '0'). On the 11th negative clock edge after the start pulse the STATUS output goes to a logic '1' indicating that the ZN432 had finished the conversion. This postive transition activates the $\overline{IRQ}$ line of the 6800, via the PIA, causing an interrupt. The 6800 stops execution of the current program sequence and begins an interrupt sequence. This involves saving the microprocessor register contents on the stack and setting the Interrupt Mask Bit so that no further interrupts will be serviced. The microprocessor is then directed to a vectoring address and branches to an interrupt routine in memory. This routine will read the converter data, via the PIA by addressing ports A and B in turn and will then either store the data away in memory for future use, or will test the data and act accordingly on the results. Reading the data on port B of PIA also has the affect of clearing the interrupt flag bit. Resumption of the interrupted program sequence can now be made by execution of a return from interrupt (RTI) instruction.

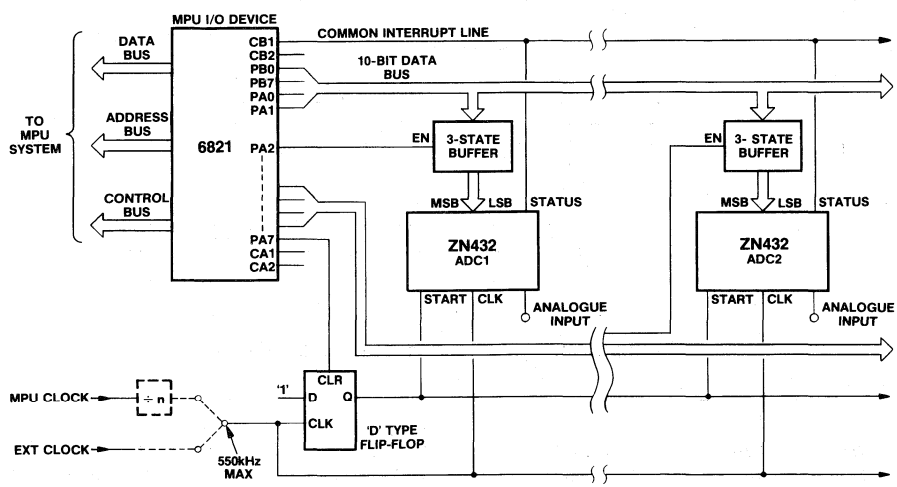



**Fig.5 Multiple ZN432 6800 I/O interface**

The configuration illustrated in Fig. 5 shows a suggested scheme for interfacing several ZN432's to an I/O device. This arrangement is similar to that previously described but in this circuit three-state buffers are used to interface each ZN432 to a common 10-bit bus from the PIA. The previously redundant lines PA2-PA6 are now used to provide the enable signals for the three-state buffers. Note that the buffers of only one converter should be enabled at any one time otherwise false data will be read from the PIA.

The STATUS output of the ZN432 has a resistive pull-up load allowing typically up to 4 outputs to be 'wire-anded' together to form a common interrupt line. With the particular configuration shown a common start signal for all the converters is produced, again from PA7 via the 'D' type flip-flop. Application of this signal would start all the converters simultaneously and a positive transistion on the CB1 line would signify that all the converters had finished. Data from each converter would then be read by enabling the three-state buffers via lines PA2-PA6 in turn.

**A ZN432 Bus interface**

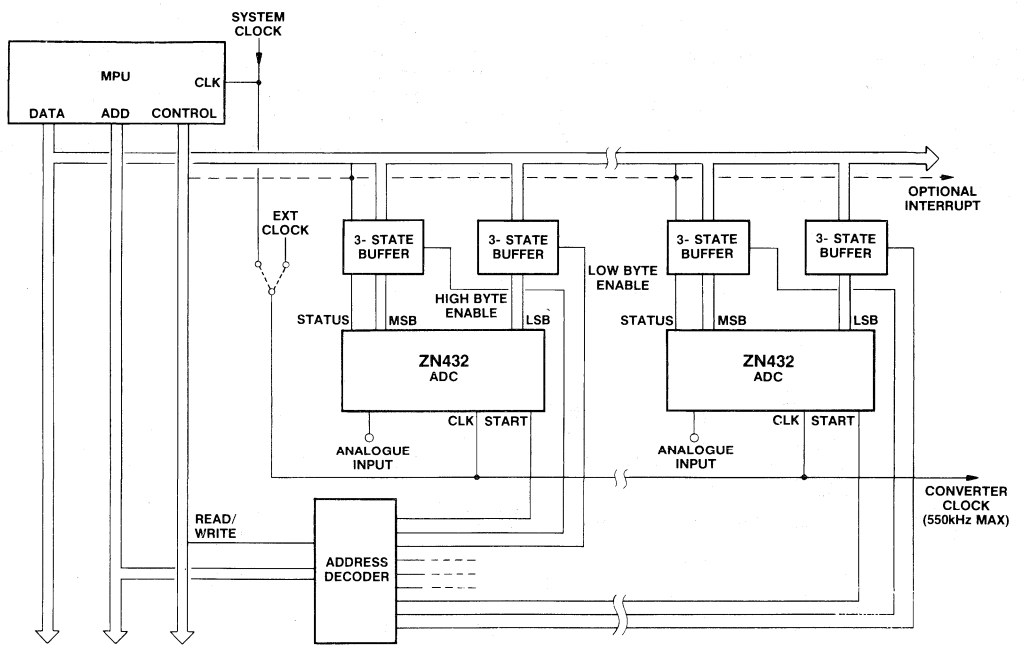



**Fig.6 Multiple ZN432 microprocessor bus interface**

The most versatile way of interfacing to a microprocessor is to go directly onto the data bus. Fig. 6 illustrates this concept with the ZN432 where three-state buffers are again used but this time connected directly to the date bus of an 8-bit microprocessor such as the 6800. Since it is only an 8-bit bus the converter data has to be read in two words by enabling the buffers per converter in two groups as indicated by the high and low byte enable lines per converter. One suggested scheme would be to transfer the output data as shown in Table 1. (Note that in converter terminology bit 10 is the least significant bit (LSB).

**Table 1**

| Data bus lines | Low byte | High byte |
|---|---|---|
| D7 | Bit 3 | – |
| D6 | Bit 4 | – |
| D5 | Bit 5 | – |
| D4 | Bit 6 | – |
| D3 | Bit 7 | – |
| D2 | Bit 8 | (Status) |
| D1 | Bit 9 | Bit 1 (MSB) |
| D0 | Bit 10 (LSB) | Bit 2 |

The STATUS output can be read on the data bus with the high data byte or alternatively these outputs can be 'wire-anded' or gated together to produce a common interrupt signal.

The start pulse and high and low byte enable signals are generated from a logic block labled 'address decode logic'. The function of this is to drive the appropriate input when the address, which has been allocated to that particular input, is present on the address bus and the control bus signals indicate a valid memory read or write operation. Note that the level of address decoding used must ensure that the three-state buffers are disabled at all times except when the actual converter data should be on the bus, otherwise bus contention problems, with other devices using the bus may occur. A convenient means of address utilisation for the system in Fig. 6 is shown in Table 2, which allocates two consecutive addresses to each converter.

**Table 2**

| Address | MPU read | MPU write |
|---|---|---|
| XXX 0 | High byte enable ADC1 | Start ADC1 |
| XXX 1 | Low byte enable ADC1 | Start ADC1 |
| XXX 2 | High byte enable ADC2 | Start ADC2 |
| XXX 3 | Low byte enable ADC2 | Start ADC2 |
| XXX 4 | High byte enable ADC3 | Start ADC3 |
| etc. | etc. | etc. |

(XXX = unique address for particular MPU system.)

A write instruction to either address will then start that converter. On completion of the conversion, detected either by interrupt, testing of the status bit, or fixed program delay, the converter data can be read by a double byte load instruction which will load the data into two consecutive RAM memory locations or into a 16-bit microprocessor register, (i.e. instruction LDX - load index register of the 6800, loads the more significant byte of the index register from the byte of memory at the address specified by the program and loads the less significant byte of the index register from the next byte of memory at one plus the address specified by the program).

Note that the 'D' type flip-flop is not shown in Fig. 6. With a direct microprocessor clock it is possible to design the address decode logic so that the timing criteria of the start pulse with respect to the clock input is complied with.

**Summary**

Numerous different microprocessors are currently available and each microprocessor based control system will have its own individual data acquisition requirements. It is impossible in a paper of this type to cover all possible permutations of microprocessor/converter interfaces, but adoption of one of the two basic methods described here should be possible with most 8-bit microprocessors, allowing the design engineer to produce the most efficient data acquisition system to meet his design objectives. The ZN432's versatility and ease of use, coupled with its wide operating temperature range and TTL compatibility, will allow it to be used in a diverse range of applications where 10-bit accuracy is necessary.

Further information on the device characteristics and gain selection components, etc., is given in the ZN432 series data sheet.

# Introduction to the ZN433 10-Bit Tracking ADC and How to Evaluate Design Performance

**The ZN433 is a monolithic 10-bit tracking A-D converter which, as its description implies, is capable of following changing analogue inputs. It uses an UP/DOWN counter, a DAC and a window comparator, as shown in the schematic diagram, Fig. 1. A window comparator is similar to a normal comparator except that, at the input, there is a 'dead band' or 'window' within which the output will not change state. This window is normally ± ½ LSB wide.**

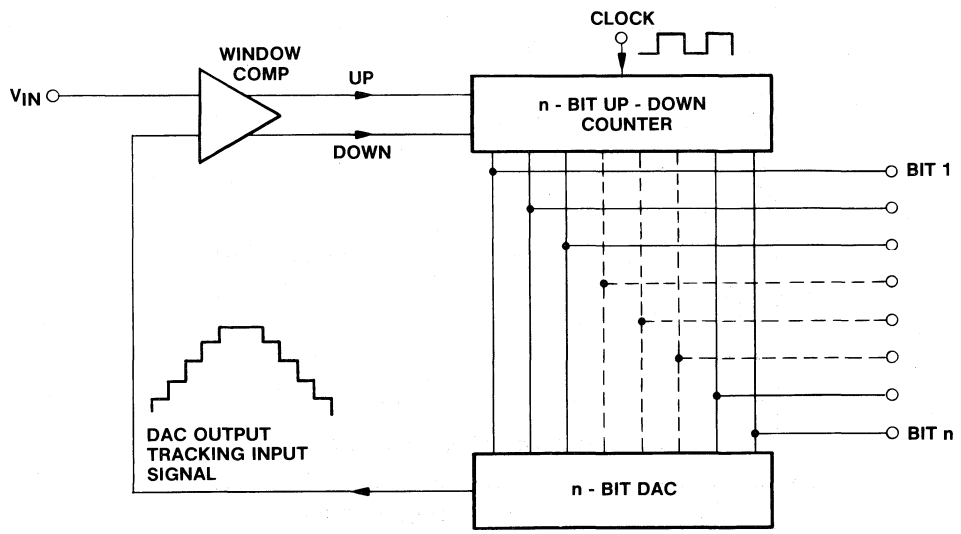



**Fig.1 Tracking ADC**

When the DAC output is less than the analogue input the comparator instructs the counter to count up and the DAC output thus increases. If the DAC output is greater than the analogue input the comparator causes the counter to count down, thus decreasing the DAC output. When the DAC output is equal to the analogue input ±½ LSB, the input is within the 'window' of the comparator and the counter is stopped. This is illustrated in Fig.2.

A tracking converter can have speed advantages over the staircase and compare and successive approximation type of converters, since the counter of the latter two can only count up and must therefore be reset between conversions.

If the rate of change of the analogue input is always less than 1LSB per clock period then a tracking converter will acquire and track accurately the input voltage and the conversion time will be one clock period. The staircase and compare converter would have to reset its counter to zero and then count up again until the new count is reached. A successive approximation converter would take at least n-½ clock pulses, where n is the number of bits.

As an extreme example consider an analogue input that changes from VFSO to (VFSO-1LSB). The staircase and compare converter will require $2^n - 1$ clock pulses for the first conversion and $2^n - 2$ clock pulses for the second conversion.

The tracking converter on the other hand, will require $2^n - 1$ clock pulses for the first conversion but only 1 clock pulse for the second conversion. This is illustrated in Fig.3.

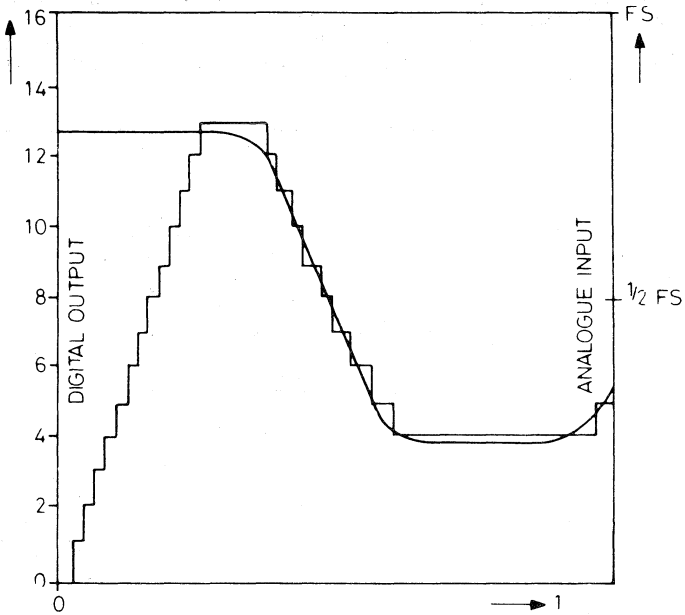



**Fig.2 Operation of tracking ADC**

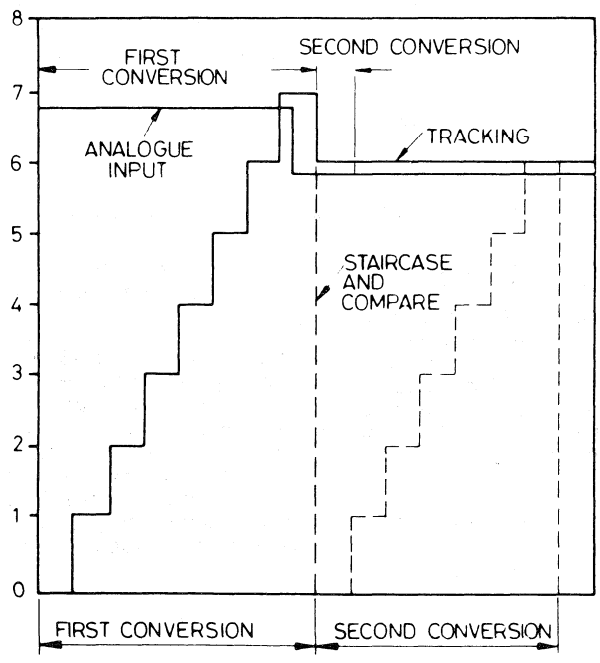



**Fig.3 Comparison of ramp and compare and tracking ADCs**

In general it can be said that a tracking converter will follow signals whose rate of change is less than ±1 LSB/clock period. If this condition is met there is no need to use a sample and hold circuit on the analogue input.

The Plessey ZN433 has a maximum clock rate of 1MHz. It is capable of generating parallel or serial output data. The data can be latched (by pin 28) and read out serially or in parallel as required. If desired the outputs can also be disabled by applying a low to send data (pin 17).

The evaluation board is designed to be versatile in demonstrating the properties of the ZN433. The outputs can either drive LED's via inverting buffers and give a visual indication of the output states, or be connected to a bus via non-inverting tristate buffers. The outputs and $\overline{\text{ENABLE}}$ of these buffers are connected to a 20-way speedbloc connector (allowing data to be read as 1 or 2 bytes) as are the control pins for the ZN433 (allowing data latching and serial data manipulation).

The ZN433 can be driven from either an external or on-board clock.

The analogue input and power supplies enter via a 9-way D-type connector.

## HOW THE ZN433 WORKS

The chip basically comprises a 2-5V reference, a reference amplifier, a D-A converter, an UP/DOWN counter controlled by a window comparator, and a data latch/shift register (see Fig.4).

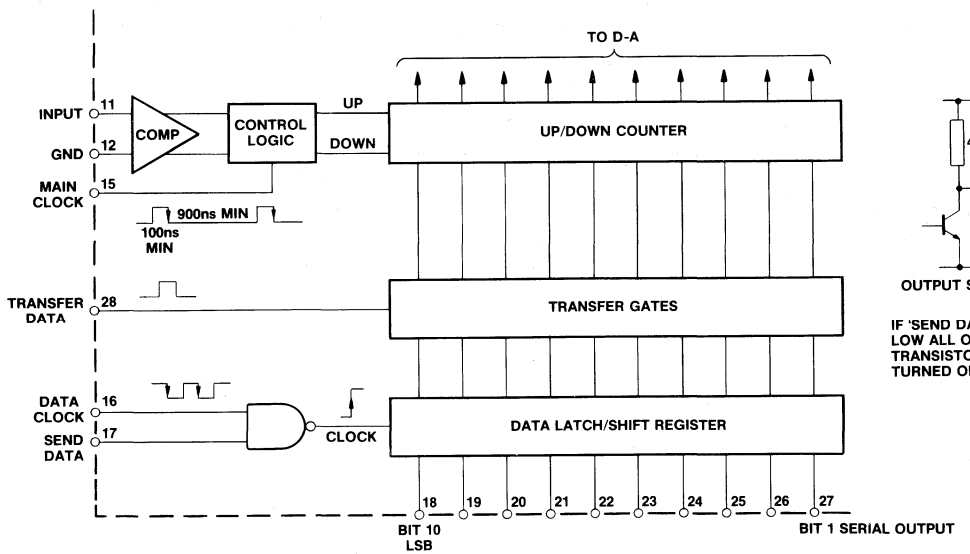



**Fig.4 System diagram of ZN433**

At the heart of the device is the current source array (CSA) D-A converter (see Fig.5). The unit current in each source is controlled by the output of the reference amplifier (approximately 1.7V). If the logic input is higher than $V_{bias}$ the current is switched to the 0V line, if not, the current is switched to the current summing line.

The bits are weighted by their number of current sources. Bit 1 has 16 current sources, bit 2 has 8, bit 5 has 1. Bits 6-10 current sources have a divide by 16 current divider. Bit 6 has 8 sources, bit 9 has 1. Bit 10 also has 1 but at half the unit current by using twice the resistor value for the emitter resistor. (This enables overall reduction in chip size due to the use of smaller resistors). Hence all the bits have correct weighting. The current sources for the different bits are interleaved to reduce any errors due to temperature gradients and process variations etc.

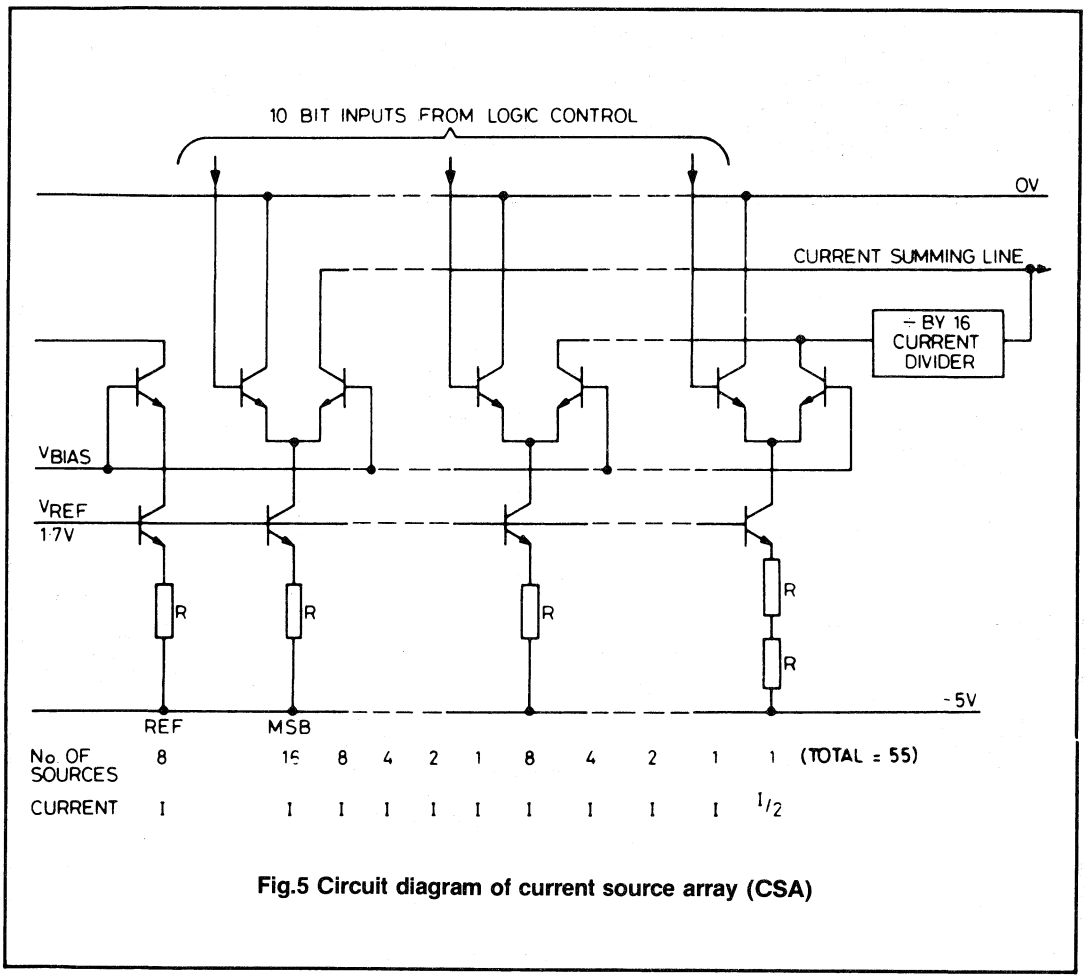



**Fig.5 Circuit diagram of current source array (CSA)**

There are 8 reference current sources distributed along the array. The reference amplifier controls these and also all the current sources for the bits.

The logic to control the current switching comes from the counter. The counter is instructed to COUNT UP, COUNT DOWN or HOLD by the window comparator. The 'window' is 1LSB wide.

If the input is within ± ½LSB of the digital outputs then the comparator output will instruct the counter to HOLD the count. This means the output will not hunt or exhibit hysteresis. If the input is not within ± ½LSB then the counter will count UP or DOWN as dictated by the comparator.

The counter outputs are connected to the data latch/shift register via transfer gates which are controlled by the transfer data pin (pin 28). If pin 28 is held permantely high then the counter outputs will appear directly at the bit outputs. Data can be latched by taking transfer data high (150nS min.) after the main clock negative going edge and low again before the next main clock negative going edge (50nS min. pulse width).

Data is latched on the negative going edge of the transfer data pulse. Once the data is latched it can be read out serially, from the MSB pin, by applying a data clock to pin 16 (1MHz max., min. pulse width 100nS). Also the outputs can be turned off at any time by applying a low to send data (pin 17). This means that the outputs of a few ZN433's can be wireAND-ed and each device selected individually for reading. However this may cause the $V_{OL}$ of the selected device to exceed the normal TTL low level due to the extra sink current from the additional pull-up resistor(s) on the other device(s). If this presents a problem then the outputs can be connected to logic with a higher input threshold e.g. CMOS.

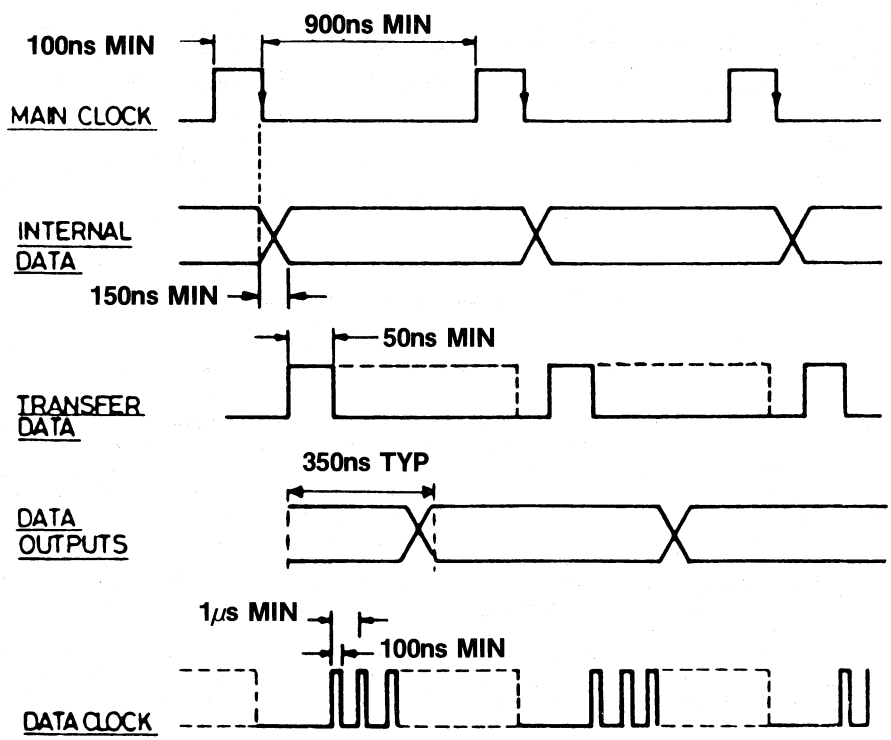



**Fig.6 Timing diagram**

## EXTERNAL COMPONENT CONNECTIONS

Basically the only external components required for the ZN433 to function are two 1 microfarad capacitors and 6 resistors (or less). The basic connections are as shown in Fig.7.

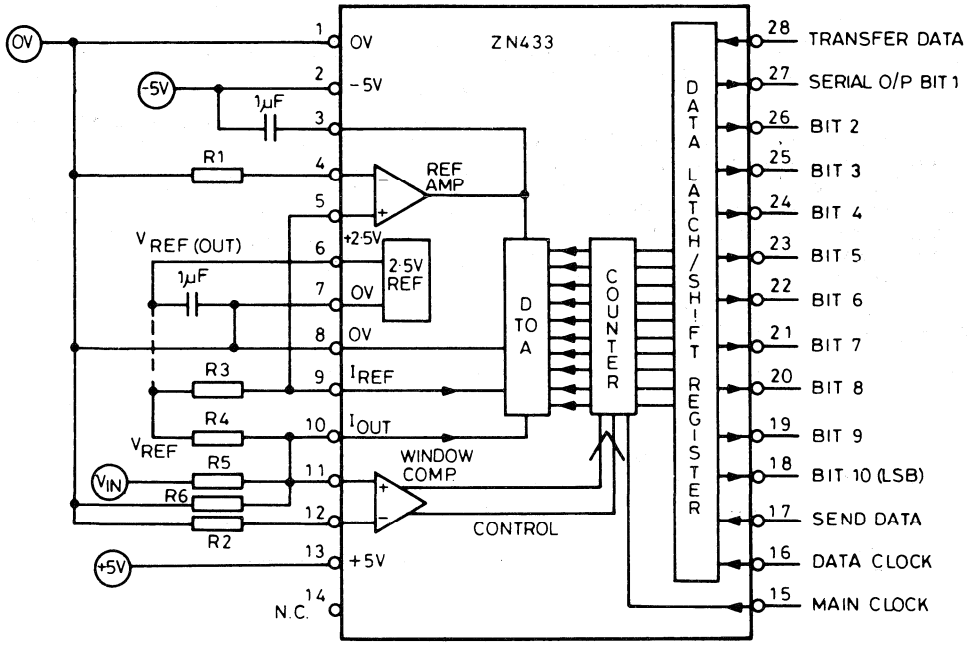



**Fig.7 Basic component connections**

R1 and R2 tie the inverting inputs of the reference amplifier and the window comparator to ground. The resistance seen by the non-inverting inputs should be equal to that seen by the inverting inputs for low offset and good temperature performance.

R3 sets the reference current which should be 1mA. R4 is only needed when using a bipolar input voltage and is chosen to offset $I_{out}$ as required. R5 is chosen to give a full-scale current of 4mA or if a bipolar voltage is used, a current swing of 4mA. R6 is chosen such that the resistance seen at the non-inverting input of the window comparator is the same as that seen at the inverting input. If a different reference voltage is used and hence a different R3, R1 should still be chosen to be equal to R3. R2 will always be 625ohms.

Resistors R3, R4 and R5 can affect offset and gain and thus require to be of high quality.

The two 1 microfarad capacitors are connected to stabilise the voltage reference and the output of the voltage reference amplifier.

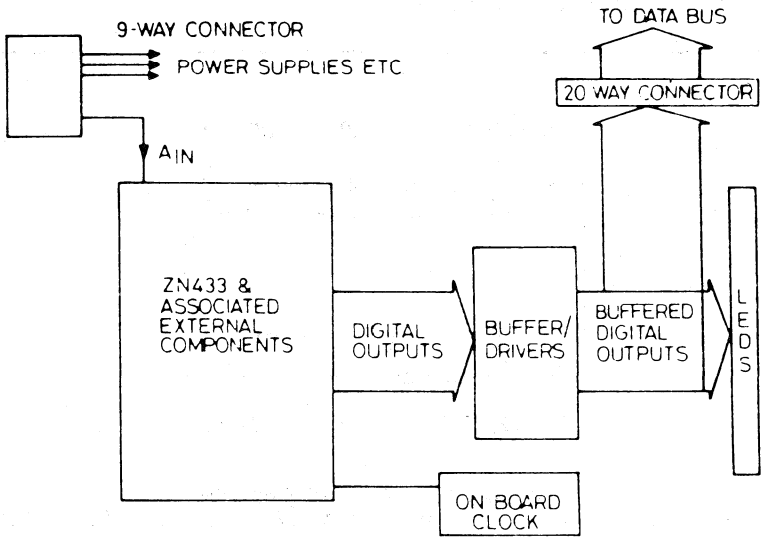



**Fig.8 Schematic diagram of evaluation board**

The board basically consists of the ZN433 and associated components, an optional on board clock and buffer/drivers to drive either LED's or data bus lines. Inverting buffers are used to drive the LED's and non-inverting buffers are used to drive the bus lines via the 20-way connector. The supplies enter via the 9-way D-type connector.

The outputs from the buffers connect to both the LED's (via resistors) and the 20-way connector. If the LED's are not required they can be omitted and likewise if it is not required to connect to a bus, the 20-way connector can be omitted.

The supply tracks on the board have been made as large as possible in order to minimise any errors due to voltage drops.

The outputs of the ZN433 go to two 16 pin I.C. sockets. In these sockets can be placed either two 16 lead non-inverting buffer/drivers or two 14 lead inverting buffers. At first it may seem odd putting a 14 lead device in a 16 pin socket. The reason is that the 16 pin devices have two pins for controlling the tristate outputs. These are used for connections to a bus.

Obviously these 2 extra control pins are not required when driving LED's hence the use of 14 lead devices. The pin assignments for the two different devices are shown in Figs. 9 and 10.

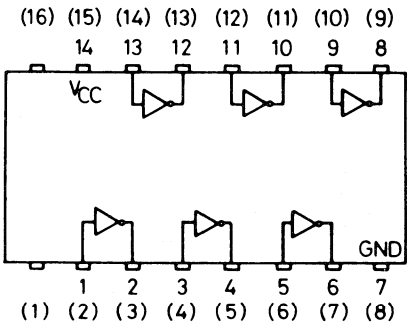



**Fig.9 Pinning for 7404, 7405 or 7406**
**(The numbers in brackets represent the corresponding socket pin numbers)**

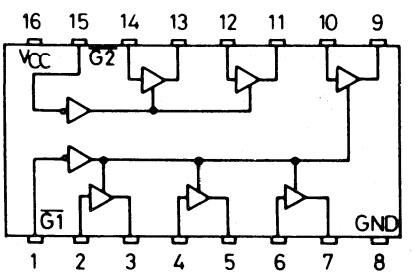



**Fig.10 Pinning for 74367**

It can be seen that the 14 lead device can be placed in the 16 pin socket as shown and the inputs and outputs of the buffers will be the same for both devices. When the 14 pin device is used the socket pins 15 and 16 must be linked to provide its $V_{CC}$. As previously stated the outputs go to both the 20-way connector and to the LED's via resistors. By applying the appropriate control waveforms to pins 1 and 15 of the 74367 tristate buffers when certain outputs are connected together, data can be read in two successive bytes on an 8-bit bus.

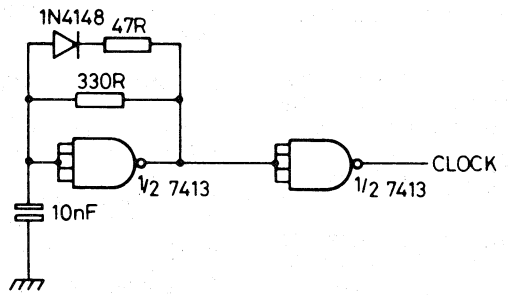



**Fig.11 On-board clock generator**

The main clock can be generated on board using a TTL dual Schmitt trigger circuit as shown in Fig.11. With the component values given in Fig. 11 the frequency is approximately 0.5MHz and the waveform as shown in Fig.12.

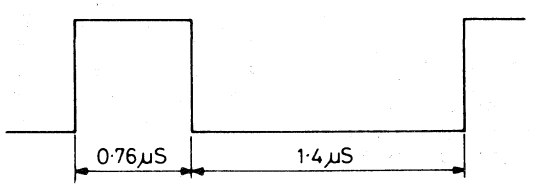



**Fig.12 On-board clock waveform**

On the negative going edge of the clock the counter is instructed to count UP, DOWN or HOLD. The counter drives the D-A which needs 900ns to settle to the 10-bit accuracy required.

The window comparator compares the D-A output with the Analogue input. The positive going edge of the clock then latches the comparator outputs which subsequently set the counter. The clock must stay high for a minimum of 100ns.

Providing the clock low period is at least 900ns and the high period at least 100ns as stated, the duty cycle doesn't matter. This means that below about 550kHz the clock can be symmetrical because the low period will always be at least 900ns.

If the on-board clock is not required, the clock components can be omitted and the ZN433 can be driven from an external clock. This can enter via the 20-way Speedbloc connector or can enter the board just below the LED's. Here a round BNC connector can either be secured to the board digital ground track directly or be mounted on a bracket which connects to the digital ground track. Connection can then be made to the clock line. Alternatively, the clock input can be soldered to terminal pins at these points.

The maximum analogue input frequency that the ZN433 can track accurately is related to the clock frequency and also the input signal amplitude. The outputs can only change 1 LSB at a time and so the input signal must not change by more than 1 LSB/clock period.

At its maximum rate of change, the ZN433 would take $2^{10}$ or 1024 clock cycles for its outputs to ramp up from zero (or -full-scale) to +full-scale. Likewise 1024 clock cycles would be needed to ramp back down. Thus 2048 clock cycles are needed for a full-scale change from zero (or -f.s.) to +f.s. and back again. This corresponds to one cycle of a full-scale triangular wave. With a 1MHz clock applied, the ZN433 can accurately track an input signal which changes less than 1 LSB/$\mu$s. This means that it can track a full-scale triangular wave input up to a frequency of

$$\frac{1}{2048\mu s} = 488\text{Hz}$$

The maximum full-scale sinewave frequency is about 311Hz - due to the fact that the rate of change is not constant but is greatest around zero, hence the maximum slew rate is encountered here.

The maximum frequency that can be tracked is increased when the input signal amplitude is reduced e.g. a half full-scale sinewave input can be tracked up to a frequency of 622Hz etc. However this does mean that resolution is effectively reduced.

The complete circuit diagram for the circuit board is shown in Fig.13. The resistor numbers are the same as used in the diagram on page 2 of the data sheet, where applicable. Resistors R3A and R3B make up the resistor R3 in the data sheet. R3A allows the gain to be adjusted. R4A, R4B and R4C make up resistor R4 in the data sheet and R4B allows the zero offset to be adjusted. R4C is only used when R4 is supposed to be infinite but offset is still required. Otherwise R4A is used with R4B to provide the adjustment, R4C being omitted.

## BOARD USED WITH LED DISPLAYS

Primarily to give a visual indication of the state of the outputs during device evaluation. In this configuration the 14 lead inverters are used with pin 1 of the device in pin 2 of the socket etc. Pin 16 of the socket has to be linked to pin 15 of the socket to supply $V_{CC}$ to the inverters.

For parallel output data, transfer data (pin 28), data clock (pin 16) and send data (pin 17) must all be taken high through links (J4, J5 and J6). If serial output data is required then these pins are used to control the latching and movement of the data (see data sheet). They can be accessed via the 20-way connector.

If serial data is not required, this connector can be omitted.

## BOARD USED FOR CONNECTION TO A BUS SYSTEM

The 20-way connector allows the ZN433 outputs to be latched and subsequently read via three-state outputs. Hence the 16 lead non-inverting buffers are used (74367's). The LED's and their resistors need not be connected. However (if they are connected, the LED's will be off when the buffer outputs are high or are in the high impedance state!

The outputs of the buffers connect directly to the 20-way connector and so do their control pins to enable them to be turned off as required. Also connected to the 20-way connector are: the ZN433 clock, the transfer data and data clock to allow manipulation of serial data, the send data to turn off all the outputs thus sending them high.

The bit outputs are arranged so that if pin 1, IC2 is linked to pin 1, IC3 (with J12) then bits 3 to 8 will be under the control of this common connection. These $\overline{\text{ENABLE}}$ pins correspond to 10b and 6b on the 20-way connector. Bits 1 and 2 are controlled by pin 15, IC2 (10a) and bits 9 and 10 are controlled by pin 15, IC3 (5b). The outputs are enabled when the $\overline{\text{ENABLE}}$ pins are taken low and are in the high impedance state when the $\overline{\text{ENABLE}}$ pins are taken high.

This arrangement allows the outputs to be read as two words with either bits 1 to 8 and bits 9 and 10 or bits 1 and 2 and bits 3 to 10 as the two words. This is illustrated in Table 1. Also, as can be seen in Table 1, all the outputs can be disabled or enabled at the same time.

| 20-way connector pins | | | Outputs selected |
|---|---|---|---|
| 10a | 5b | 10b and 6b linked | |
| L | L | L | All bits |
| L | H | L | Bits 1 to 8 |
| H | L | H | Bits 9 and 10 |
| L | H | H | Bits 1 and 2 |
| H | L | L | Bits 3 to 10 |
| H | H | H | No bits |

**Table 1**

## BOARD USED WITH EXTERNAL CLOCK

Here the on board clock components can be omitted. Using an external clock enables the ZN433 to be run at any desired frequency within its range. This would be useful if it is wished to synchronise the ZN433 with some other system.

The use of an external clock would probably give better results than the on board clock because the latter tends to generate a lot of noise.

## OFFSET AND GAIN SETTING PROCEDURE

The offset and gain are adjusted by R4B and R3A respectively. These are placed near the edge of the board for easy adjustment. The value of the fixed and variable resistor in each case is such that together their values can be adjusted to around the value stated in the data sheet i.e. R3A + R3B = R3, R4A + R4B = R4 (remember R4C is only used when R4 = $\infty$). The value of the variable resistors is dependant on how fine the adjustment is required to be, but the combination must be chosen to allow sufficient adjustment. The resistors must be of high stability.

**Unipolar operation**

R4B is used to adjust the zero, it should be adjusted so that for an input of ½LSB, the LSB just flickers between '0' and '1' with all the other bits at '0'. R3A is used to adjust the gain. This should be adjusted so that for an input of full-scale − 1½LSB, the LSB just flickers between '0' and '1' with all the other bits at '1'.

The setting of one control may affect the other so the above procedure should be repeated until both settings are satisfactory.

**Bipolar operation**

Again R4B adjusts the offset but this time the input is − (full-scale − ½LSB). Again the LSB is required to flicker between '0' and '1' with all the other bits at '0'.

R3A adjusts the gain as above. For an input of full-scale − 1½LSB, R3A is adjusted until the LSB just flickers between '0' and '1' with all the other bits at '1', as for unipolar operation.

The procedure should again be repeated until both settings are satisfactory.

## 9-WAY CONNECTOR

Pins 2 and 7 are not connected. The wipers of R3A and R4B connect to the voltage reference which is brought out to pin 1. This allows an external reference to be used. The external reference and the internal reference share the same decoupling point on the analogue ground - as they will not both need it at the same time. A capacitor decoupling the external reference can thus be positioned 90° anti clockwise to C5 (the internal reference decoupling capacitor). The internal reference (pin 6) on the ZN433, can be connected to the wipers of R3A and R4B via a link (J2).

The analogue input enters via pin 6. The analogue and digital grounds connect to pins 4 and 8 respectively, and may either be connected together near the chip (using J3) or brought out separately depending on which will give the best results for a particular application.

The − 5V and + 5V supplies connect to pins 3 and 5 respectively and the + 5V auxiliary supply is connected to pin 9. If desired this auxiliary supply can be linked to the + 5V supply (with J1) and used for example to power an external transducer.

Note: The above pin connections apply when the 9-way PCB connector is a socket and will be different if a plug is used.

## USING THE BOARD WITH DIFFERENT INPUT VOLTAGE RANGES

Whatever maximum analogue input voltage is used $I_{ref}$ should always be about 1mA and $I_{out}$ full-scale should always be about 4mA. Thus in order to accommodate different input voltage ranges and different reference voltages, the resistors associated with these currents must be changed. How these resistors are calculated and a table of calculated values, for various input voltages, are given in the data sheet.

**BOARD LINKS**

**Optional:**

| | | |
|---|---|---|
| J1 | – | Links the board +5V to the auxiliary +5V on the 9-way connector to provide a +5V auxiliary output. |
| J2 | – | Applies the internal reference to the ZN433 and thus configures the board for operation with the on chip 2.5V reference. |
| J3 | – | Connects the analogue and digital grounds together near the ZN433 - may be desirable in some applications. |
| J4 | – | Ties transfer data (pin 28) high making the output data latch transparant. Used when the data does not need to be latched. |
| J5 and J6 | – | Tie send data and data clock high. Used when the outputs do not need to be turned off, and when serial output data is not required. |
| J9 and J13 | – | Connect +5V to the 14 lead inverters, if they are chosen to drive the LED's. |
| J12 | – | Links 6b and 10b (on the 20-way connector) together to allow either pin to control bits 3 to 8. |
| J14 | – | Links on board clock output to ZN433 clock input, when the on board clock is required. |

**Mandatory:**

| | | |
|---|---|---|
| J7 and J8 | – | Provide the ground connections for IC2 and IC3. |
| J10 | – | Links bit 2 output from IC2 to the 20-way connector and the relevant LED feed resistor. |
| J11 | – | Connects +5V to IC3 socket - pin 16. |

| | | | | | |
|---|---|---|---|---|---|
| **ICs** | | | **Capacitors** | | |
| IC1 | = | ZN433 | C1 | = | 100μF electrolytic - axial |
| IC2 | = | 7404 or 74367 | C2 | = | 100μF electrolytic - axial |
| IC3 | = | 7404 or 74367 | C3 | = | 0.1μF disc ceramic |
| IC4 | = | 7413 | C4 | = | 1μF tantalum bead |
| | | | C5 | = | 1μF tantalum bead |
| **Resistors** | | | C6 | = | 0.1μF disc ceramic |
| R1 | = | 2.4K | C7 | = | 0.1μF disc ceramic |
| R2 | = | 620R | C8 | = | 10nF ceramic |
| R3A | = | 1K 20 turn trimpot | C9 | = | 100μF tantalum bead |
| R3B | = | 1.8K | **Miscellaneous** | | |
| R4A | = | 100K | D1-D10 | = | LED's |
| R4B | = | 1M 20 turn trimpot | D11 | = | 1N4148 |
| R4C | = | 100K | IC2 socket | = | 16 pin DIL socket |
| R5 | = | 620R | IC3 socket | = | 16 pin DIL socket |
| R6 | = | ∞ | IC4 socket | = | 14 pin DIL socket |
| R7-R16 | = | 330R | **Connectors** | | |
| R17 | = | 330R | 9-way connector | = | D-type sub miniature |
| R18 | = | 47R | 20-way connector | = | Speedbloc system |
| | | | Round chassis mounting connector | = | BNC type |

Depending on input voltage range

**Table 2 Component list**

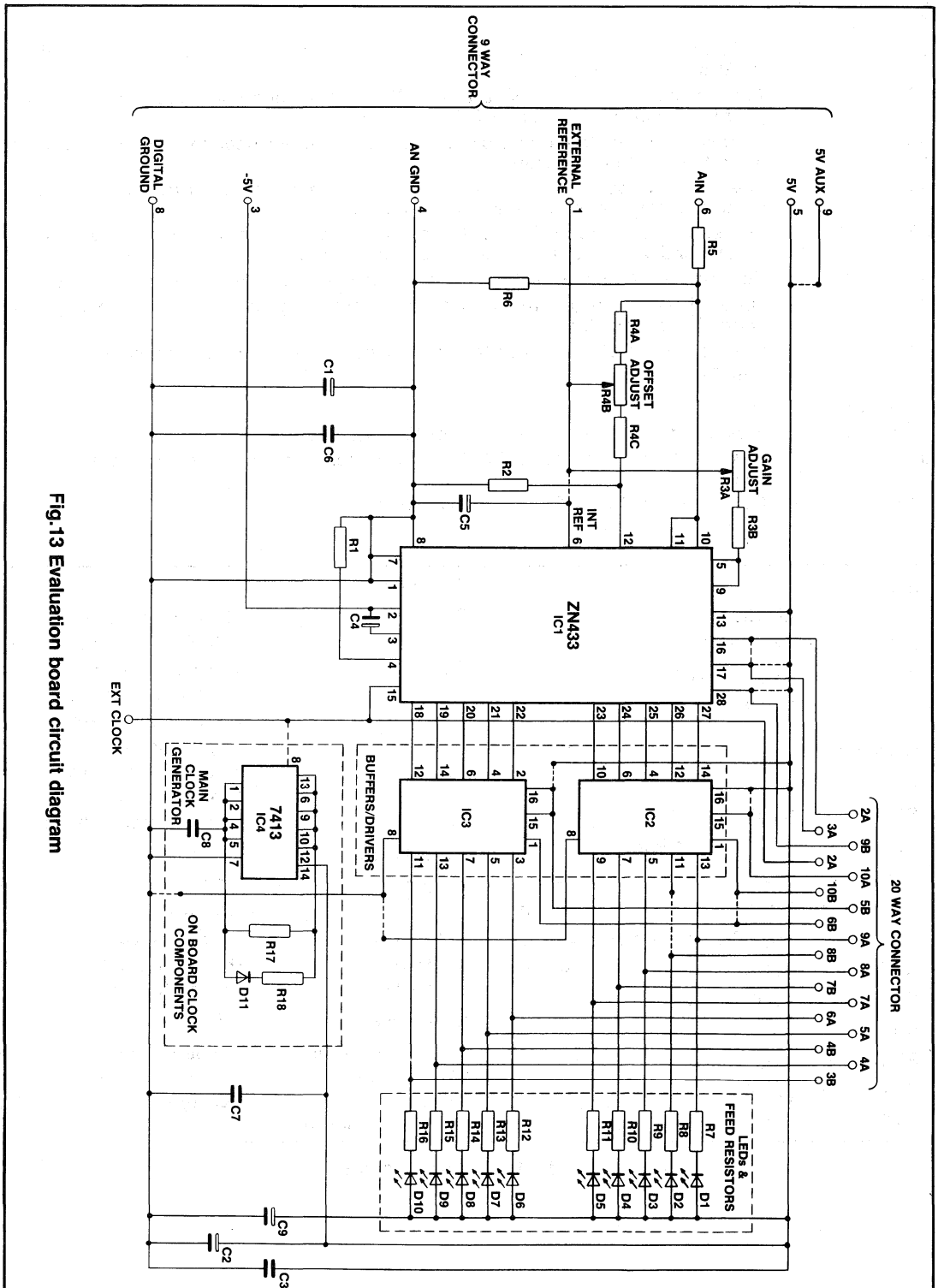



Fig.13 Evaluation board circuit diagram

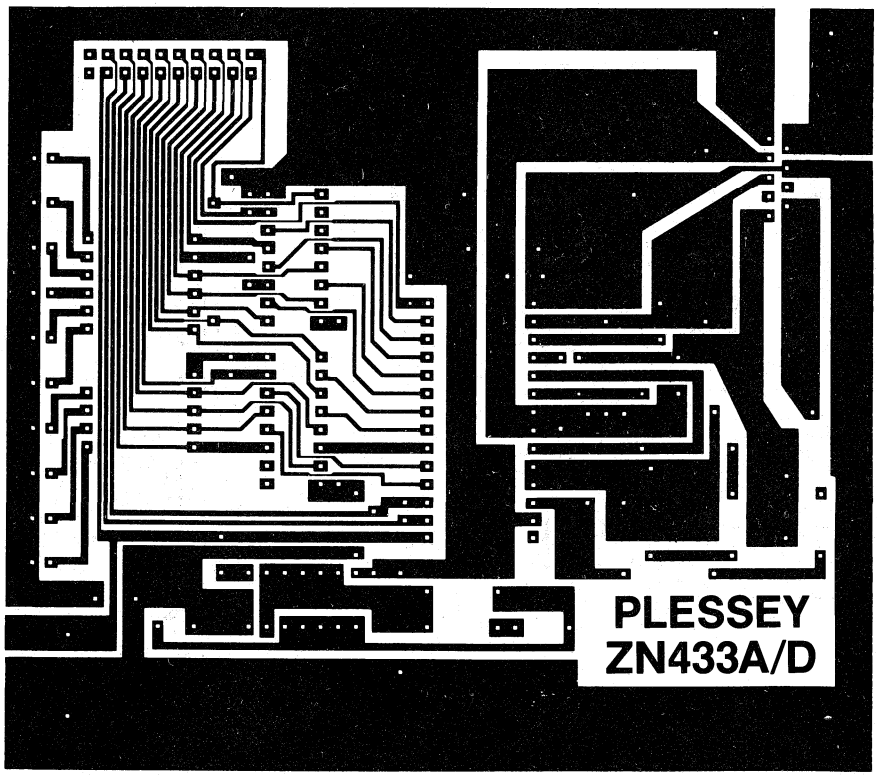



Fig.14 PCB copper side (1:1)

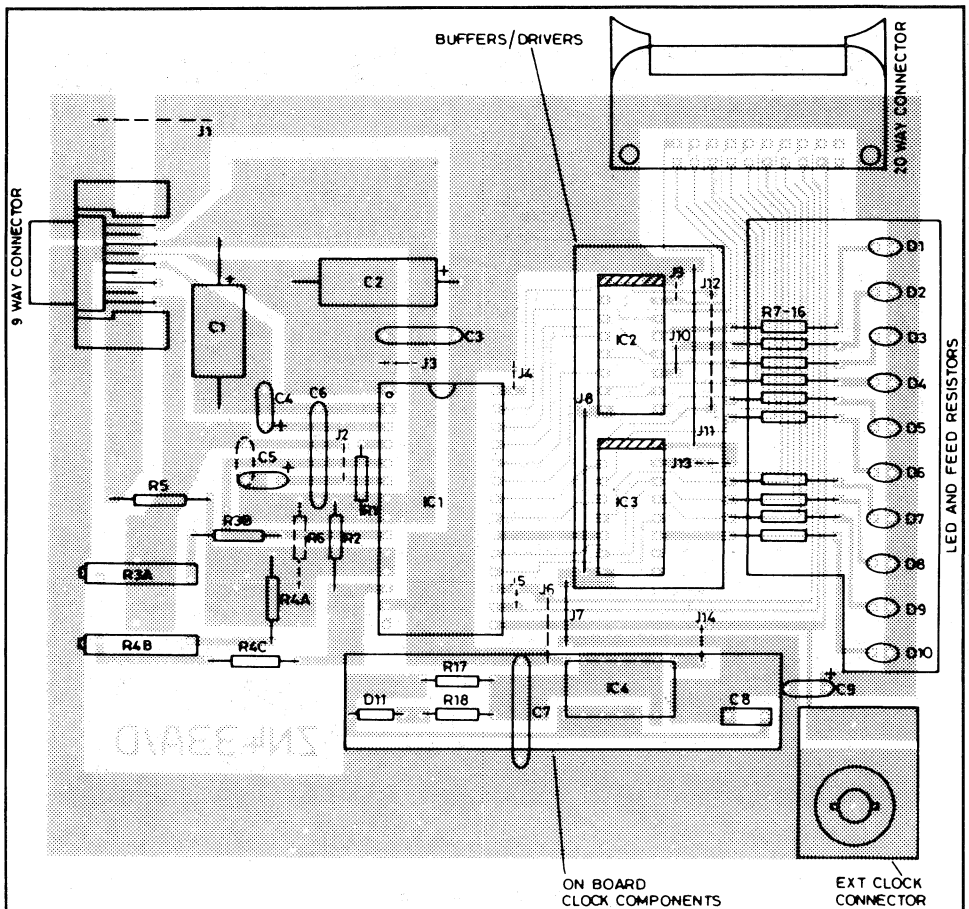



**Fig.15 Component layout - actual size**

**9-way D-type socket**

| | | |
|---|---|---|
| 1 | = | External reference |
| 2 | = | NC |
| 3 | = | −5V Supply |
| 4 | = | Analogue ground |
| 5 | = | +5V supply |
| 6 | = | $A_{IN}$ |
| 7 | = | NC |
| 8 | = | Digital ground |
| 9 | = | Auxiliary +5V |

**20-way, speedbloc plug**

| | | | | | |
|---|---|---|---|---|---|
| 1a | = | NC | 1b | = | NC |
| 2a | = | Main clock | 2b | = | Data clock |
| 3a | = | Send data | 3b | = | bit 10 |
| 4a | = | bit 9 | 4b | = | bit 8 |
| 5a | = | bit 7 | 5b | = | IC 3, output $\overline{\text{enable}}$ 2 |
| 6a | = | bit 6 | 6b | = | IC 3, output $\overline{\text{enable}}$ 1 |
| 7a | = | bit 5 | 7b | = | bit 4 |
| 8a | = | bit 3 | 8b | = | bit 2 |
| 9a | = | bit 1 | 9b | = | Transfer $\overline{\text{data}}$ |
| 10a | = | IC 2, output $\overline{\text{enable}}$ 2 | 10b | = | IC 2, output $\overline{\text{enable}}$ 1 |

**Table 3 Pin assignment for connectors**

# Interfacing the ZN439 with the 6500 Family of Microprocessors

**The object of this report is to present the techniques involved in interfacing the ZN439 to the 6500 family of microprocessors. The circuit designs were all proven on a 6502 development system but apply equally to all the other microprocessors in the family. Direct bus and port interfacing will be considered for single and multiple converter applications. In both cases polling and interrupt driven examples will be given, highlighting the features which make the ZN439 ideally suited to interfacing to todays microprocessors. Circuit diagrams, as well as flow diagrams and sample programs will be included to give the system designer a full appreciation of what is required.**

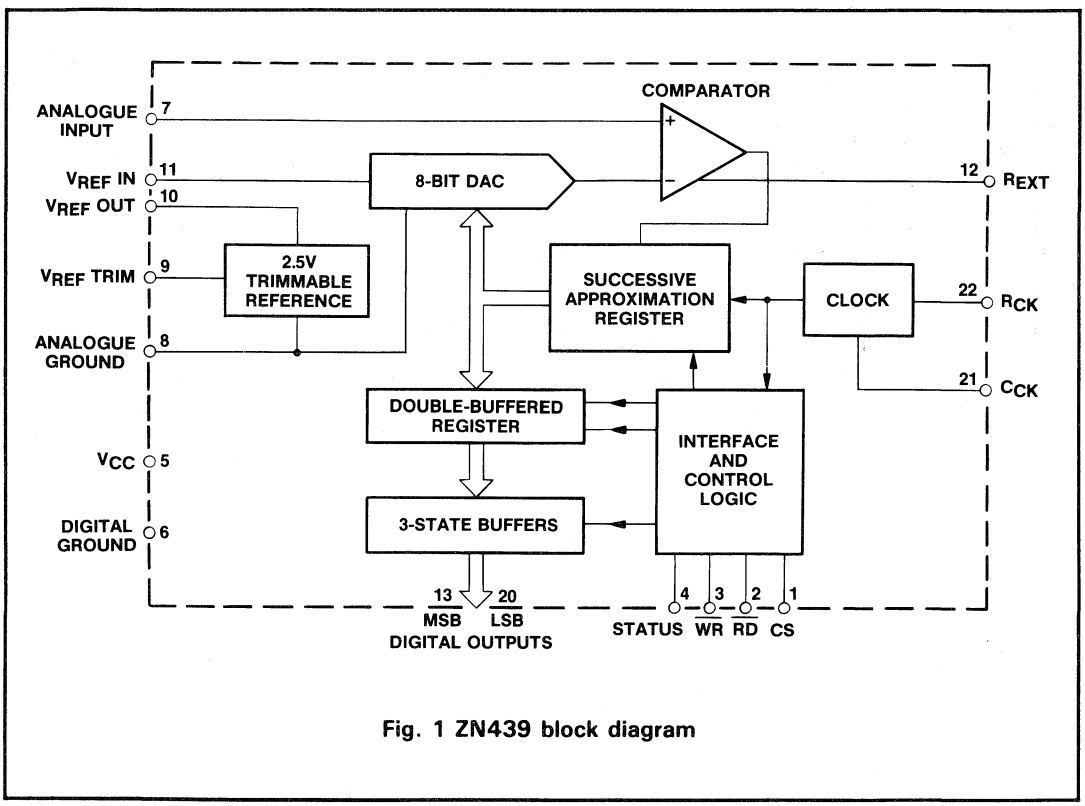



Fig. 1 ZN439 block diagram

## THE ZN439 A-D CONVERTER

The ZN439 is an 8-bit successive approximation converter which has been designed to allow simple interfacing to microprocessors. All active circuitry is contained on-chip including clock generator, trimmable 2.5V bandgap reference, control logic and a double buffered register with three-state outputs. The main feature of this device is the use of a double buffered register which allows the outputs to be read at any time irrespective of the conversion status. A block diagram of the device is shown in Fig. 1.

## CIRCUIT DESCRIPTION

The ZN439 utilises the successive approximation technique to produce an 8-bit digital output. Upon receipt of a negative going pulse on the $\overline{WR}$ input the status output and the MSB input to the DAC go high while the remaining DAC inputs are taken low. The resulting analogue output from the DAC is compared with the unknown analogue input signal by the comparator. If the input signal is larger, the MSB remains high and if not it is taken low. On the second clock pulse this sequence is repeated for the next most significant bit. This process is continued until all the 8 bits have been compared. On the 8th negative clock edge, status goes low to indicate the end of conversion and providing the $\overline{RD}$ input is high the double buffered register is updated with the new data. For this reason the $\overline{RD}$ input cannot be tied low as this would prevent the double buffered register from being updated. The status output will remain low until either:

a) Another start convert pulse is applied to the $\overline{WR}$ input.

b) The data is read from the converter by applying a read pulse to the $\overline{RD}$ input.

The resetting of the status output by the application of a read pulse makes the device ideally suited to interrupt operation. At the end of a conversion the status output goes low which causes an interrupt within the system. The interrupt service routine will involve reading data from the converter which will take the status output back high and thus remove the interrupt.

The device can also be made to continuously convert by tying the $\overline{CS}$ and $\overline{WR}$ inputs low. In this mode after a conversion is complete the status output goes low and remains low for one clock cycle. Another conversion is then automatically initiated and the status output is taken high. As with the interrupt mode of operation the status output will be taken high prematurely if a read pulse is applied to the $\overline{RD}$ input.

Finally the $\overline{CS}$ input can be used for decoding purposes to enable the device. When the $\overline{CS}$ input is high any $\overline{RD}$ or $\overline{WR}$ signals are locked out and hence ignored by the converter control logic. Timing diagrams for the interrupt and continuous conversion modes of operation are shown in Fig. 2. For further information on this device refer to the ZN439 data sheet.

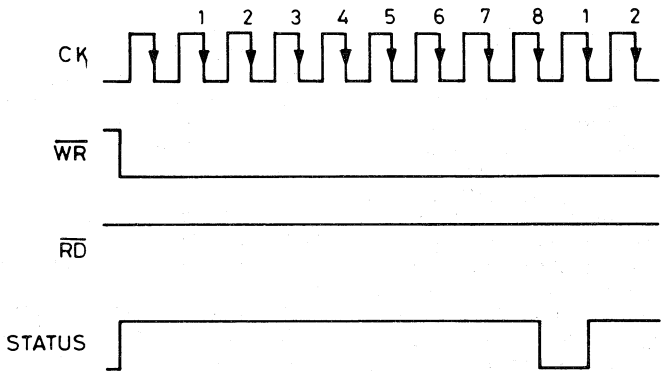



Fig. 2a Continuous conversion without read

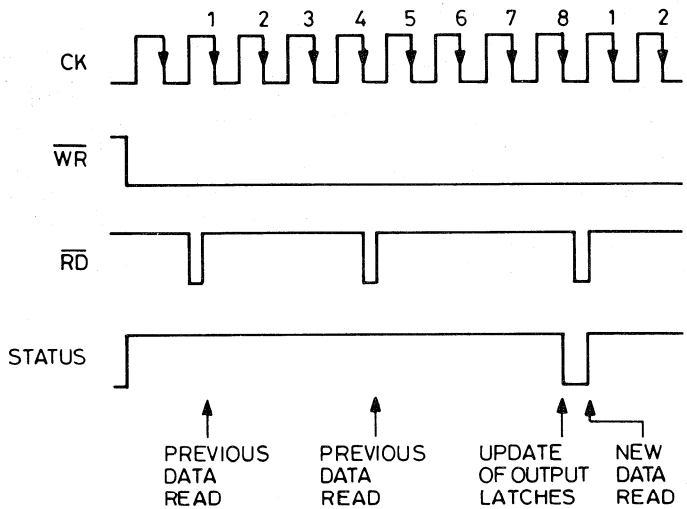



Fig. 2b Continuous conversion with read

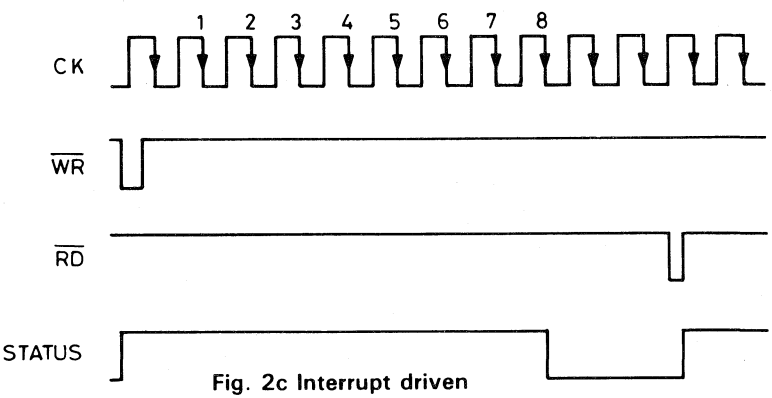



Fig. 2c Interrupt driven

Fig. 2 ZN439 timing diagrams

## DIRECT BUS INTERFACING

### The 6500 family of microprocessors

The 6500 family consists of 10 NMOS microprocessors. All are bus and software compatible and provide options of addressable memory, interrupt input, on-chip clock oscillators and drivers. There are three speed versions 1MHz, 2MHz and 3MHz which with pipeline architecture provides very fast instruction execution. The series has recently been increased by the introduction of three CMOS microprocessors available in four speed options 1MHz, 2MHz, 3MHz and 4MHz. Each has a 64K byte address range, an improved instruction set, lower power consumption, two hardware enhancements but are all bus and software compatible with the NMOS devices.

A full description of the architecture and instruction set of these microprocessors is beyond the scope of this report. It is therefore assumed that the designer will be familiar with these details. For further information please refer to the 6500 and 65C00 microprocessor data available from the manufacturers or their distributors.

### ROM type operation

The most important feature of the ZN439 is the ability to read valid data at any time independent of the conversion status. This makes the device ideally suited to ROM type operation. By using a minimal amount of address decoding the ZN439 can be located within the system memory map in the same manner as a ROM. The decoded enable line is connected to the $\overline{RD}$ input of the ZN439. Therefore whenever the microprocessor reads data from this address the $\overline{RD}$ input is taken low and the ZN439 places valid data onto the bus. The $\overline{WR}$ and $\overline{CS}$ lines are tied low so that the ZN439 cycles continuously. In this manner any data read is guaranteed to be at worst 5$\mu$s old, assuming a clock speed of 1.6MHz. A block diagram showing the connections required is given in Fig. 3.

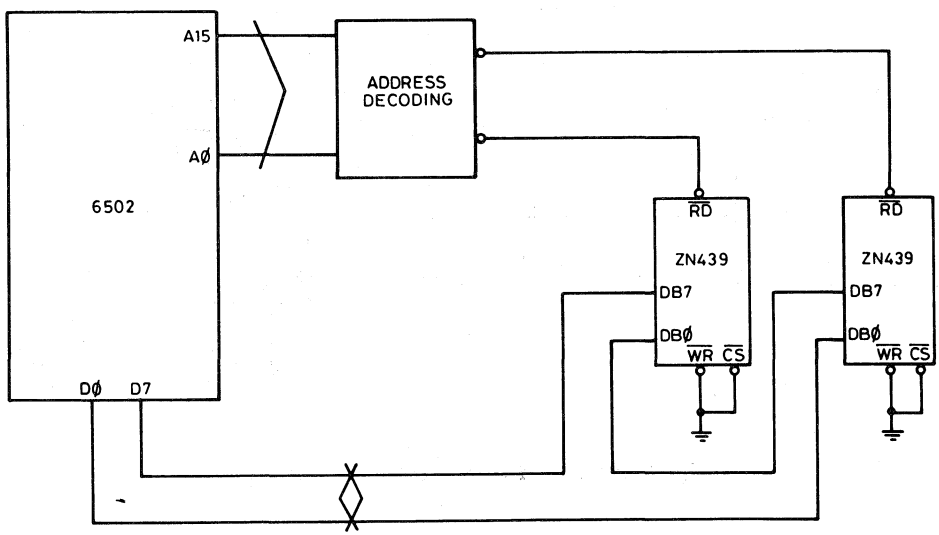



Fig. 3 Direct bus interfacing

**Interrupt driven operation**

If the data from the converter is to be read infrequently the designer may prefer the device to be interrupt driven. In this mode of operation a low going start convert pulse is applied to the $\overline{WR}$ input. At the end of conversion the high to low transition of the status output is used to generate an interrupt. This is done by buffering the status output with an open collector buffer whose output is connected to the microprocessor $\overline{IRQ}$ input. Data is read from the ZN439 during the interrupt service routine. The action of reading the data sets the status output back high and so removes the interrupt. A block diagram is shown in Fig. 4.

It should be noted that after power up the status output will go low thus pulling the $\overline{IRQ}$ line low. Therefore a 'dummy' ZN439 data read should be performed to set the status line high and remove the interrupt. This will prevent erroneous data being read once the microprocessor has enabled interrupts after power up.

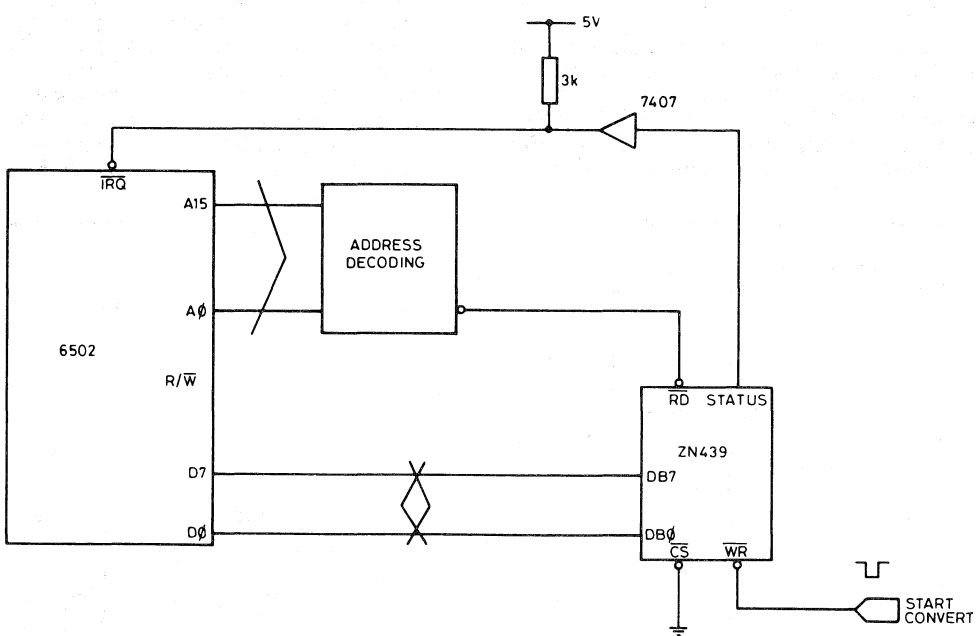



**Fig. 4 Interrupt driven direct bus interfacing**

Another interrupt driven application would be operating the device in its continuous conversion mode with a slow clock (e.g. 1KHz). This method could be employed when monitoring a slowly varying analogue voltage. Providing the input voltage did not change by more than 1LSB during a conversion cycle the digital result will be 8 bit accurate. The microprocessor interrupt would be generated using the status buffering already described. In this mode the status and hence the $\overline{IRQ}$ line would remain low for 1 clock cycle. Care must therefore be taken to ensure that the microprocessor can respond to the interrupt within this time. If the microprocessor doesn't respond within 1 ZN439 clock cycle then the interrupt will be missed. This will only usually be a problem in multi-interrupt systems. In such a system the ZN439 interrupt may be ignored by the microprocessor until it has finished servicing another interrupting device. Therefore the other interrupt service routine must not be longer than 1 ZN439 clock cycle.

**Multi-interrupt systems**

In some systems more than one device may be capable of generating an interrupt. In these multi-interrupt systems some form of polling will be required to determine the origin of the interrupt. This means that each interrupting device must provide some form of flag to indicate to the microporcessor that it has requested the interrupt. The easiest way of providing this with the ZN439 is by using the status output as an interrupt flag. This can be implemented by connecting the status output via a three-state buffer onto bit 0 of the data bus. The enable line of the three-state buffer is derived from the address decoding in the same manner as the $\overline{RD}$ input of the ZN439. Therefore by reading the data from this address and testing bit 0 the microprocessor can determine whether the ZN439 is responsible for the interrupt.

An example of this is given below where two ZN439's occupy successive addresses in the memory map. Each have separate asynchronous start convert ($\overline{WR}$) inputs. The status output of the first is connected to bit 0 and the second to bit 1 of the data bus in the manner described above. By reading the data from the flag address and examining bits 0 and 1, the microprocessor is able to determine which converter has generated the interrupt. A circuit diagram is shown in Fig. 5. A typical interrupt flow diagram and program are given in Fig. 6 and Fig. 7 respectively.

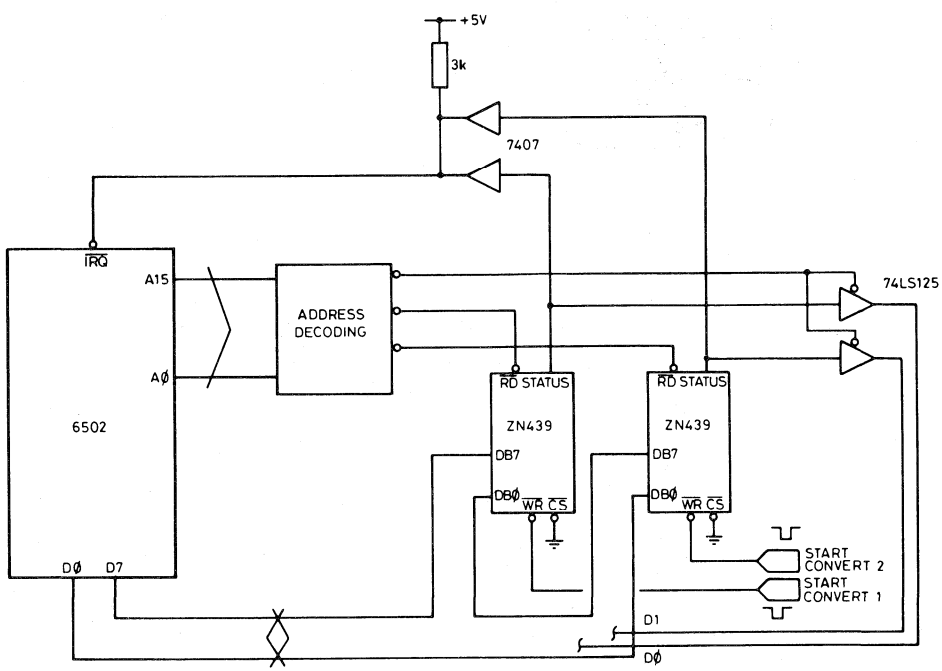



Fig. 5 Multi-interrupt direct bus interfacing

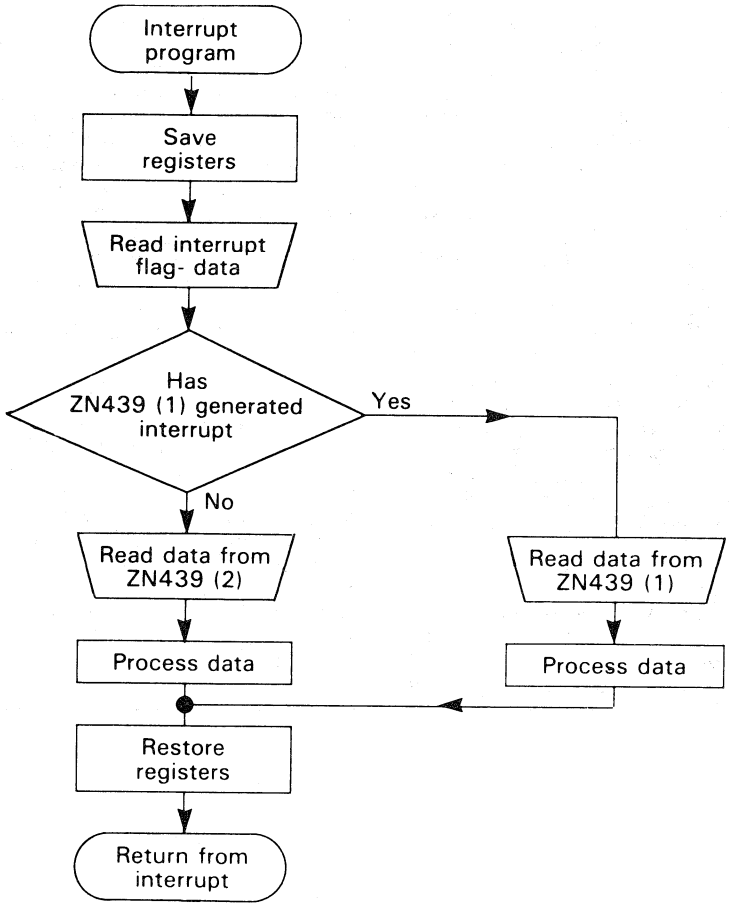

Interrupt program
Save registers
Read interrupt flag- data
Has ZN439 (1) generated interrupt
Yes
No
Read data from ZN439 (2)
Read data from ZN439 (1)
Process data
Process data
Restore registers
Return from interrupt

Fig. 6

| Address | Object code | Label | Mnemonic | Operand | Comments |
|---|---|---|---|---|---|
| 2000 | 48 | | PHA | | |
| 2001 | 8A | | TXA | | |
| 2002 | 48 | | PHA | | Save registers |
| 2003 | 98 | | TYA | | |
| 2004 | 48 | | PHA | | |
| 2005 | AD 00 12 | | LDA | 1002 | Read flag data |
| 2008 | 4A | | LSR | A | Has ZN439(1) gene- |
| 2009 | B0 08 | | BCS | AD2 | rated the interrupt |
| 200B | AD 00 10 | | LDA | 1000 | Read ZN439(1) data |
| 200E | 85 80 | | STA | 80 | Process data |
| 2010 | 4C 18 20 | | JMP | END | |
| 2013 | AD 00 11 | AD2 | LDA | 1001 | Read ZN439(2) data |
| 2016 | 85 81 | | STA | 81 | Process data |
| 2018 | 68 | END | PLA | | |
| 2019 | A8 | | TAY | | |
| 201A | 68 | | PLA | | Restore registers |
| 201B | AA | | TAX | | |
| 201C | 68 | | PLA | | |
| 201D | 40 | | RTI | | Return |

**ADDRESS ALLOCATION**

80 Memory location for storing ZN439(1) data.
81 Memory location for storing ZN439(2) data.
1000 ZN439(1).
1001 ZN439(2).
1002 Interrupt flags.
2000 Start address of program.

Note: All numbers are in Hex.

**Fig. 7**

**Interfacing to the 4MHz CMOS 65C00 series**

The high speed 4MHz 65C00 series have a maximum access time of 160nS. This access time must include both delay time through the address decoding and the enable time of the ZN439 data outputs. As the maximum enable time of the ZN439 is 160nS the device is too slow to interface directly to this microprocessor.

To overcome this problem the read cycle must be extended by use of the microprocessor RDY input. Fig. 8 shows a simple circuit using a JK flip-flop to stop the microprocesor for 1 clock period during a ZN439 read cycle. This is a standard procedure with high speed micro-processors. A timing diagram is shown in Fig. 9.

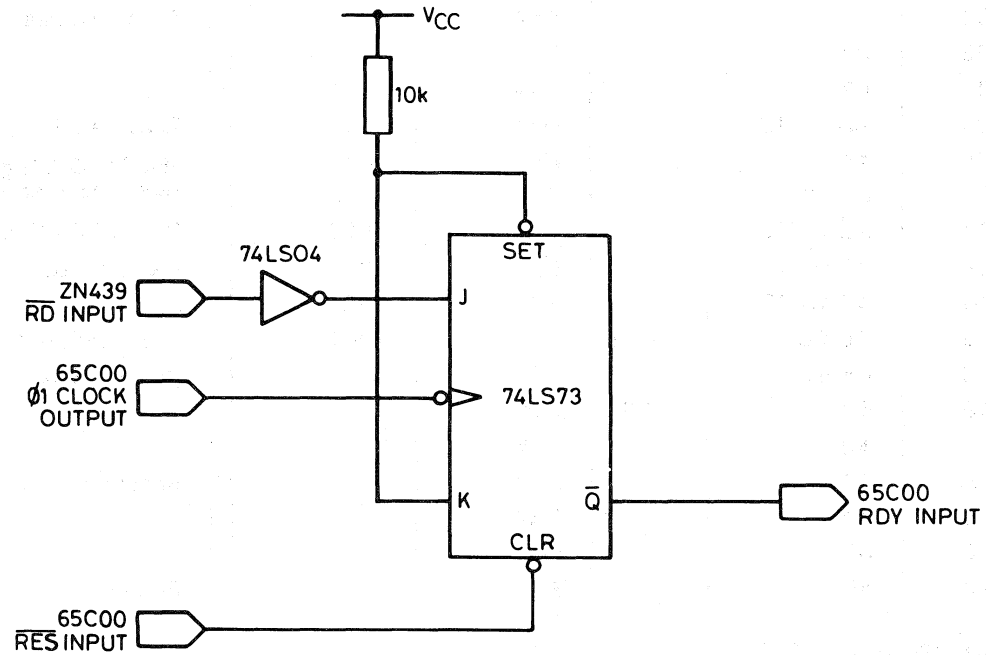



**Fig. 8 Read cycle extender circuit**

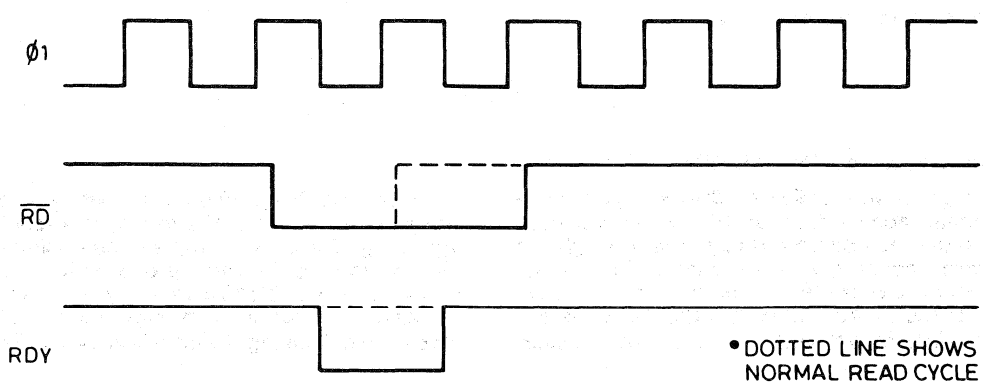



**Fig. 9 Timing diagram**

## PORT INTERFACING

In some cases it may be necessary to interface the converter to an existing microcomputer system. In these cases the address space may already have been fully allocated and so the only interfacing possible will be via the system ports. The following section gives hardware and software details of the different techniques available for interfacing the ZN439 to the popular peripheral interface chip the 6522 VIA.

All the program examples assume the 6522 is in its reset state.

### The 6522 versatile interface adaptor

The 6522 VIA is an NMOS I/O control device available in two speed options 1 and 2MHz. It contains two 8-bit bi-directional ports, each line of which can be programmed as either an input or an output. Associated with each port are two control lines. These lines can be programmed as either interrupt inputs or handshake outputs. In addition the device contains two 16-bit counter timers and a serial shift register. To facilitate control of the many features the VIA contains interrupt flag, interrupt enable, function control and auxiliary control registers.

To complement the CMOS microprocessors in the 6500 family the VIA is also available as a CMOS device the 65C22. This is available in four speed options 1, 2, 3 and 4MHz and is fully compatible with the NMOS device.

For further information please refer to the 6522 and 65C22 data sheets.

### Direct port interfacing

#### (1) Single converter

The simplest method of interfacing a single converter to the 6522 is shown in Fig. 10. The data outputs of the ZN439 are connected to the port A data lines which are configured as inputs. As the $\overline{RD}$ input cannot be tied low it must be taken low before reading the converter data and returned high afterwards. This is achieved using the port A control line, CA2 programmed as an output. To read the data CA2 is taken low. The data is then read from the port A input register. Finally CA2 is taken high, allowing the ZN439 double buffered register to be updated after the next conversion. As only one port is required this circuit is equally applicable to port B using PB0-7 and CB2 instead of PA0-7 and CA2. A flow diagram and program showing the required initialisation and data read steps are shown in Figs. 11 and 12 respectively.

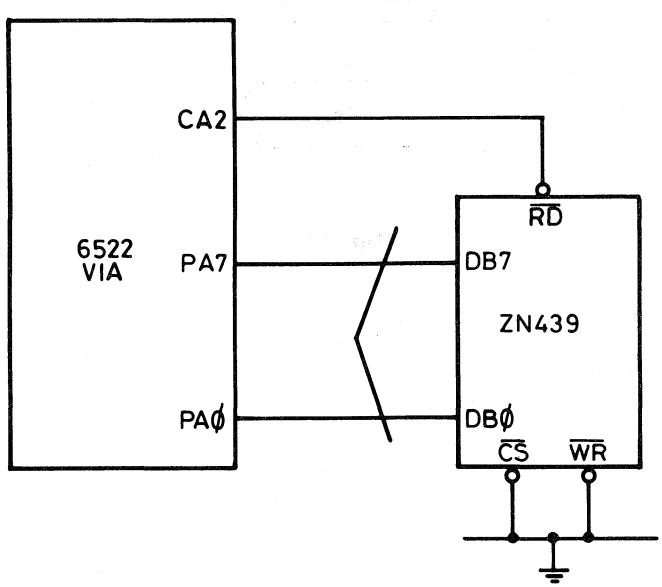



**Fig. 10 Single converter - direct port interfacing**

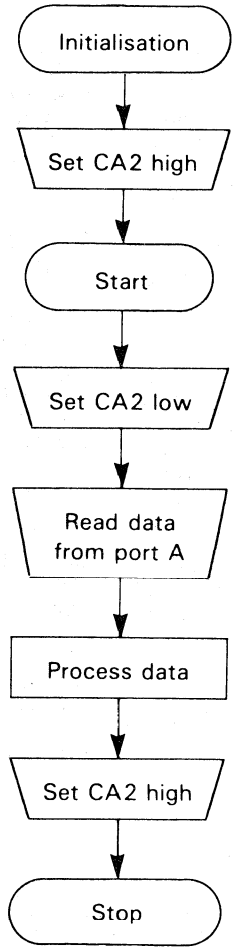

Initialisation
Set CA2 high
Start
Set CA2 low
Read data
from port A
Process data
Set CA2 high
Stop

**Fig. 11**

| Address | Object code | Label | Mnemonic | Operand | Comments |
|---|---|---|---|---|---|
| 2000 | AD OC 50 | | LDA | 500C | |
| 2003 | 29 F1 | | AND | #F1 | Sets CA2 high without affecting the other port control lines |
| 2005 | 09 OE | | ORA | #OE | |
| 2007 | 8D OC 50 | | STA | 500C | |
| 3000 | AD OC 50 | | LDA | 500C | |
| 3003 | 29 FD | | AND | #FD | Sets CA2 low |
| 3005 | 8D OC 50 | | STA | 500C | |
| 3008 | AD O1 50 | | LDA | 5001 | Read ZN439 data |
| 300B | 85 80 | | STA | 80 | Process data |
| 300D | AD OC 50 | | LDA | 500C | |
| 3010 | 09 02 | | ORA | #02 | Sets CA2 high |
| 3012 | 8D OC 50 | | STA | 500C | |

**ADDRESS ALLOCATION**

80 Memory address for storing ZN439 data.
2000 Start address of initialisation.
3000 Start address of ZN439 read program.
5001 VIA data register for port A.
500C VIA peripheral control register.

**Fig. 12**

**(2) Multiple converters**

For connecting more than one converter to a 6522 an extension of the single converter circuit is used. A circuit diagram is shown in Fig. 13. As before the port A inputs are connected to the data bit outputs of each converter. Port B is now used to provide the individual $\overline{RD}$ outputs to each converter. To read data from a ZN439 the appropriate bit output of port B is taken low. Data can then be read from the port A input register as before. Note, only one bit of port B should be taken low at a time. A flow diagram and program are shown in Figs. 14 and 15.

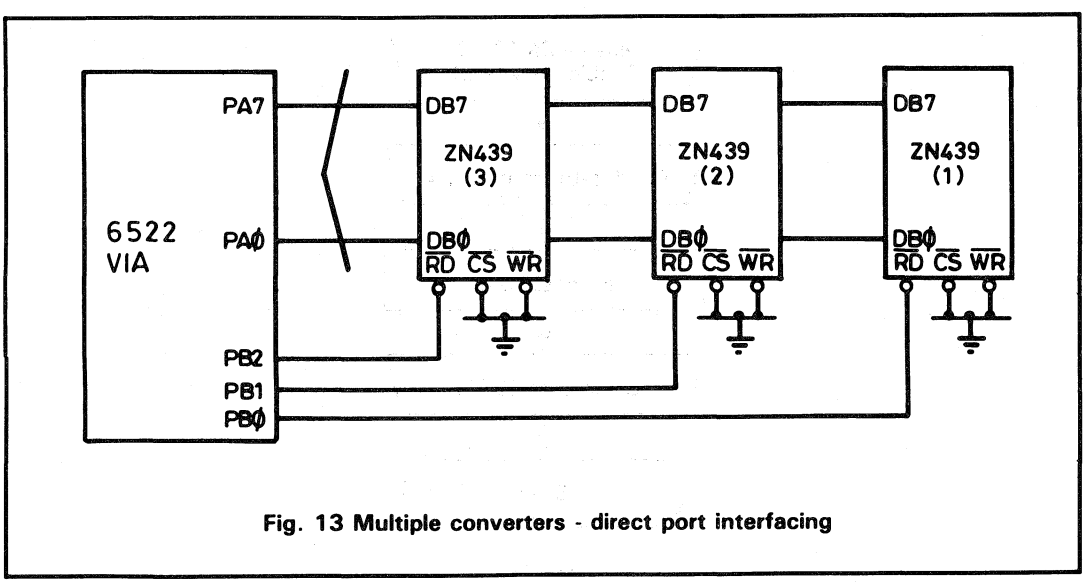



**Fig. 13 Multiple converters - direct port interfacing**

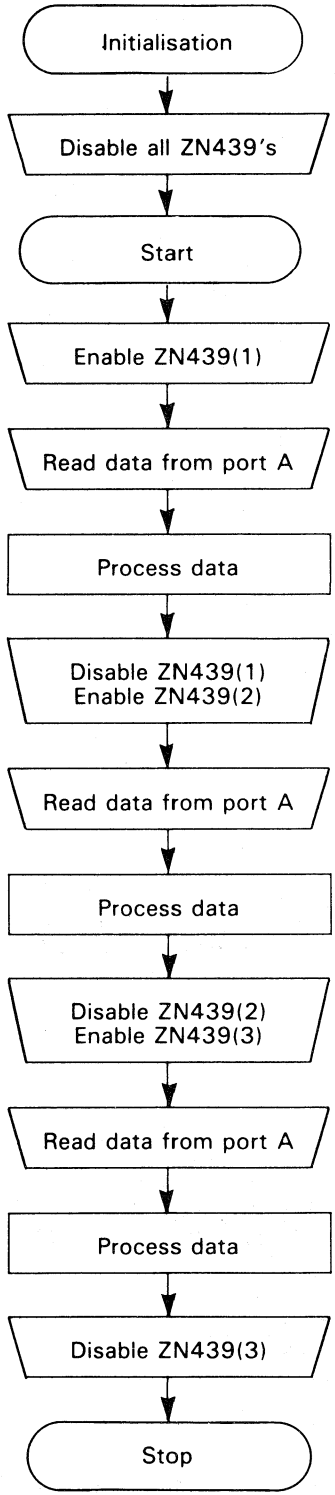

Initialisation
Disable all ZN439's
Start
Enable ZN439(1)
Read data from port A
Process data
Disable ZN439(1)
Enable ZN439(2)
Read data from port A
Process data
Disable ZN439(2)
Enable ZN439(3)
Read data from port A
Process data
Disable ZN439(3)
Stop

**Fig. 14**

| Address | Object code | Label | Mnemonic | Operand | Comments |
|---|---|---|---|---|---|
| 2000 | A9 07 | | LDA | # 07 | |
| 2002 | 8D 00 50 | | STA | 5000 | Disable all ZN439's |
| 2005 | 8D 02 50 | | STA | 5002 | |
| 3000 | A9 06 | | LDA | # 06 | |
| 3002 | 8D 00 50 | | STA | 5000 | Enable ZN439(1) |
| 3005 | AD 01 50 | | LDA | 5001 | Read data from ZN439(1) |
| 3008 | 85 80 | | STA | 80 | Process data |
| 300A | A9 05 | | LDA | # 05 | Disable ZN439(1) |
| 300C | 8D 00 50 | | STA | 5000 | Enable ZN439(2) |
| 300F | AD 01 50 | | LDA | 5001 | Read data from ZN439(2) |
| 3012 | 85 81 | | STA | 81 | Process data |
| 3014 | A9 03 | | LDA | # 03 | Disable ZN439(2) |
| 3016 | 8D 00 50 | | STA | 5000 | Enable ZN439(3) |
| 3019 | AD 01 50 | | LDA | 5001 | Read data from ZN439(3) |
| 301C | 85 82 | | STA | 82 | Process data |
| 301E | A9 07 | | LDA | # 07 | Disable ZN439(3) |
| 3020 | 8D 00 50 | | STA | 5000 | |

**ADDRESS ALLOCATION**

80 Memory address for storing ZN439(1) data.
81 Memory address for storing ZN439(2) data.
82 Memory address for storing ZN439(3) data.
2000 Start address of initialisation.
3000 Start address of ZN439 read program.
5000 VIA data register for port B.
5001 VIA data register for port A.
5002 VIA data direction register for port B.

**Fig. 15**

**Interrupt port interfacing**

**(1) Single converter**

In some cases it may be advantageous to have the ZN439 interrupt driven. The ZN439 would signal to the VIA that new data was available. The VIA would then interrupt the microprocessor which would read and process the converted data. This is easily implemented using an extension of the direct port interfacing circuit of Fig. 10. By connecting the status output to the CA1 input, interrupt driven operation is made possible. A circuit diagram is illustrated in Fig. 16.

A start convert pulse is first applied to the $\overline{WR}$ input. At the end of conversion the status output goes low. This produces a negative transition on the CA1 interrupt input which sets the CA1 interrupt flag within the VIA. With the CA1 interrupt enable bit set the VIA will take the $\overline{IRQ}$ output low to generate a system interrupt. The microprocessor then responds by executing an interrupt service routine. This routine will involve reading the converter data from port A as described previously.

At this point it should be noted that a problem could arise during power up. After $V_{CC}$ has reached 4.75V the status output will go low between 1 and 8 clock cycles later. If the RES input of the VIA is not held low for at least this time the negative transition on the status output will set the CA1 interrupt flag. Therefore once the CA1 interrupt enable bit is set an interrupt will be generated and the microprocessor will read erroneous data. To overcome this problem the CA1 interrupt flag sould be reset during initialisation before the interrupt enable bit is set.

A typical flow diagram and program are shown in Figs. 17 and 18.

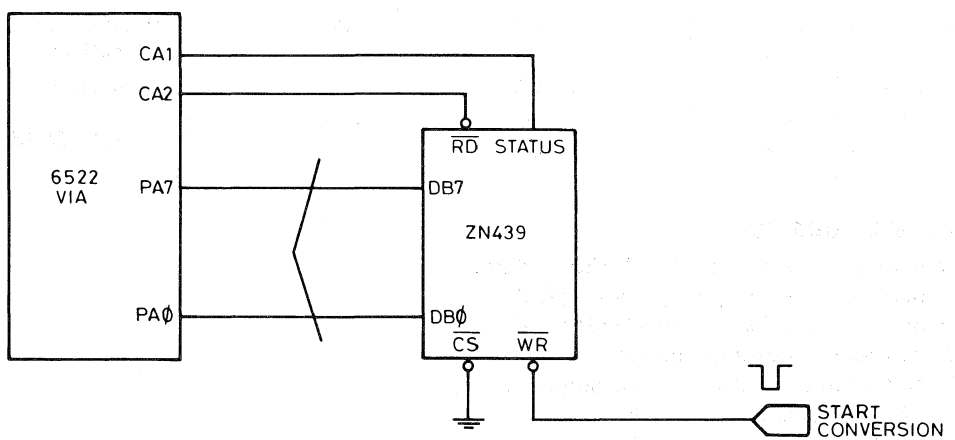



Fig. 16 Single converter - interrupt port interfacing

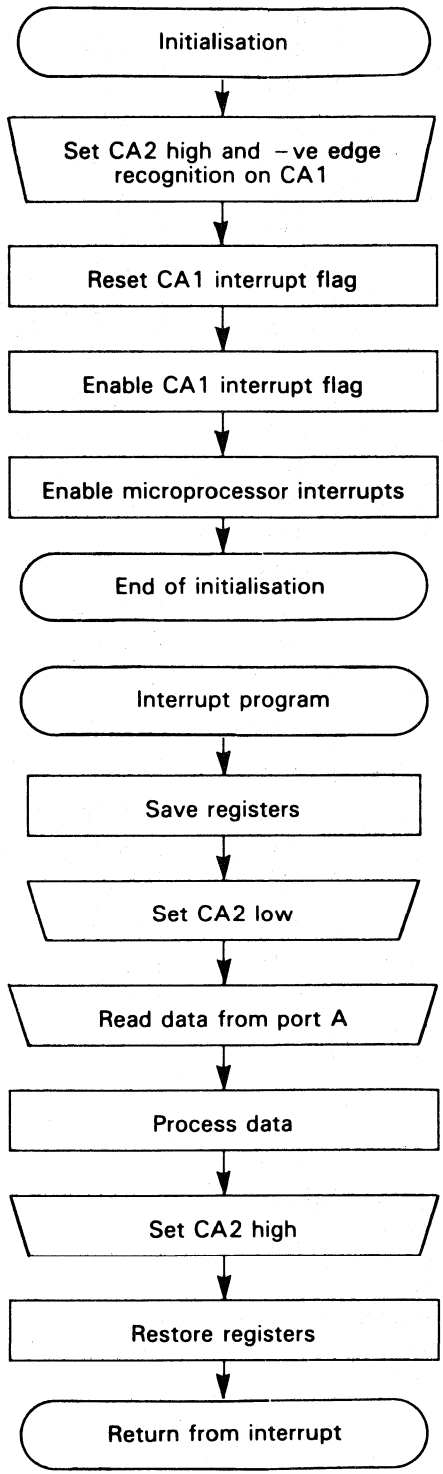

Initialisation
Set CA2 high and −ve edge recognition on CA1
Reset CA1 interrupt flag
Enable CA1 interrupt flag
Enable microprocessor interrupts
End of initialisation
Interrupt program
Save registers
Set CA2 low
Read data from port A
Process data
Set CA2 high
Restore registers
Return from interrupt

**Fig. 17**

| Address | Object code | Label | Mnemonic | Operand | Comments |
|---|---|---|---|---|---|
| 2000 | AD OC 50 | | LDA | 500C | Set CA2 high and negative edge recognition on CA1 without affecting the other port control lines |
| 2003 | 29 FO | | AND | #FO | |
| 2005 | 09 OE | | ORA | # OE | |
| 2007 | 8D OC 50 | | STA | 500C | |
| 200A | A9 82 | | LDA | #82 | Reset CA1 interrupt flag |
| 200C | 8D OD 50 | | STA | 500D | |
| 200F | 8D OE 50 | | STA | 500E | Enable CA1 interrupt flag |
| 2012 | 58 | | CLI | | Enable micro-processor interrupts |
| 3000 | 48 | | PHA | | Save registers |
| 3001 | 8A | | TXA | | |
| 3002 | 48 | | PHA | | |
| 3003 | 98 | | TYA | | |
| 3004 | 48 | | PHA | | |
| 3005 | AD OC 50 | | LDA | 500C | Set CA2 low |
| 3008 | 29 FD | | AND | #FD | |
| 300A | 8D OC 50 | | STA | 500C | |
| 300D | AD 01 50 | | LDA | 5001 | Read data from ZN439 |
| 3010 | 85 80 | | STA | 80 | Process data |
| 3012 | AD OC 50 | | LDA | 500C | Set CA2 high |
| 3015 | 09 02 | | ORA | #02 | |
| 3017 | 8D OC 50 | | STA | 500C | |
| 301A | 68 | | PLA | | Restore registers |
| 301B | A8 | | TAY | | |
| 301C | 68 | | PLA | | |
| 301D | AA | | TAX | | |
| 301E | 68 | | PLA | | |
| 301F | 40 | | RTI | | Return |

**ADDRESS ALLOCATION**

80 Memory address for storing ZN439 data.
2000 Start address of initialisation.
3000 Start address of interrupt program.
5001 VIA data register for port A.
500C VIA peripheral control register
500D VIA interrupt flag register.
500E VIA interrupt enable register.

**Fig. 18**

**(2) Multiple converters**

To interface more than two converters to the VIA two problems have to be overcome.

Firstly there is the problem of generating the interrupt. The standard procedure would be to wire-OR the status outputs together and use this common output to generate the interrupt. This is achieved by connecting the common wire-OR output to the VIA interrupt input CA1.

The second problem is determining which device has generated the interrupt. This is overcome by using the status output of each device as an interrupt flag and connecting each bit to an input bit of port B. By examining the state of these flags the microprocessor can ascertain which device has requested an interrupt.

A circuit diagram detailing the connections required to interface three devices to the VIA is shown in Fig. 19. Port B is configured such that bits 0, 1 and 2 are outputs and bits 5, 6 and 7 are inputs. As in the single converter case an external start convert pulse is applied to the $\overline{WR}$ input of one of the devices. At the end of the conversion the status output goes low which sets the CA1 interrupt flag within the VIA. With the CA1 interrupt enable bit set the VIA will then interrupt the microprocessor. By reading the data on port B and examining bits 5, 6 and 7 the microprocessor can determine which device is responsible for the interrupt. The interrupting converter can then be enabled by taking bit 0, 1 or 2 low. The converter data can then be read from port A. The action of reading the data also clears the interrupt flag within the VIA which removes the interrupt. Finally the appropriate bit of port B is taken high to disable the output buffer of the ZN439 and allow update at the end of the next conversion.

It should be noted that as CA1 is an edge triggered input a second interrupt occuring soon after a first will not be recognised by the VIA. Therefore after servicing one interrupt and before returning from the service routine the interrupt flag data on port B must be examined again. This will ensure that no interrupts are missed. A flow diagram and program are shown in Figs. 20 and 21.

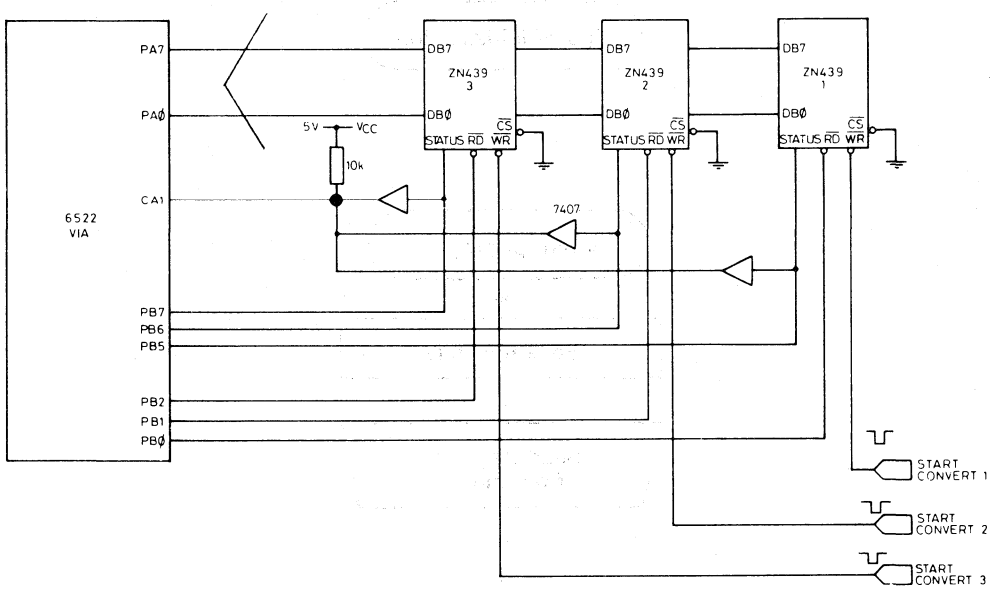
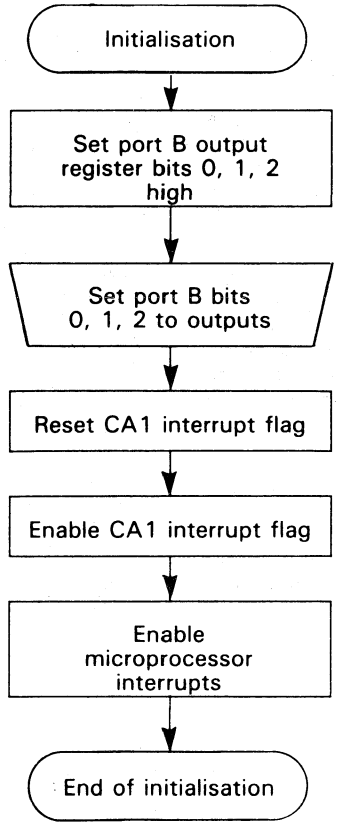
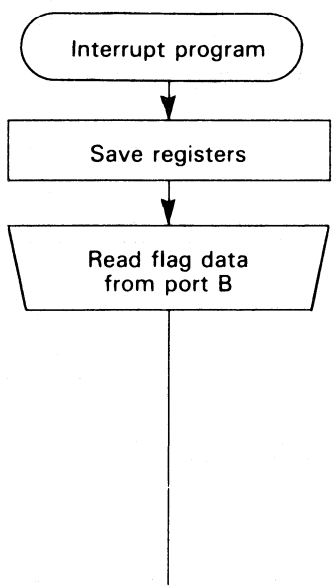



Fig. 19 Multiple converters - interrupt port interfacing


Initialisation
Set port B output register bits 0, 1, 2 high
Set port B bits 0, 1, 2 to outputs
Reset CA1 interrupt flag
Enable CA1 interrupt flag
Enable microprocessor interrupts
End of initialisation


Interrupt program
Save registers
Read flag data from port B

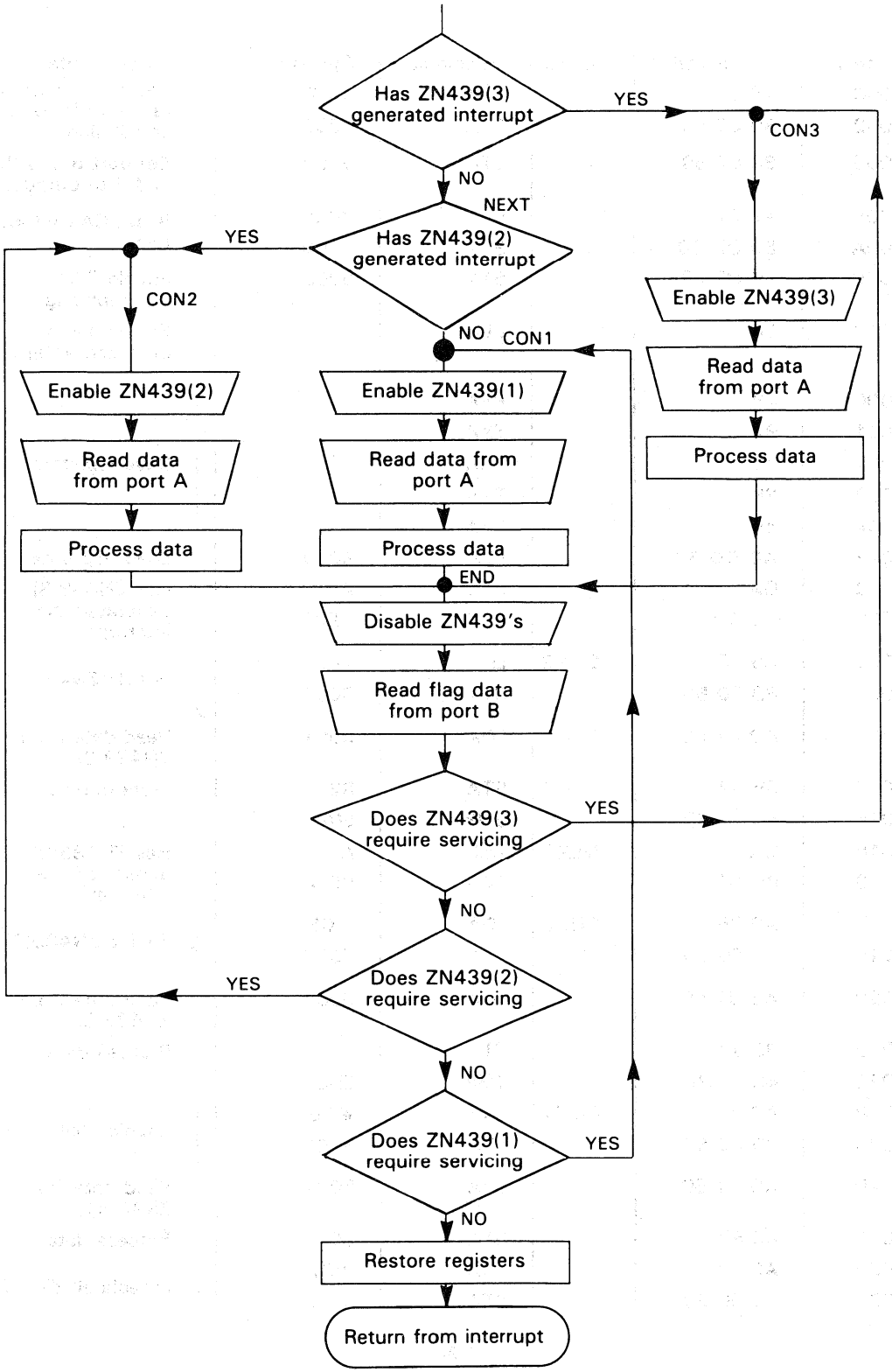

Has ZN439(3) generated interrupt
YES
CON3
NO
NEXT
Has ZN439(2) generated interrupt
YES
CON2
Enable ZN439(3)
NO
CON1
Read data from port A
Enable ZN439(2)
Enable ZN439(1)
Process data
Read data from port A
Read data from port A
Process data
Process data
END
Disable ZN439's
Read flag data from port B
Does ZN439(3) require servicing
YES
NO
Does ZN439(2) require servicing
YES
NO
Does ZN439(1) require servicing
YES
NO
Restore registers
Return from interrupt

Fig. 20

| Address | Object code | Label | Mnemonic | Operand | Comments |
|---|---|---|---|---|---|
| 2000 | A9 07 | | LDA | #07 | Set port B output register bits 0, 1 and 2 high |
| 2002 | 8D 00 50 | | STA | 5000 | |
| 2005 | 8D 02 50 | | STA | 5002 | Set port B bits 0, 1 and 2 to outputs |
| 2008 | A9 82 | | LDA | #82 | Reset CA1 interrupt flag |
| 200A | 8D OD 50 | | STA | 500D | |
| 200D | 8D OE 50 | | STA | 500E | Enable CA1 interrupt flag |
| 2010 | 58 | | CLI | | Enable micro-processor interrupts |
| 3000 | 48 | | PHA | | Save registers |
| 3001 | 8A | | TXA | | |
| 3002 | 48 | | PHA | | |
| 3003 | 98 | | TYA | | |
| 3004 | 48 | | PHA | | |
| 3005 | AD OO 50 | | LDA | 5000 | Load flag data |
| 3008 | OA | | ASL | A | Has ZN439(3) generated the interrupt |
| 3009 | BO OD | | BCS | NEXT | |
| 300B | A9 03 | CON3 | LDA | #03 | Enable ZN439(3) |
| 300D | 8D 00 50 | | STA | 5000 | |
| 3010 | AD 01 50 | | LDA | 5001 | Read data from ZN439(3) |
| 3013 | 85 82 | | STA | 82 | Process data |
| 3015 | 4C 37 30 | | JMP | END | |
| 3018 | OA | NEXT | ASL | A | Has ZN439(2) generated the interrupt |
| 3019 | BO OD | | BCS | CON1 | |
| 301B | A9 05 | CON2 | LDA | #05 | Enable ZN439(2) |
| 301D | 8D 00 50 | | STA | 5000 | |
| 3020 | AD 01 50 | | LDA | 5001 | Read data from ZN439(2) |
| 3023 | 85 82 | | STA | 81 | Process data |
| 3025 | 4C 37 30 | | JMP | END | |
| 3028 | A9 06 | CON1 | LDA | #06 | Enable ZN439(1) |
| 302A | 8D 00 50 | | STA | 5000 | |
| 302D | AD 01 50 | | LDA | 5001 | Read data from ZN439(1) |
| 3030 | 85 80 | | STA | 80 | Process data |
| 3032 | A9 07 | | LDA | #07 | Disable all ZN439's |
| 3034 | 8D 00 50 | | STA | 5000 | |

Fig. 21

| Address | Object code | Label | Mnemonic | Operand | Comments |
|---|---|---|---|---|---|
| 3037 | AD 00 50 | END | LDA | 5000 | Load flag data |
| 303A | OA | | ASL | A | Does ZN439(3) need servicing |
| 303B | 90 CE | | BCC | CON3 | |
| 303D | OA | | ASL | A | Does ZN439(2) need servicing |
| 303E | 90 DC | | BCC | CON2 | |
| 3040 | OA | | ASL | A | Does ZN439(1) need servicing |
| 3041 | 90 E5 | | BCC | CON1 | |
| 3043 | 68 | | PLA | | Restore registers |
| 3044 | A8 | | TAY | | |
| 3045 | 68 | | PLA | | |
| 3046 | AA | | TAX | | |
| 3047 | 68 | | PLA | | |
| 3048 | 40 | | RTI | | Return |

**ADDRESS ALLOCATION**

80 Memory address for storing ZN439(1) data.
81 Memory address for storing ZN439(2) data.
82 Memory address for storing ZN439(3) data.
2000 Start address of initialisation.
3000 Start address of interrupt program.
5000 VIA data register for port B.
5001 VIA data register for port A.
5002 VIA data direction register for port B.
500D VIA interrupt flag register.
500E VIA interrupt enable register.

**Fig. 21 (cont.)**

## CONCLUSIONS

The examples given in this report should demonstrate the minimal hardware and simple software required to interface the ZN439 to the 6500 series of microprocessors. A wide variety of configurations have been given to allow the designer maximum flexibility in choosing an option best suited to his application.

All the programs given show the start address at location 2000 with the VIA starting at location 5000. These are purely arbitrary and will undoubtedly reside at different locations within the designers system. All the programs are directly relocatable except the last program of Fig. 21 which includes two absolute jumps whose operands will require changing.

In the flow diagrams there is a box labelled 'process data'. This translates in the program to storing the ZN439 data in a memory location. In reality this will be replaced by more complex data processing. For completeness the X and Y registers are saved and restored during the interrupt service routine, despite not being used in the program. This is because the more complex processing required by the designer will probably include the use of the X and Y registers.

It has been assumed throughout that the ZN439's will be the only interrupting devices in the system. If this is not the case then some form of polling will be required to determine what has generated the interrupt. With port interfacing this is easily achieved by examining the VIA interrupt flag register. In the case of direct bus interfacing the interrupt flag provided by the buffered status output (Fig. 5) can be examined.

Despite this report being written for the 6500 family the principles involved are valid for other microprocessors. It is therefore hoped that the techniques presented here will prove valuable to designers interfacing the ZN439 to other popular microprocessors.

# Interfacing the ZN447/8/9 A-D Converters to the Z80μP via a Z80 PIO

**This report illustrates how to interface one or more ZN447/8/9 A-D converters to a Z80 based microprocessor system using a Z80 PIO. Circuit diagrams and program examples are given to enable the user to get his interface system working. The following is also applicable to the faster versions of the Z80μP and the Z80 PIO and also to the CMOS versions. Most of the principles described can also be applied when interfacing the ZN447/8/9 to other popular μPs.**

**In order to keep this report concise it is assumed that the reader is familiar with the Z80 system.**

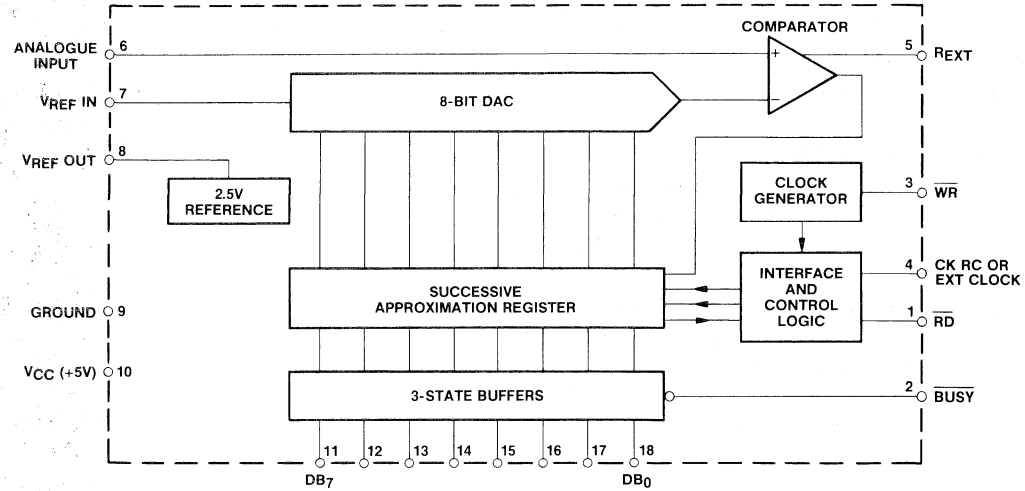



**Fig. 1 ZN447/8/9 system diagram**

## TNE ZN447/8/9 A-D CONVERTER

The ZN447/8/9 are 8-bit successive approximation A-D converters with linearity errors of ± ¼, ±½ and 1 LSB respectively.

Hereafter any description relating to one of these devices is equally applicable to the other two types.

All active circuitry is contained on-chip including three-state output buffers, 2.5V bandgap reference and a clock generator.

They are each capable of converting unipolar or bipolar input voltages with the only external components required for operation being a reference resistor and capacitor, clock capacitor, resistor to the negative supply and the analogue input scaling resistor(s) (to accommodate the different input voltages).

A conversion is initiated by taking the $\overline{WR}$ input low and then high. The conversion then takes between 7½ and 8½ clock cycles after the $\overline{WR}$ positive edge. The $\overline{WR}$ input signal may be completely asynchronous to the chip clock. The falling edge of the $\overline{WR}$ signal sets the MSB high and the remaining bits low. This edge also sets the $\overline{BUSY}$ output low. Once started the converter cycles through a successive approximation routine to arrive at a result (see data sheet for explanation). When the conversion is finished, the $\overline{BUSY}$ output goes high indicating that valid data may now be read. A low at the $\overline{RD}$ input enables the data outputs and a high puts them into the high impedance state.

The devices will operate correctly with clock frequencies up to at least 900kHz. At 900kHz the conversion time is less than 9.5$\mu$s. (in fact the devices will typically operate above 900kHz but some loss in accuracy may result).

The negative supply requirement is minimal (e.g. 75$\mu$A) and can easily be supplied from a simple diode pump circuit.

Further information including the input resistors required for various unipolar and bipolar input voltages and examples of diode pump circuits, can be obtained from the data sheet.

## Z80 PIO

The Z80 PIO is a programmable two port device which provides a TTL compatible interface between peripheral devices and the Z80 CPU. It is capable of interfacing directly to the CPU without any external logic. The two 8-bit, bidirectional ports, each have two handshake lines (RDY and $\overline{STB}$) for use when transferring data to or from peripherals. Either port or indeed any port bit, can be programmed to act as an input or output.

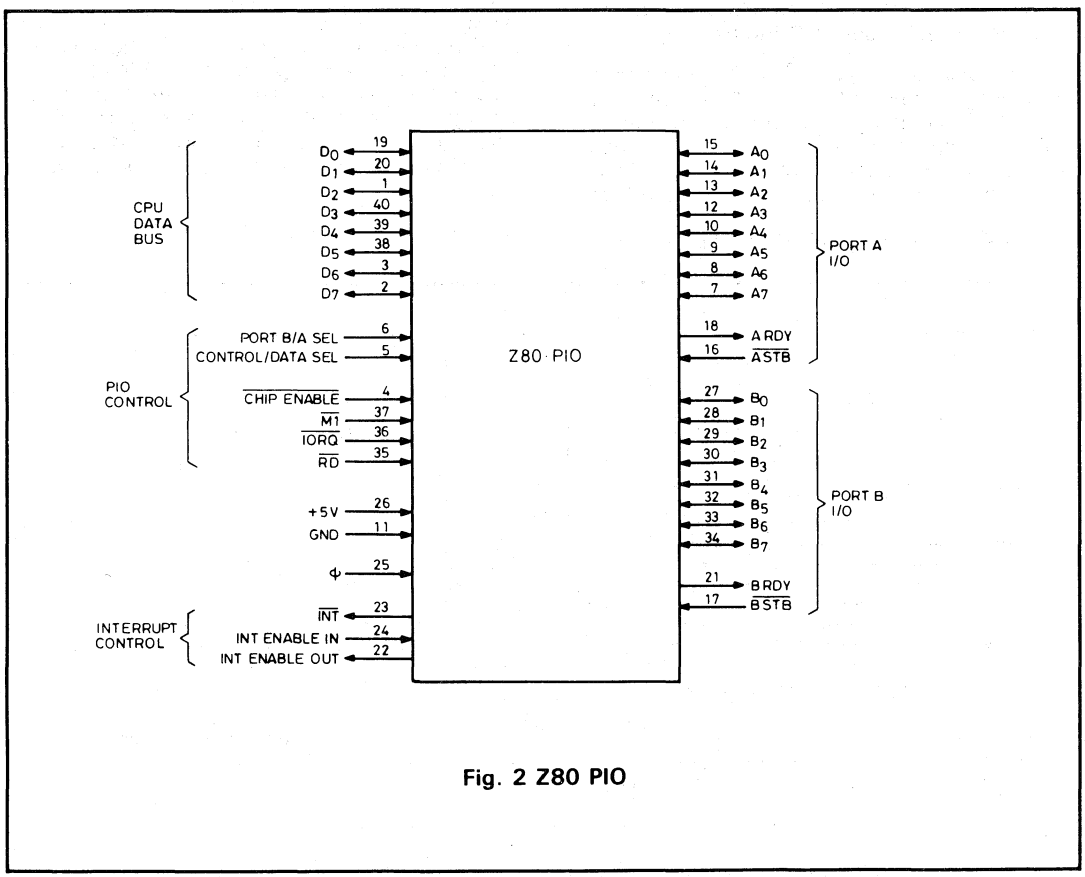



**Fig. 2 Z80 PIO**

The PIO has 4 operating modes:

Mode 0 (Output mode) - All port bits are set to outputs.

Mode 1 (Input mode) - All port bits are set to inputs.

Mode 2 (Bidirectional mode) - Used for bidirectional data transfer - not considered in this report.

Mode 3 (Control mode) - Each bit can be programmed individually to act as an input or output. Useful for status and control applications.

We will utilise mode 1 for reading the result of the A-D conversion. With mode 3 we can configure some of the port bits as outputs, taking them low and high as desired (can be used for controlling the $\overline{RD}$ and $\overline{WR}$ input on the converters) and we can configure some of the port bits as inputs (for monitoring the $\overline{BUSY}$ outputs). If the $\overline{BUSY}$ outputs are not being monitored and the port bits are being used as outputs, mode 0 could instead be used for controlling the $\overline{RD}$ and $\overline{WR}$ inputs.

In the input mode, the $\overline{STB}$ input needs to be low to allow data into the port. A positive edge on the $\overline{STB}$ latches data into the port, causes RDY to go low and generates an interrupt if enabled. During a port read the RDY line will be forced low, if not already low, and then high.

This is a brief introduction to a complex device. Further information can be obtained from the manufacturers data sheets.

## INTERFACING A SINGLE ZN447/8/9 TO THE Z80 USING A SINGLE PORT

If it is required to interface only one ZN448 to the Z80 system, this can be achieved using only a single port (½PIO). Here the $\overline{RD}$ input on the ZN448 is tied low and hence the data outputs are permanently enabled.

A conversion can be started with a $\overline{WR}$ pulse derived from the RDY signal or from some other logic. Valid data can then be read when the conversion is finished. In order to ensure this, either a program delay can be used ((i) below) or the $\overline{BUSY}$ output can be used to generate an interrupt via the port $\overline{STB}$ input ((ii) below).

### (i) Data acquisition using a program delay

Here a dummy read is issued to the port to generate a positive transition on the RDY output. This edge then triggers a monostable which in turn supplies a $\overline{WR}$ pulse to the ZN448. This initiates a conversion. The program then cycles through a delay routine to give the conversion time to finish. After this a genuine read is issued to the port and the data then processed as required.

The circuit diagram is as follows:

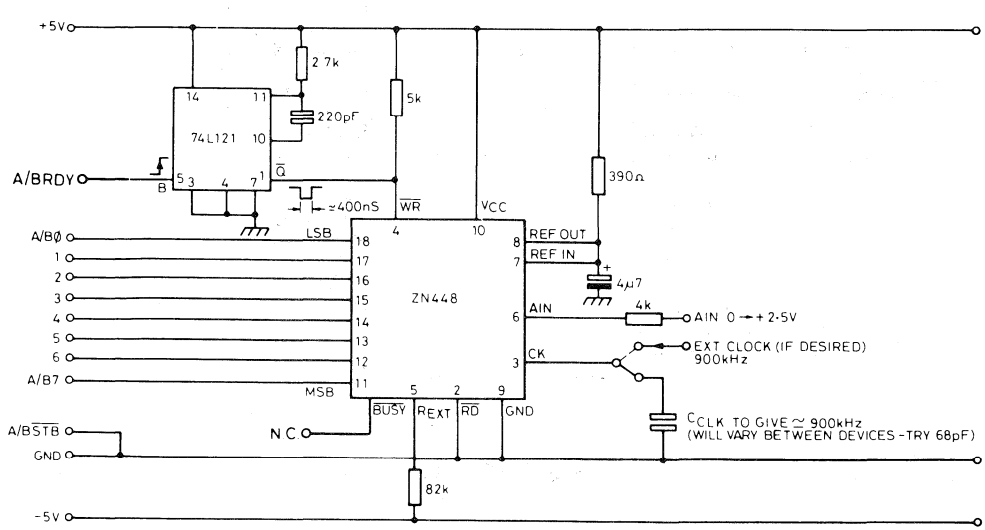



**Fig. 3 Interfacing a single ZN448 to a single port - program controlled**

**PROGRAM LISTING**

**PROGRAM 1**

| Address | Object code | Label | Source code | Comments |
|---|---|---|---|---|
| NN00 | 3E 4F | | LD A,4FH | Sets port to input (Mode 1) |
| NN02 | D3 PORTCO | | OUT PORTCO,A | |
| NN04 | DB PORTDA | | IN A,PORTDA | Dummy read from port |
| NN06 | 3E DELAY | | LD A,DELAY | Initialises A for delay |
| NN08 | 3D | (1) | DEC A | Delay routine |
| NN09 | 20 FD | | JR NZ, (1) | |
| NN0B | DB PORTDA | | IN A,PORTDA | Reads result of conversion |
| NN0D | 32 MEM | | LD (MEM),A | Stores result |
| NN10 | ? | | ? | Returns to monitor program (Command(s) system dependant) |

**KEY:**

NN00 = Any Suitable starting address.
PORTCO = Port control address.
PORTDA = Port data address.
DELAY = Initialisation byte for delay (see comments).
MEM = 16-bit memory location nominated for storing data. (Needs assembling in the order Lo-byte, Hi-byte in the object code).

**COMMENTS**

The delay required depends on processor speed and the ZN448 clock frequency. With the ZN448 clock frequency at 900kHz, try working down from DELAY = 06H. For slower clocks the delay may need increasing accordingly.

When the processor reads the result of the conversion from the port, a further conversion is automatically initiated. This is of no consequence during normal operation. However if the data is being inspected manually for evaluation purposes, the data can appear incorrect at the first glance. This is because the valid data on the ZN448 outputs is one conversion behind the data read into the processor. Hence if the analogue input voltage is on the edge of a code transition, any noise present could possibly cause the result in memory and the data on the ZN448 outputs to differ slightly. If desired this can be overcome by examining the ZN448 outputs just before the conversion result is read (e.g. insert a break in the program), and then acquire the data for subsequent comparison.

The above arrangement is useful when there is only one spare port and it can be dedicated to this purpose.

**(ii) Data acquisition under interrupt control**

Interrupts are useful when interfacing to slow peripherals. However the ZN448 is not itself a slow peripheral as it can be operated to give a conversion time of less than 10$\mu$s. Hence it does not need to be interrupt driven.

However it may be required to call on the ZN448 relatively infrequently - as governed by some timing logic (e.g. a counter timer chip):

(a) this timing logic could vector to a subroutine which then starts a conversion and reads the result. In this case the subroutine might as well incorporate a delay - this has been covered in the previous section.

(b) alternatively this timing logic could initiate a conversion directly or, for example, via a monostable. This effectively makes the ZN448 appear slower and now makes interrupts more useful.

The second situation (b) above is now considered in this section. It is left to the user to configure this "timing logic" to best suit his particular requirements.

Remember that $\overline{\text{BUSY}}$ goes high to signal the end of conversion and also that the port $\overline{\text{STB}}$ input responds to positive transitions. Thus when $\overline{\text{BUSY}}$ is connected to $\overline{\text{STB}}$ and interrupts are enabled, an interrupt will be generated when $\overline{\text{BUSY}}$/$\overline{\text{STB}}$ goes high. This would then summon a service routine to read the result of the conversion.

**PROGRAM EXAMPLE**

This is a program to start a conversion, cycle through a delay routine (until conversion has finished) and then read the result. This data is then stored in memory.

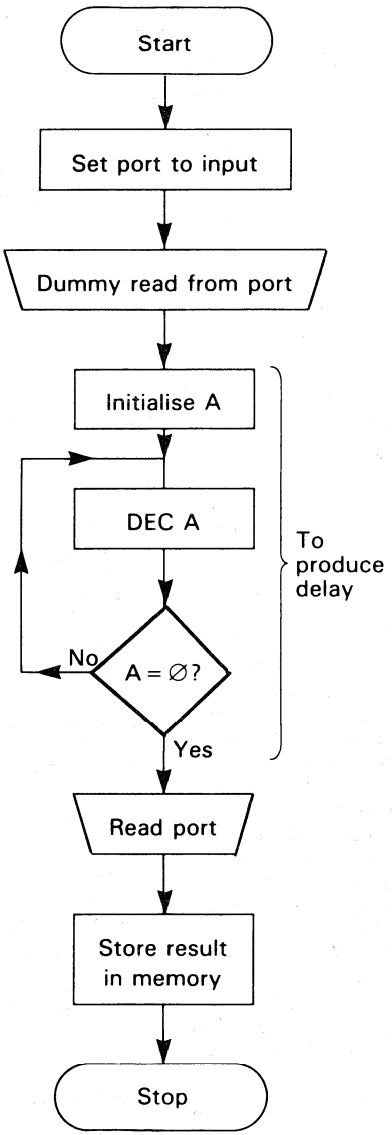
**PROGRAM STATEMENT**

: Nominate memory location for storing the conversion results:

: Decide on delay required (see comments for suggestions).

: It is assumed that the port needs initialising.

**FLOWCHART 1**



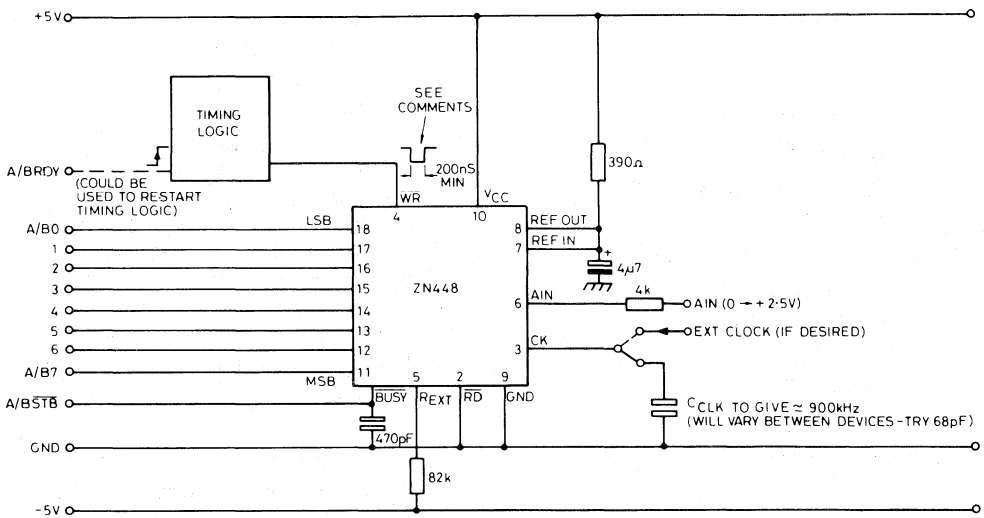



**Fig. 4 Interfacing a single ZN448 to a single port - interrupt driven**

The capacitor on the $\overline{\text{BUSY}}$ O/P is to meet the port data to $\overline{\text{STB}}$ rising edge set up time.

## PROGRAM EXAMPLE

Here, when an interrupt is generated via $\overline{\text{BUSY}}$, the μP is vectored to the service routine which then reads and stores the result of the conversion, the conversion having been previously initiated by the timing logic.

The μP is set to interrupt mode 2, as the ports are designed to be used in this mode. The contents of the I register and the port interrupt vector are combined by the μP to form a 16-bit vector. This is then used to look up the starting address of the interrupt service routine. The μP then loads the program counter with this address and continues program execution from this location.

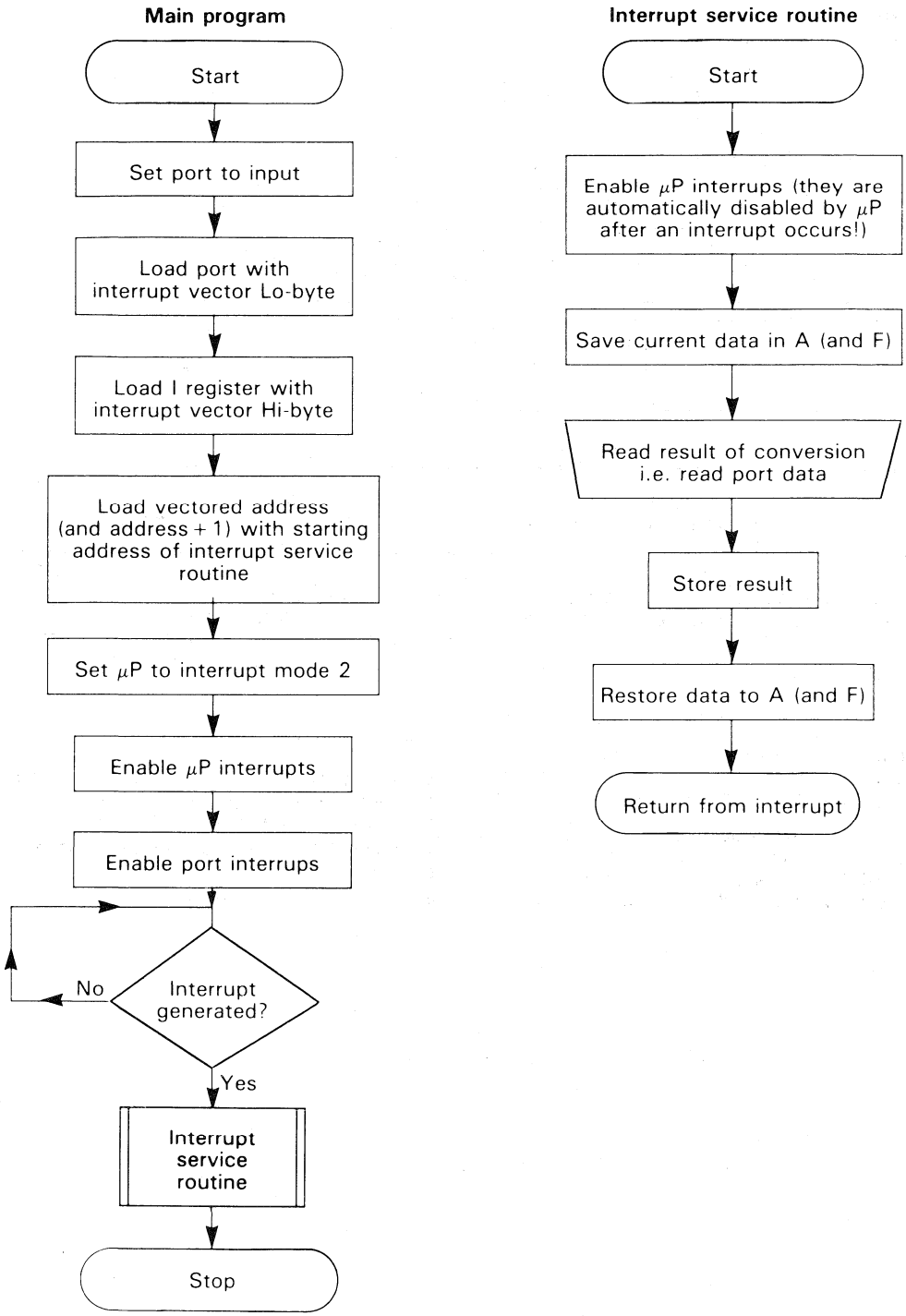
## PROGRAM STATEMENTS

: Nominate memory locations for the vectored address, the interrupt service routine and for storing the conversion result.

: It is assumed that the user initiates conversion correctly when required.

: It is assumed that the port needs initialising:

FLOWCHART 2


Main program
Start
Set port to input
Load port with interrupt vector Lo-byte
Load I register with interrupt vector Hi-byte
Load vectored address (and address + 1) with starting address of interrupt service routine
Set μP to interrupt mode 2
Enable μP interrupts
Enable port interrups
No
Interrupt generated?
Yes
Interrupt service routine
Stop
Interrupt service routine
Start
Enable μP interrups (they are automatically disabled by μP after an interrupt occurs!)
Save current data in A (and F)
Read result of conversion i.e. read port data
Store result
Restore data to A (and F)
Return from interrupt

**PROGRAM LISTING**

**PROGRAM 2**

| Address | Object code | Label | Source code | Comments |
|---|---|---|---|---|
| NN00 | 3E 4F | | LD A,4FH | Sets port to input (Mode 1) |
| NN02 | D3 PORTCO | | OUT PORTCO,A | |
| NN04 | 3E IVECL | | LD A,IVECL | Loads port with interrupt vector Lo-byte |
| NN06 | D3 PORTCO | | OUT PORTCO,A | |
| NN08 | 3E IVECH | | LD A,IVECH | Loads I register with interrupt vector Hi-byte |
| NN0A | ED 47 | | LD I,A | |
| NN0C | 3E SERVL | | LD A,SERVL | Loads vectored address (and consecutive address) with starting address of interrupt service routine |
| NN0E | 32 IVEC | | LD (IVEC),A | |
| NN11 | 3E SERVH | | LD A,SERVH | |
| NN13 | 32 IVEC + 1 | | LD (IVEC + 1),A | |
| NN16 | ED 5E | | IM 2 | Sets $\mu$P to Interrupt mode 2 |
| NN18 | FB | | EI | Enables $\mu$P interrupts |
| NN19 | 3E 83 | | LD A,83H | Enables port interrupts |
| NN1B | D3 PORTCO | | OUT PORTCO,A | |
| NN1D | 76 | | HALT | Waits for interrupt (or reset!) |
| NN1E | ? | | ? | Returns to monitor (command(s) system dependant) |

**INTERRUPT SERVICE ROUTINE**

| Address | Object code | Label | Source code | Comments |
|---|---|---|---|---|
| MM00 | FB | | EI | Re-enables $\mu$P interrupts |
| MM01 | F5 | | PUSH AF | Stores current values of AF |
| MM02 | DB PORTDA | | IN A,PORTDA | Reads result of conversion |
| MM04 | 32 MEM | | LD(MEM),A | Stores result in memory |
| MM07 | F1 | | POP AF | Restores AF values |
| MM08 | ED 4D | | RETI | Returns from interrupt |

**KEY:**

NN00 = Any Suitable starting address.
PORTCO = Port control address.
PORTDA = Port data address.
IVECL = Low-byte of 16-bit interrupt vector (in port).
IVECH = High-byte of 16-bit interrupt vector (in I register).
IVEC = 16-bit interrupt vector formed by IVECH and IVECL.
IVEC + 1 = 16-bit address one location higher up in memory than IVEC.
SERVL = Interrupt service routine starting address-low byte.
SERVH = Interrupt service routine starting address-high byte.
MM00 = 16-bit starting address for interrupt service routine formed by SERVH and SERVL.
MEM = 16-bit address nominated for storing conversion results.
(Remember that the above 16-bit addresses need to be assembled in the order Lo-byte, Hi-byte in the object code).

## COMMENTS

Remember that the $\overline{WR}$ falling edge sets the MSB high and all the other bits low. Hence the $\mu$P must latch the conversion result before any further $\overline{WR}$ falling edges are generated - otherwise incorrect data could be latched! This arrangement is useful when acquiring data relatively infrequently, under the control of some external logic, and/or when the ZN448 is operated with a slow clock.

For evaluation purposes, a single-shot debounced $\overline{WR}$ pulse may be supplied. Data can then be examined for integrity.

## INTERFACING ONE OR MORE ZN447/8/9's TO THE Z80.

When it is required to connect more than a single ZN448 to a port, some control must be exerted over the three-state outputs. This is easily achieved by connecting the $\overline{RD}$ inputs to the bit outputs from another port. The relevant port bits and thus the $\overline{RD}$ inputs, can then be taken low individually, to enable only the desired device.

Further, this controlling port can do other useful things for us, such as generating $\overline{WR}$ pulses (by taking the relevant port bit(s) low and back high) and checking for the end of a conversion by monitoring the $\overline{BUSY}$ output(s).

Setting some of the port bits as inputs and some as outputs takes advantage of the control mode (mode 3) of the port.

The enable/disable times of the converter outputs need not be considered, since they are much less than the Z80 instruction execution times.

## DATA ACQUISITION UNDER PROGRAM CONTROL

Here one port is assigned to reading the data from the ZN448's and another port used to control the $\overline{RD}$ and $\overline{WR}$ inputs and to monitor the $\overline{BUSY}$ outputs.

As an example consider interfacing 2 × ZN448's as follows:

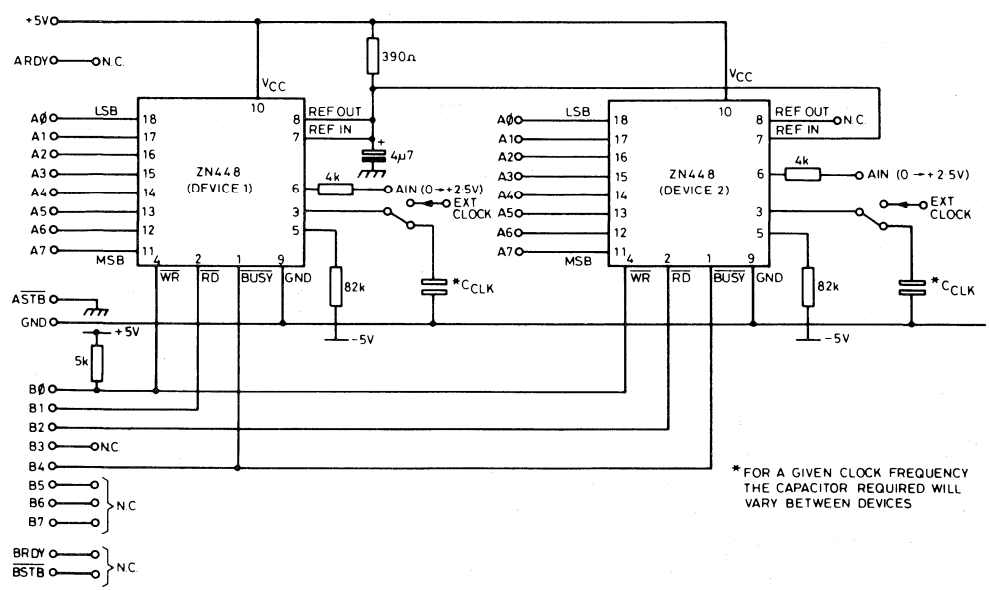



**Fig. 5 Interfacing 2 × ZN448's to the Z80 using both ports of a Z80 PIO - $\overline{BUSY}$'s polled**

Note that in the circuit of Fig. 5, the reference input ($V_{REF\ IN}$) of the second ZN448 is driven from the reference output ($V_{REF\ OUT}$) of the first ZN448. This provides excellent gain tracking between converters. Up to five ZN448's may be driven from a single internal reference without changing the reference resistor.

## PROGRAM EXAMPLE

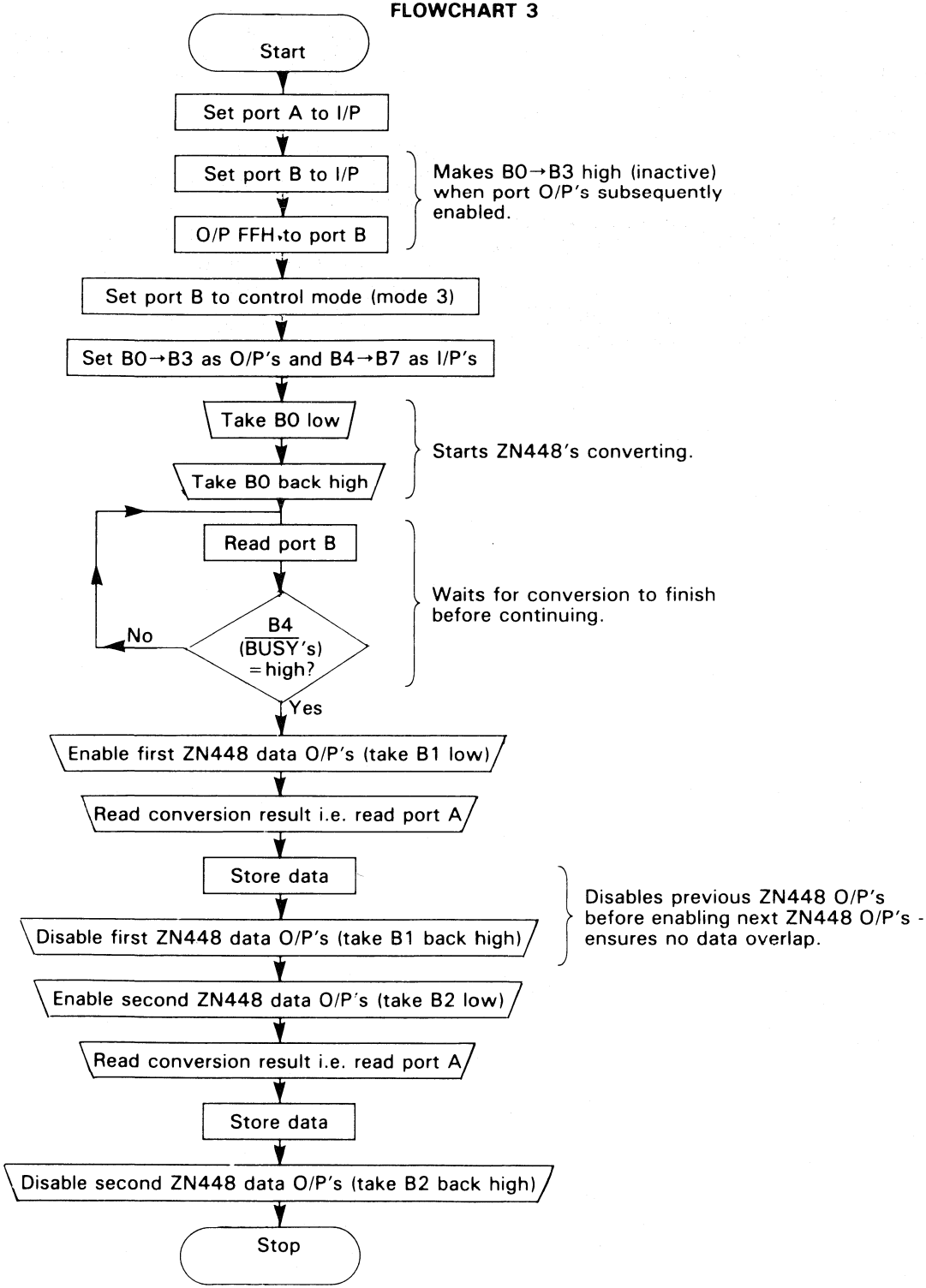
Here is a program to start the two ZN448's converting, then read and store the data when they have finished the conversion.

Conversion is initiated by taking B0 ( = both $\overline{WR}$ inputs) low and then high. B4 ( = both $\overline{BUSY}$'s) is then polled until it is found to be high, thus indicating that both ZN448's have finished converting. Each device is then brought out of the three-state condition in turn - by taking B1 and B2 ( = both $\overline{RD}$ inputs) low individually - to allow the data to be read.

## PROGRAM STATEMENTS

```
: Nominate memory locations for storing the
  conversion results.
: It is assumed that both ports need initialising.
: FEH = Take WR low word.
: FDH = Select first ZN448 word.
: FBH = Select second ZN448 word.
```

**FLOWCHART 3**


Start
Set port A to I/P
Set port B to I/P
O/P FFH to port B
Makes B0→B3 high (inactive) when port O/P's subsequently enabled.
Set port B to control mode (mode 3)
Set B0→B3 as O/P's and B4→B7 as I/P's
Take B0 low
Take B0 back high
Starts ZN448's converting.
Read port B
B4 (BUSY's) = high?
No
Yes
Waits for conversion to finish before continuing.
Enable first ZN448 data O/P's (take B1 low)
Read conversion result i.e. read port A
Store data
Disable first ZN448 data O/P's (take B1 back high)
Disables previous ZN448 O/P's before enabling next ZN448 O/P's - ensures no data overlap.
Enable second ZN448 data O/P's (take B2 low)
Read conversion result i.e. read port A
Store data
Disable second ZN448 data O/P's (take B2 back high)
Stop

**PROGRAM LISTING**

**PROGRAM 3**

| Address | Object code | Label | Source code | Comments |
|---|---|---|---|---|
| NN00 | 3E 4F | | LD A,4FH | Sets port A to input (Mode 1) |
| NN02 | D3 PORTCO1 | | OUT PORTCO1,A | |
| NN04 | DB PORTCO2 | | OUT PORTCO,A | Sets port B to input (mode 1) |
| NN06 | 3E FF | | LD A,FFH | O/P's FFH to port B (to make O/P's inactive when first enabled) |
| NN08 | D3 PORTDA2 | | OUT PORTDA2,A | |
| NN0A | 3E CF | | LD A,CFH | Sets port B to control mode (mode 3) |
| NN0C | D3 PORTCO2 | | OUT PORTCO2,A | |
| NN0E | 3E F0 | | LD A,F0H | Sets B0→B3 as O/P's and B4→B7 as I/P's |
| NN10 | D3 PORTCO2 | | OUT PORTCO2,A | |
| NN12 | 3E FE | | LO A,FEH | Takes B0 low and then back high to start devices converting |
| NN14 | D3 PORTDA2 | | OUT PORTDA2,A | |
| NN16 | 3E FF | | LD A,FFH | |
| NN18 | D3 PORTDA2 | | OUT PORTDA2,A | |
| NN1A | DB PORTDA2 | POLL | IN A,PORTDA2 | Waits for $\overline{BUSY}$'s to go high before continuing |
| NN1C | CB 67 | | BIT 4,A | |
| NN1E | 28 FA | | JR Z,POLL | |
| NN20 | 3E FD | | LD A,FDH | Takes $\overline{RD}$ low on first ZN448 |
| NN22 | D3 PORTDA2 | | OUT PORTDA2,A | |
| NN24 | DB PORTDA1 | | IN A,PORTDA1 | Reads and stores first ZN448 conversion result |
| NN26 | 32 MEM1 | | LD (MEM1),A | |
| NN29 | 3E FF | | LD A,FFH | Takes $\overline{RD}$ back high |
| NN2B | D3 PORTDA2 | | OUT PORTDA2,A | |
| NN2D | 3E FB | | LD A,FBH | Takes $\overline{RD}$ low on second ZN448 |
| NN2F | D3 PORTDA2 | | OUT PORTDA2,A | |
| NN31 | DB PORTDA1 | | IN A,PORTDA1 | Reads and stores second ZN448 conversion result |
| NN33 | 32 MEM2 | | LD (MEM2),A | |
| NN36 | 3E FF | | LD A,FFH | Takes RD back high |
| NN38 | D3 PORTDA2 | | OUT PORTDA2,A | |
| NN3A | ? | | ? | Return to monitor (command(s) system dependant) |

**KEY:**

NN00 = Any Suitable starting address.
PORTCO1 = Port A control address.
PORTCO2 = Port B control address.
PORTDA1 = Port A data address.
PORTDA2 = Port B data address.
MEM1 = 16-bit address nominated for storing first ZN448 data. MEM2 = 16-bit address nominated for storing second ZN448 data.
(Remember that MEM1 and MEM2 need to be assembled in the order Lo-byte, Hi-byte in the object code).

## COMMENTS

The principles illustrated in program 3 can be extended to allow the interfacing of more ZN448's. In fact it can immediately be seen that there are four port B lines spare that can be used for this purpose.

Further, up to three $\overline{BUSY}$ outputs can be connected to a single port bit and likewise up to three $\overline{WR}$ inputs can be driven from a single port bit - but here the pull-up resistor may need reducing to 2.4K. (If a CMOS PIO is used, the pull-up resistor can be dispensed with).

We can readily interface four ZN448's by using two port lines to drive the $\overline{WR}$ inputs and two port lines to monitor the $\overline{BUSY}$ outputs. The remaining four port lines connecting to the $\overline{RD}$ inputs and being used to select the required ZN448.

If the $\overline{BUSY}$ outputs are not polled and a software delay is used instead (covered in the section on interfacing a single ZN447/8/9), we can interface up to 6 devices. Two of the port lines will be needed to drive the 6 $\overline{WR}$ inputs and the remaining 6 lines will again be used to enable the required ZN448.

The leakage current of the ZN448 three-state outputs need not concern us ($\pm 2\mu A$ max. at 2V).

If the software needs changing to suit a particular hardware setup, the above principles are still applicable i.e.:

- Initiate conversions by taking the relevant port bit(s) assigned to the $\overline{WR}$ inputs low and back high.
- Ensure that conversion is over before reading the result - by polling the $\overline{BUSY}$ outputs (or using a softare delay).
- Enable the ZN448's individually (to prevent contention) - by taking the appropriate port bit(s) and hence $\overline{RD}$ inputs low individually - and read the conversion result.

In practice it may be that we are interested in only one of the ZN448's at a particular time. Here, though we may start several devices converting at the same time, we can just ignore the others and read only the desired device.

## DATA ACQUISITION UNDER INTERRUPT CONTROL

As discussed in the previous section on interrupts, the ZN448 is not a slow peripheral and hence does not need to be interrupt driven. However if it is wished to utilise the ZN448 relatively infrequently - under the control of some timing logic - then interrupts become more useful. This is considered in this section.

Here one port is assigned to reading the data from the ZN448's and another port is used to control the $\overline{RD}$ inputs and to monitor the $\overline{BUSY}$ outputs. In fact we can set the port to generate an interrupt when only one of a number of port bits go high. Thus we can generate an interrupt when a $\overline{BUSY}$ goes high. In order to get these facilities the port needs setting to its control mode (mode 3).

Care must be taken when using a port to generate interrupts in this manner. This is because the bits set to give the interrupt, must first all be low, before an interrupt can be generated on any of them going high. Also if any of these bits remain high, further interrupts will be prevented. Therefore, the relevant port bits must be set low initially and must also be set back low after the interrupting device has been serviced. This means that for our purposes, we must ensure that the $\overline{WR}$ inputs and hence the $\overline{BUSY}$ outputs, are low initially and are set back low again after servicing. This can be achieved using positive edge triggered D-type flip-flops with preset and clear inputs - see below. (Remember that $\overline{BUSY}$ is held low by a low on the $\overline{WR}$ input and goes high at the end of a conversion).

An example, consider interfacing two ZN448's as follows:

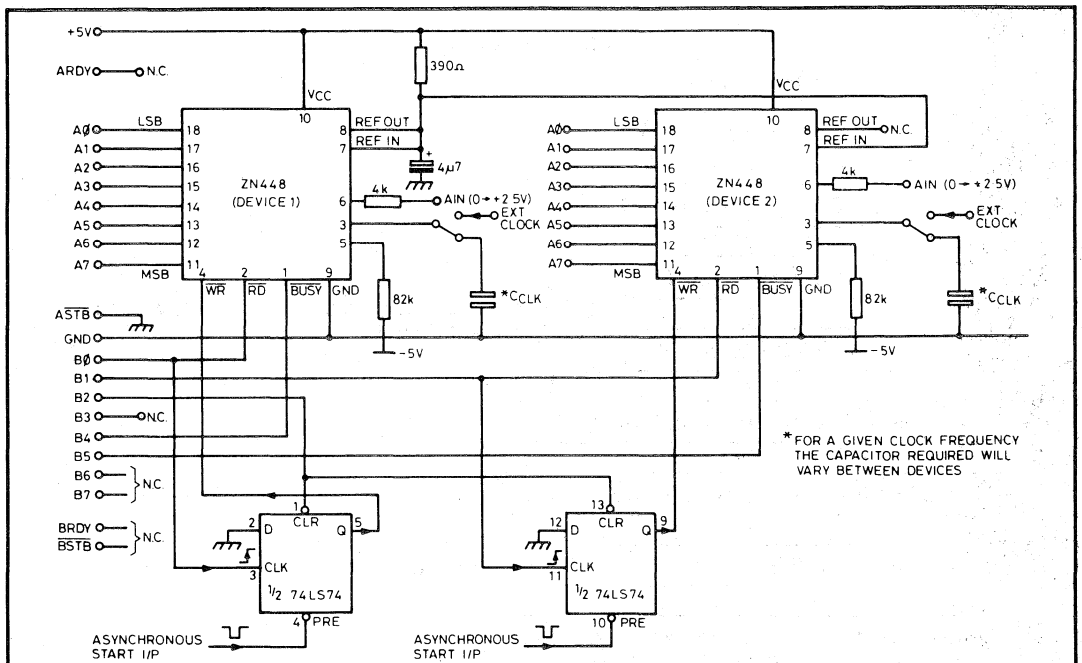



**Fig. 6 Interfacing 2 × ZN448's to the Z80 using both ports of a Z80 PIO - interrupt driven**

(Note that again one reference is used to drive both devices, as in the previous section).

In the circuit of Fig. 6, B2 is used to clear the $\overline{\text{BUSY}}$'s initially and the rising edge of the relevant $\overline{\text{RD}}$ signal is used to clear the $\overline{\text{BUSY}}$'s after servicing (as described below). Thus complying with the above requirements.

The falling edge of the asynchronous start input signal from the timing logic, forces the Q output high on the associated D-type flip-flop. Hence the $\overline{\text{WR}}$ input, which was previously low, is now taken high and this starts a conversion. At the end of the conversion the $\overline{\text{BUSY}}$ output goes high and this is used to generate our interrupt.

During the service routine, the $\overline{\text{RD}}$ input on a given device is taken low to enable the outputs, and then back high after the data has been latched into port A. Thus a $\overline{\text{RD}}$ positive edge is generated every time a device is read. This edge clocks a low through to the Q output on the appropriate D-type, and hence takes the relevant $\overline{\text{WR}}$ input and $\overline{\text{BUSY}}$ output low.

For correct clearing of the $\overline{\text{BUSY}}$'s and hence correct operation, the asynchronous start input signals must:

(i) be inactive (high) when the CLR inputs on the D-types (B2) are low initially.

(ii) have returned back high after initiating a conversion, before the associated $\overline{\text{RD}}$ positive edge occurs.

## PROGRAM EXAMPLE

This program vectors to an interrupt service routine on the occurrence of an interrupt. The service routine then reads and stores the data from the interrupting ZN448('s).

Conversion is initiated by the users timing logic and an interrupt is generated when one or more of the $\overline{\text{BUSY}}$ outputs goes high.

The $\mu$P is set to interrupt mode 2 as the ports are designed to be used with this mode. The contents of the I register and the port interrupt vector are combined by the $\mu$P to form a 16-bit vector. This vector is then used to look up the starting address of the interrupt service routine. The $\mu$P then loads the program counter with this address and continues program execution from this location.

## PROGRAM STATEMENTS

: It is assumed that the user initiates conversion correctly when required.

: It is assumed that both ports need initialising.

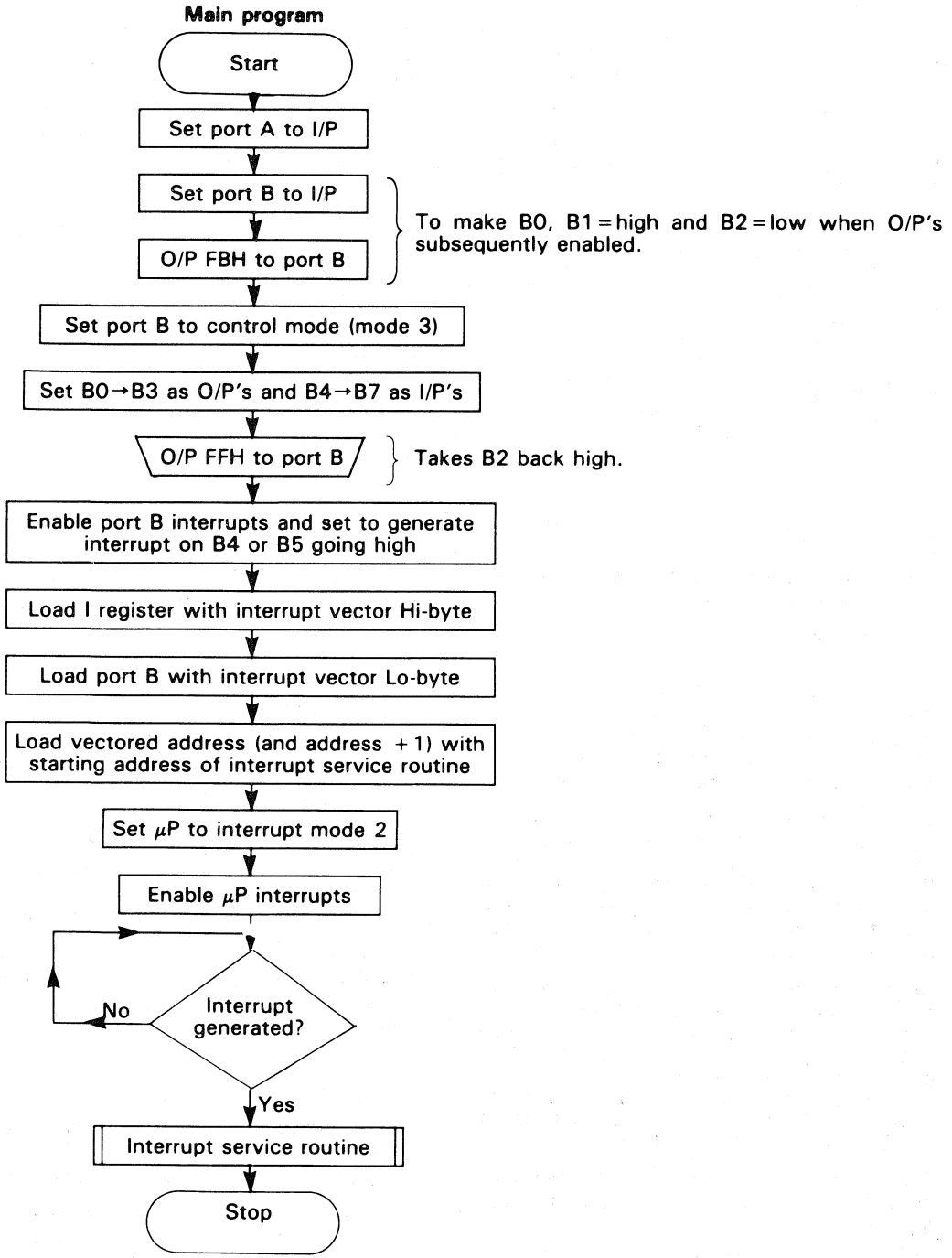
: Nominate memory locations for the vectored address, the interrupt service routine and for storing the conversion results.

: FEH = Select first ZN448 word.

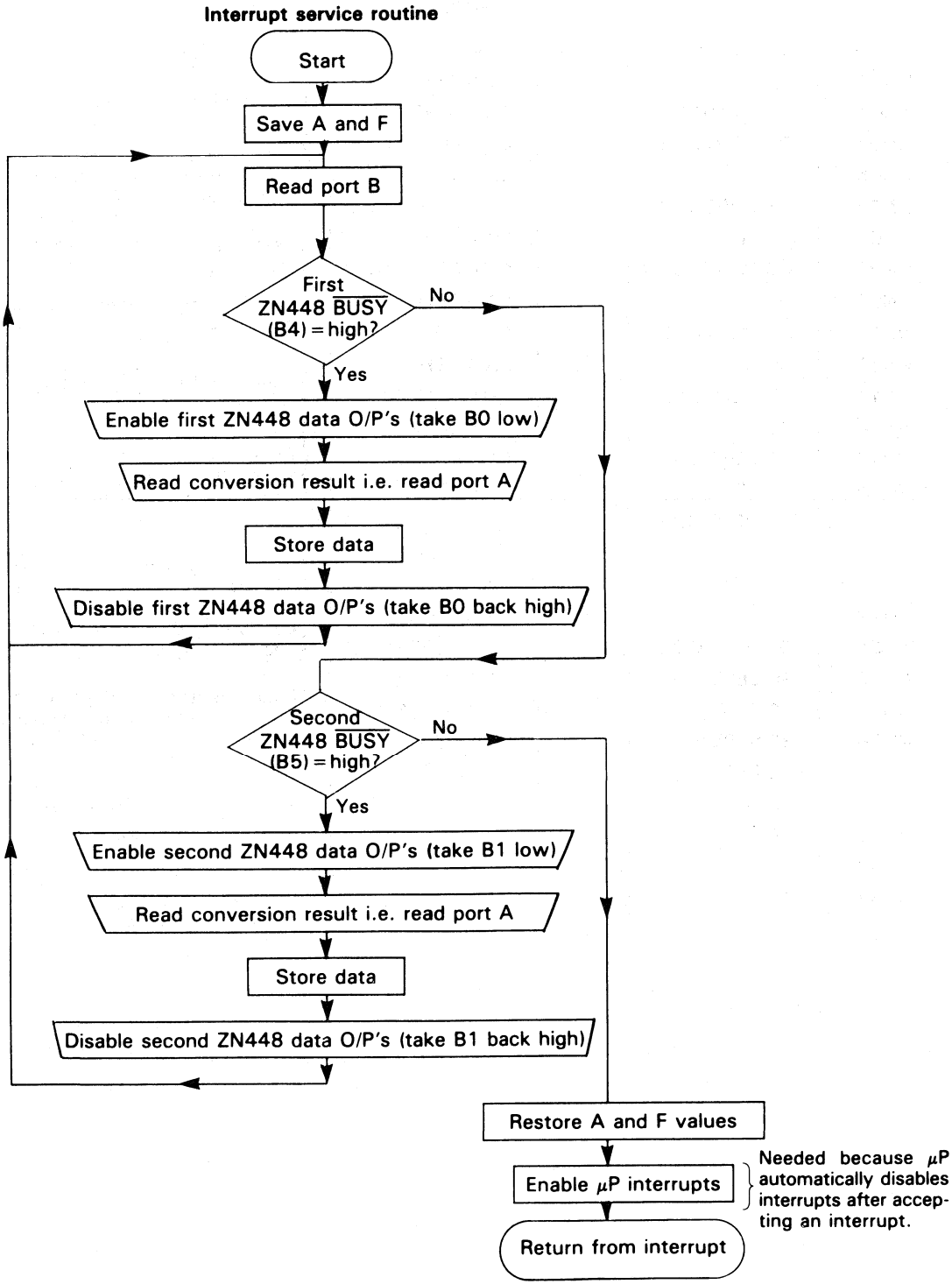
: FDH = Select second ZN448 word.

: FBH = Clear $\overline{\text{BUSY}}$ outputs word.

## FLOWCHART 4


Main program
Start
Set port A to I/P
Set port B to I/P
O/P FBH to port B
To make B0, B1 = high and B2 = low when O/P's subsequently enabled.
Set port B to control mode (mode 3)
Set B0→B3 as O/P's and B4→B7 as I/P's
O/P FFH to port B
Takes B2 back high.
Enable port B interrupts and set to generate interrupt on B4 or B5 going high
Load I register with interrupt vector Hi-byte
Load port B with interrupt vector Lo-byte
Load vectored address (and address + 1) with starting address of interrupt service routine
Set μP to interrupt mode 2
Enable μP interrupts
No
Interrupt generated?
Yes
Interrupt service routine
Stop

**FLOWCHART 4 (cont.)**



**PROGRAM LISTING**

**PROGRAM 4**

| Address | Object code | Label | Source code | Comments |
|---|---|---|---|---|
| NN00 | 3E 4F | | LD A,4FH | |
| NN02 | D3 PORTCO1 | | OUT PORTCO1,A | Sets port A to I/P (Mode 1) |
| NN04 | D3 PORTCO2 | | OUT PORTCO2,A | |
| NN06 | 3E FB | | LD A,FBH | Sets port B to I/P (mode 1) and sets CLR on D-types to go low when port O/P's enabled |
| NN08 | D3 PORTDA2 | | OUT PORTDA2,A | |
| NN0A | 3E CF | | LD A,CFH | |
| NN0C | D3 PORTCO2 | | OUT PORTCO2,A | Sets port B to control mode (mode 3) |
| NN0E | 3E F0 | | LD A,F0H | |
| NN10 | D3 PORTCO2 | | OUT PORTCO2,A | Sets B0→B3 as O/P's and B4→B7 as I/P's |
| NN12 | 3E FF | | LO A,FFH | |
| NN14 | D3 PORTDA2 | | OUT PORTDA2,A | Takes CLR on D-types back high |
| NN16 | 3E B7 | | LD A,B7H | |
| NN18 | D3 PORTCO2 | | OUT PORTCO2,A | |
| NN1A | 3E CF | | LD A,CFH | Sets port B to generate Int. on B4 or B5 going high, also enables port interrupts |
| NN1C | D3 PORTCO2 | | OUT PORTCO2,A | |
| NN1E | 3E IVECH | | LD A,IVECH | |
| NN20 | ED 47 | | LD I,A | Loads I reg. with interrupt vector Hi-byte |
| NN22 | 3E IVECL | | LD A,IVECL | |
| NN24 | D3 PORTCO2 | | OUT PORTCO2,A | Loads port B with interrupt vector Lo-byte |
| NN26 | 3E SERVL | | LD A,SERVL | |
| NN28 | 32 IVEC | | LD (IVEC),A | |
| NN2B | 3E SERVH | | LD A,SERVH | Loads vectored address (and next consecutive address) with starting address of interrupt service routine |
| NN2D | 32 IVEC + 1 | | LD (IVEC + 1),A | |
| NN30 | ED 5E | | IM 2 | Sets $\mu$P to interrupt mode 2 |
| NN32 | FB | | EI | Enables $\mu$P's interrupts |
| NN33 | 76 | | HALT | Waits for Interrupt (or reset!) |
| NN34 | ? | | ? | Returns to monitor (command(s) system dependant) |

**PROGRAM LISTING**

**PROGRAM 4 (cont.)**

**Interrupt service routine**

| Address | Object code | Label | Source code | Comments |
|---|---|---|---|---|
| MM00 | F5 | | PUSH AF | Saves current values of A and F |
| MM01 | DB PORTDA2 | POLL1 | IN A,PORTDA2 | Reads port B |
| MM03 | CB 67 | | BIT 4,A | Tests B4 and jumps if B4 = 0 |
| MM05 | 28 0F | | JR Z,POLL2 | |
| MM07 | 3E FE | | LD A,FEH | Selects first ZN448 |
| MM09 | D3 PORTDA2 | | OUT PORTDA2,A | |
| MM0B | DB PORTDA1 | | IN A,PORTDA1 | Reads and stores first ZN448 data |
| MM0D | 32 MEM1 | | LD (MEM1),A | |
| MM10 | 3E FF | | LD A,FFH | Puts first ZN448 O/P's back into high impedance state |
| MM12 | D3 PORTDA2 | | OUT PORTDA2,A | |
| MM14 | 18 EB | | JR, POLL1 | Jumps back to read port B |
| MM16 | CB 6F | POLL2 | BIT 5,A | Tests B5 and jumps if B5 = 0 |
| MM18 | 28 0F | | JR Z,RETURN | |
| MM1A | 3E FD | | LD A,FDH | Selects second ZN448 |
| MM1C | D3 PORTDA2 | | OUT PORTDA2,A | |
| MM1E | DB PORTDA1 | | IN A,PORTDA1 | Reads and stores second ZN448 data |
| MM20 | 32 MEM2 | | LD (MEM2),A | |
| MM23 | 3E FF | | LD A,FFH | Puts second ZN448 O/P's back into high impedance state |
| MM25 | D3 PORTDA2 | | OUT PORTDA2,A | |
| MM27 | 18 D8 | | JR, POLL1 | Jumps back to read port B |
| MM29 | F1 | RETURN | POP AF | Restores A and F values |
| MM2A | FB | | EI | Re-enables $\mu$P Int's. |
| MM2B | ED 4D | | RETI | Return from Int. |

**KEY:**

NN00 = Any Suitable starting address.
PORTCO1 = Port A control address.
PORTCO2 = Port B control address.
PORTDA1 = Port A data address.
PORTDA2 = Port B data address.
IVECL = Low byte of 16-bit interrupt vector (in port).
IVECH = High byte of 16-bit interrupt vector (in I Reg.).
IVEC = 16-bit interrupt vector formed by IVECH and IVECL.
IVEC + 1 = 16-bit address one location higher up in memory than IVEC.
SERVL = Interrupt service routine starting address-low byte.
SERVH = Interrupt service routine starting address-high byte.
MM00 = 16-bit starting address for interrupt service routine formed by SERVH and SERVL.
MEM1 = 16-bit address nominated for storing first ZN448 data.
MEM2 = 16-bit address nominated for storing second ZN448 data.
(Remember that the above 16-bit addresses need assembling in the order Lo-byte, Hi-byte in the object code).

## COMMENTS

The principles illustrated above can be extended to allow more ZN448's to be interrupt driven in this manner. Readily we can interface three ZN448's with each $\overline{RD}$ and $\overline{BUSY}$ allocated to their own port bit. Further if we clear the $\overline{BUSY}$ outputs by some method which does not use one of the port bits, we can interface four ZN448's. (For example we could pulse the CLR inputs low on the D-types, by writing to an address dedicated to this purpose).

It is important to realise that in the above example, the $\mu$P was not allowed to return from the service routing until both $\overline{BUSY}$'s were low simultaneously. This is to ensure that none of them remain high and inhibit further interrupts! Regardless of how many ZN448's are being interfaced, the same applies i.e. ensure that all $\overline{BUSY}$'s are low before returing from the service routine.

The software may need modifying to suit a particular hardware setup. If so, then in addition to the above, it should be ensured that the $\overline{BUSY}$ outputs are cleared initially and after device servicing.

The leakage current of the ZN448 three-state outputs need not concern us ($\pm 2\mu$A max. at 2V).

## FURTHER CONSIDERATIONS

Some sections of the above programs can be separated out and placed in the users initialisation routines i.e. they do not need repeating once proper initialisation has been achieved. Also the above programs were ended in some "return to monitor' commands. However in a real environment, sections of the programs will probably form part of a subroutine or loop, or part of a service routine.

The data acquired in the above examples was put straight into memory. It could instead have been processed and then either stored or outputted to another port.

In the examples given, where the $\overline{RD}$ inputs are controlled by port bits, these bits could be further decoded, thus extending their addressing range. This would also have the benefit of preventing the outputs from more than one device being enabled together (sould an erroneous word be accidentally written to that port).

Again when the ZN448 three-state outputs are controlled, various other devices can be connected to the port that reads the data. This port could also be swapped between input and output modes - provided proper control is exerted.

In the foregoing description, port A has been used for reading the data and port B for controlling/monitoring the ZN448's. These ports could be interchanged or could even be from different PIO's.

## SUMMARY

This report describes the versatility with which the ZN447/8/9 A-D converters can be interfaced with the Z80 $\mu$P. Clearly, there are many other ways of storing and processing the acquired data. The user can tailor these to suit her/his own particular requirements.

Most of the above principles can also be applied when interfacing the ZN447/8/9 to other popular $\mu$Ps.Full Engineering and Applications support is available to assist with technical queries relating to the applications of any of our data converter products.

# An Analog Output System for the Z80$\mu$P using the ZN558 8-Bit DAC

**This report is intended to illustrate how to interface the ZN558 8-bit D-A converter to a Z80 based microprocessor system using a Z80 PIO. Circuit diagrams and program examples are given to enable the user to get his interface system working. The following is equally applicable to the faster versions of the Z80 microprocessor and the Z80 PIO and also to the CMOS versions.**

**In order to keep this report concise it is assumed the reader is familiar with the Z80 system.**

## THE ZN558 D-A CONVERTER

The ZN558 is a monolithic 8-bit $\mu$P compatible D-A converter with input latches to facilitate updating from a data bus. It operates from a single +5V supply and is TTL and 5V CMOS compatible. The latch is transparent when $\overline{\text{enable}}$ is LOW and the data is held when enable is taken HIGH. The ZN558 also contains a 2.5V reference the use of which is pin optional to retain flexibility. An external reference may therefore be substituted.

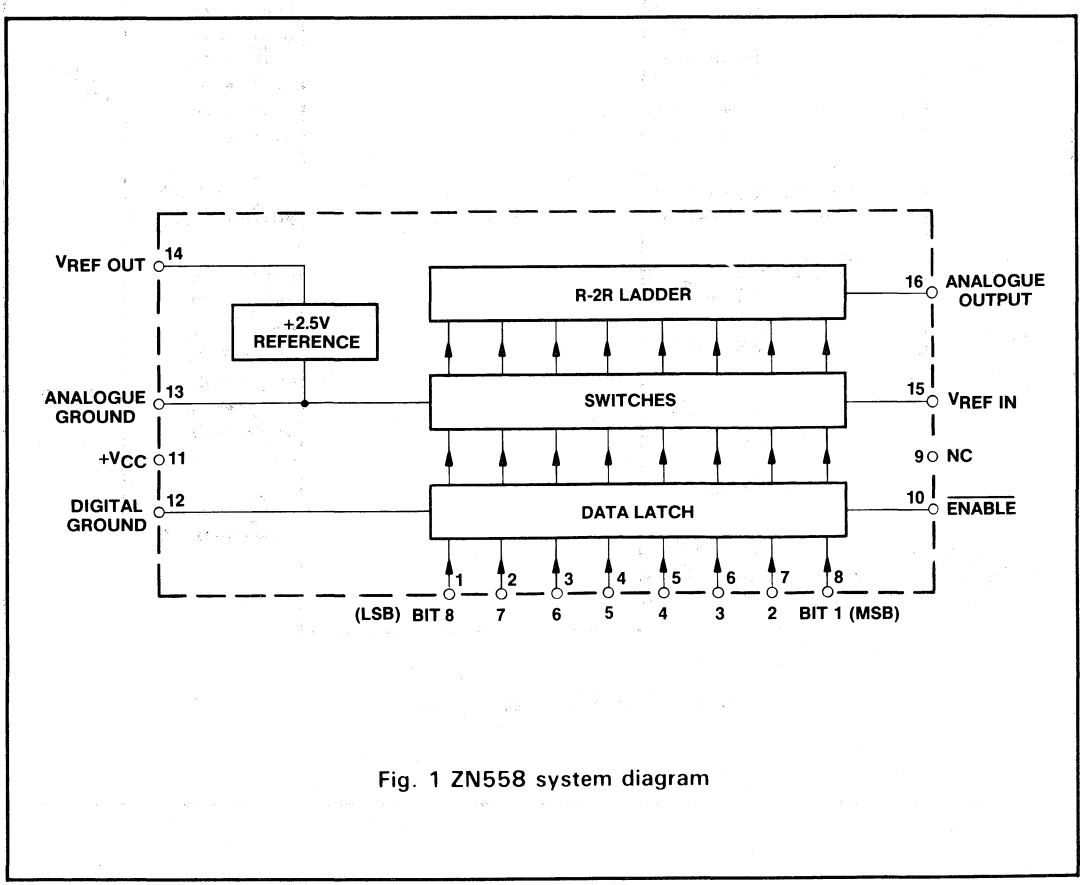



Fig. 1 ZN558 system diagram

The typical worst case settling time for the ZN558 is 1.25$\mu$s and the typical 1LSB major transition settling time is 800ns.

Further information including suitable analogue output buffering circuits can be obtained from the data sheet.

### Z80 PIO

The Z80 PIO is a programmable two port device which provides a TTL compatible interface between peripheral devices and the Z80 CPU. It is capable of interfacing directly to the CPU without any external logic. The two 8-bit, bidirectional ports, each have two handshake lines (RDY and $\overline{STB}$) for use when transferring data to or from peripherals. Either port or indeed any port bit, can be programmed to act as an input or output.

This is a very brief introduction to a very complex device. Further information can be obtained from the manufacturers data.

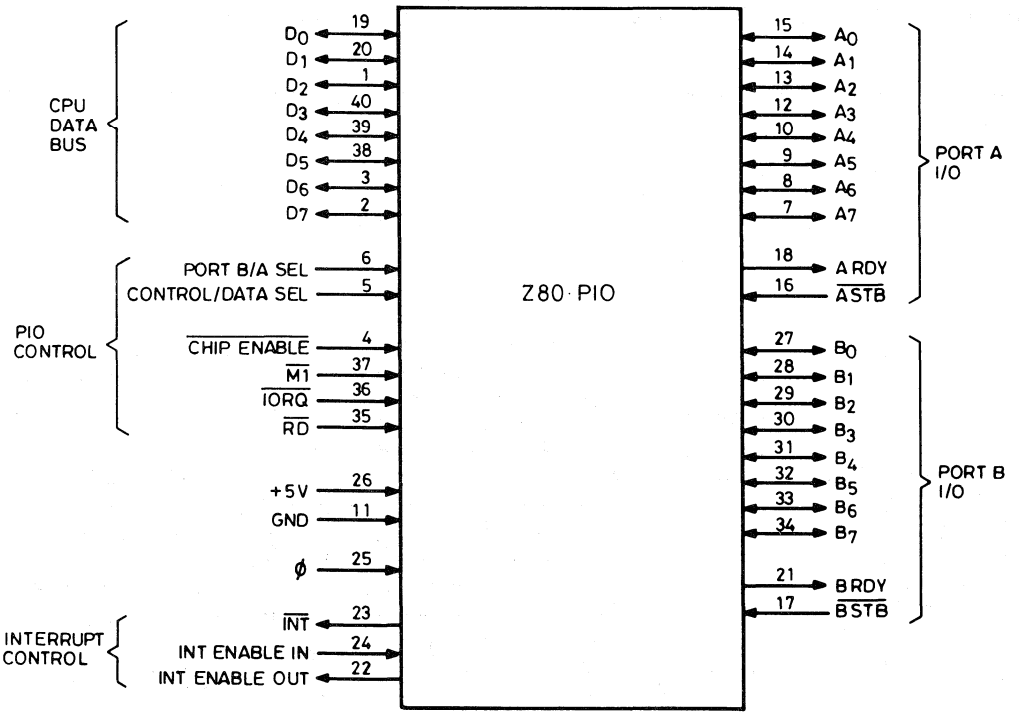



Fig. 2 Z80 PIO - pinning diagram

## INTERFACING A SINGLE ZN558 D-A TO THE Z80

If the Z80 is required to interface to only one ZN558, this can be achieved with a single port (outputting data to the ZN558), if the enable input is tied LOW.

With $\overline{\text{enable}}$ tied LOW, the ZN558 will convert whatever is presented to its inputs at all times. The circuit diagram for this arrangement is as follows:

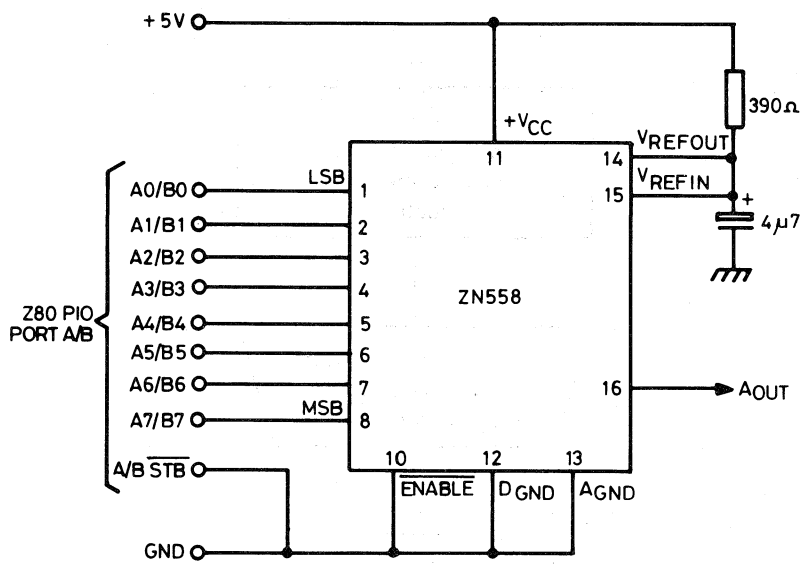



Fig. 3 Circuit diagram for interfacing a single ZN558 to the Z80

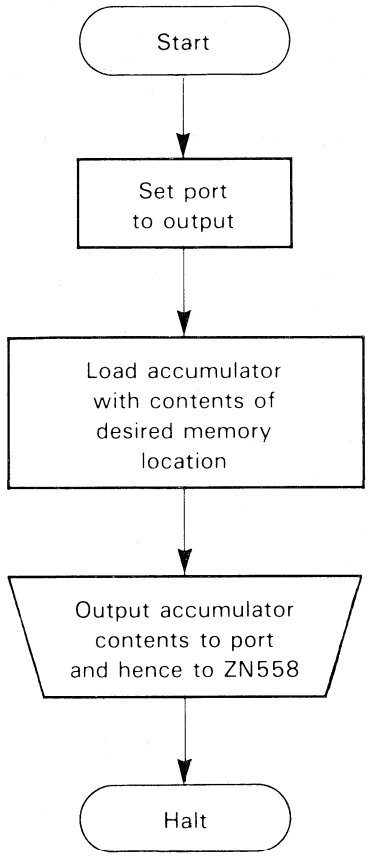
## PROGRAM EXAMPLE

This is a program to read the contents of a memory location - which has been previously loaded with the desired data - and subsequently output this data to the ZN558 via one of the Z80 PIO ports.

## PROGRAM - STATEMENTS

:It is assumed that the port is in the reset state:
:Load desired memory location with required data:

## PROGRAM FLOWCHART




## PROGRAM LISTING

| Address | Object code | Source code | Comments |
|---|---|---|---|
| NN00 | 3E 0F | LD A, 0FH | Sets port to O/P (mode 0). |
| NN02 | D3 add1 | OUT add1, A | |
| NN04 | 3A YZ WX | LD A, (WXYZ) | Loads acc. with the desired data from the specified memory location. |
| NN07 | D3 add2 | OUT add2, A | O/P's acc. contents to port and hence to ZN558 |
| NN09 | 76 | HALT | Halts processor. |

## NOTES

NN00 = Any convenient starting address
add1 = Port control address
add2 = Port data address
WXYZ = MEMORY LOCATION which has been previously loaded with data, where WX = HI-address byte and YZ = LO-address byte.

## COMMENTS

This arrangement has the advantage of simplicity and is useful where a port can be dedicated to this purpose.

The data in the above example was obtained from the designated memory location. This Data could instead have been read in from some port and maybe processed before subsequently being outputted to the ZN558.

## INTERFACING ONE OR MORE ZN558's TO THE Z80

The general arrangement for interfacing several ZN558's to a Z80 system is shown in the following diagram.

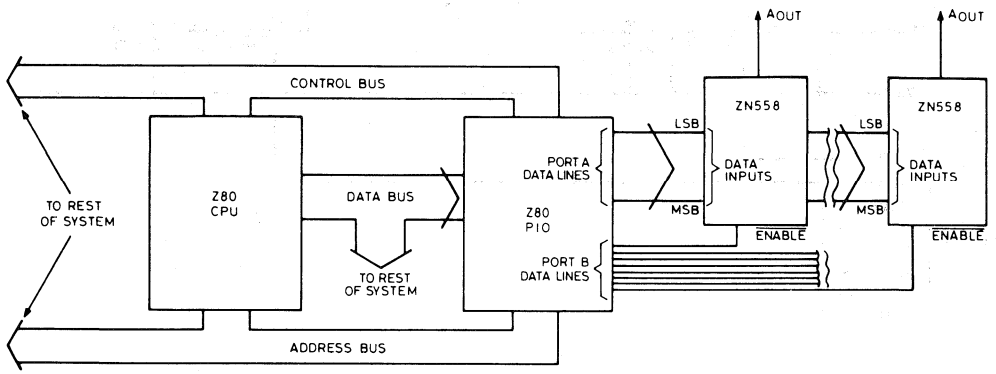



**Fig. 4 Interfacing several ZN558's to the Z80 - schematic diagram**

Here the ZN558 data inputs are connected to the data lines from one port and the enable inputs are controlled with the data lines from another port. These lines are taken LOW individually when it is required to make one of the ZN558's read the data presented to its inputs. The relevant line can then be taken back high to latch this data. This arrangement allows the ZN558's to be addressed or selected individually and ignore the data the rest of the time.

The data set-up and hold times and the $\overline{\text{enable}}$ pulse width need not be considered since they are much less than the Z80 instruction execution times.

A circuit diagram and program example for interfacing to two ZN558's follows. This implementation can easily be extended if more ZN558's are required:

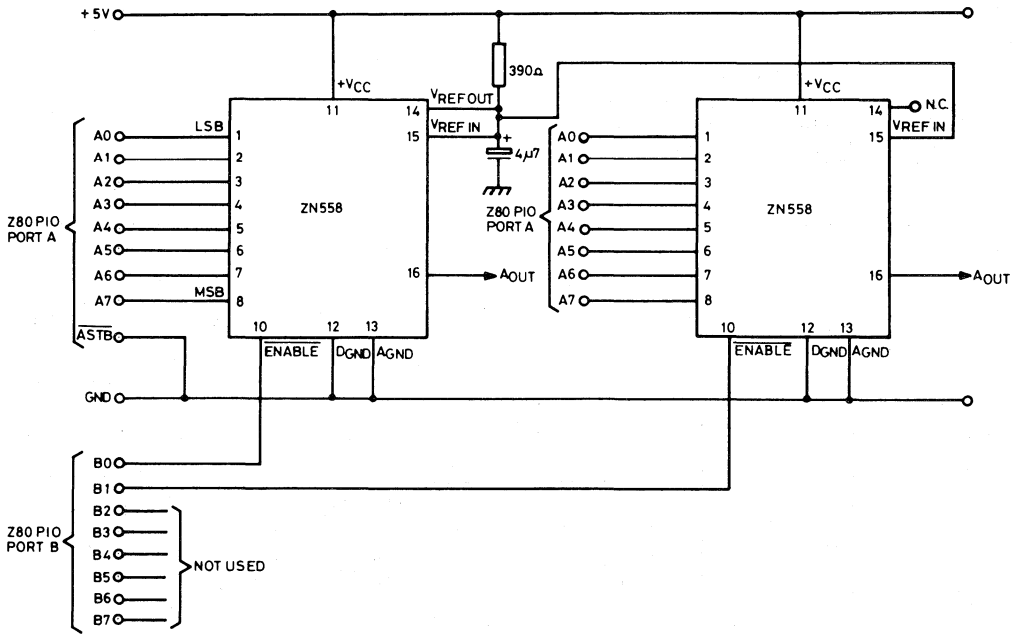



**Fig. 5 Circuit diagram for interfacing two ZN558's to the Z80 - latching controlled by port B**

Note that in the above diagram, the reference input ($V_{REF\ IN}$) of the second ZN558 is driven from the reference output ($V_{REF\ OUT}$) of the first ZN558. This provides excellent gain tracking between the converters. Up to five ZN558's may be driven from a single internal reference without having to change the reference resistor ($R_{REF}$).

## PROGRAM EXAMPLE

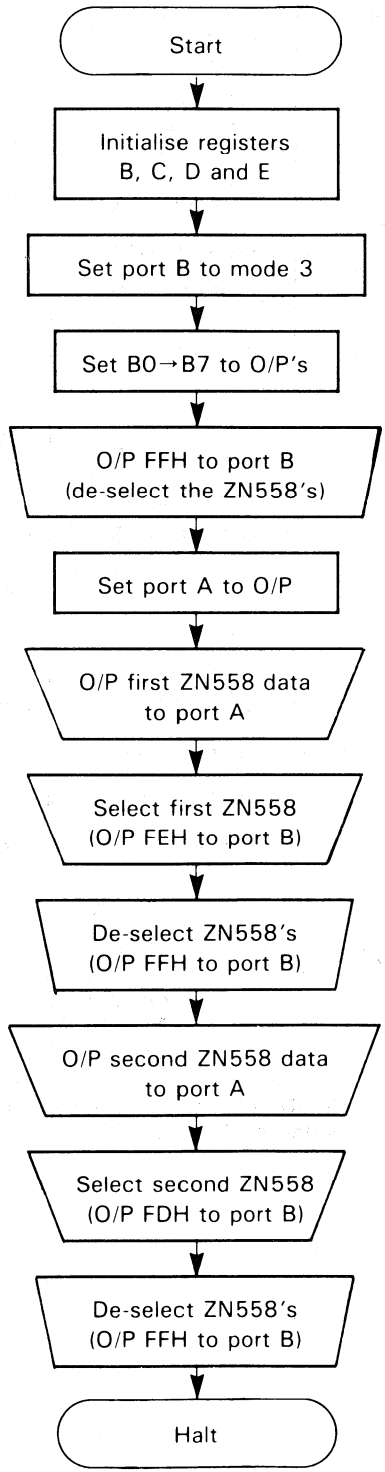
This is a program to write different data to two ZN558's. Port A is used for writing the data and port B is used to select the relevant ZN558.

Some of the Z80 registers are being used to hold the select and de-select words and to hold the port B data address.

## PROGRAM - STATEMENTS

:It is assumed that the port is in the reset state:
B0 connected to enable on first ZN558
B1 connected to the enable on second ZN558
C REGISTER = Port B data address
D REGISTER = De-select ZN558's word (FFH)
E REGISTER = Select first ZN558 word (FEH)
B REGISTER = Select second ZN558 word (FDH)

## PROGRAM FLOWCHART



**PROGRAM LISTING**

| Address | Object code | Source code | Comments |
|---|---|---|---|
| NN00 | 06 FD | LD B, FDH | Initialises registers B,C,D & E |
| NN02 | 0E add1 | LD C, add1 | |
| NN04 | 16 FF | LD D, FFH | |
| NN06 | 1E FE | LD E, FEH | |
| NN08 | 3E CF | LD A, CFH | Sets port B to mode 3 |
| NN0A | D3 add2 | OUT add2, A | |
| NN0C | 3E 00 | LD A, 00H | Sets B0→B7 to O/P's |
| NN0E | D3 add2 | OUT add2, A | |
| NN10 | ED 51 | OUT (C), D | O/P's FFH to port B i.e. de-selects ZN558's |
| NN12 | 3E 0F | LD A, 0FH | Sets port A to O/P's |
| NN14 | D3 add3 | OUT add3, A | |
| NN16 | 3E data1 | LD A, data1 | O/P's first ZN558 data to Port A |
| NN18 | D3 add4 | OUT add4, A | |
| NN1A | ED 59 | OUT (C), E | Selects first ZN558 |
| NN1C | ED 51 | OUT (C), D | De-selects ZN558's |
| NN1E | 3E data2 | LD A, data 2 | O/P's second ZN558 data to Port A |
| NN20 | D3 add4 | OUT add4, A | |
| NN22 | ED 41 | OUT (C), B | Selects second ZN558 |
| NN24 | ED 51 | OUT (C), D | De-selects ZN558's |
| NN26 | 76 | HALT | HALTS processor |

**NOTES**

NN00 = Any convenient starting address
add1 = Port B data address
add2 = Port B control address
add3 = Port A control address
add4 = Port A data address
data1 = Data to first ZN558 (selected by B0)
data2 = Data to second ZN558 (selected by B1)

**COMMENTS**

As previously stated this principle can be extended to address additional ZN558's if required. The enable inputs on these other ZN558's being connected to the desired port B data bits. Each port bit can then be taken low individually as required - by writing different select words to the port - to address the relevant ZN558.

The relevant D.C. characteristics for the ZN558 and the Z80 PIO are shown in the following table:

| Z80 PIO - CMOS | Z80 PIO - NMOS | ZN558 |
|---|---|---|
| $V_{OH} = 2.4V$ min. when $I_{OH} = -1.6mA$ | $V_{OH} = 2.4V$ min. when $I_{OH} = -250\mu A$ | $I_{IH} = 20\mu A$ max. when $V_{IH} = 2.4V$ |
| $V_{OL} = 0.4V$ max. when $I_{OL} = 2mA$ | $V_{OL} = 0.4V$ max. when $I_{OL} = 2mA$ | $I_{IL} = -5\mu A$ max. when $V_{IL} = 0.4V$ |

**TABLE 1 ZN558 AND Z80 PIO - D.C. CHARACTERISTICS**

In some applications, it may be undesirable to use the Z80 registers as above i.e. to hold the ZN558('s) and port addressing words. If this is the case, these instructions can easily be substituted with:

```
LD A, byte
OUT address, A
```

as have been used in other parts of the program.

## FURTHER CONSIDERATIONS

In the above examples the port used for outputting the data byte is set to mode 0. However for our purpose we do not need the handshake lines (RDY and $\overline{STB}$). Therefore the RDY line is ignored and the $\overline{STB}$ line is tied low (to prevent any spurious transitions). If preferred this port could be set to mode 3 with all the bits set as outputs (here RDY is held LOW and $\overline{STB}$ is inhibited internally).
In addition to connecting the ZN558('s) to the data port, it may be required to connect a peripheral that will utilise the handshake lines (obviously the ZN558('s) will have to be selected only when required, to ignore unwanted data). Here it is up to the user to ensure that this other peripheral ignores the handshake lines when data is written to the ZN558('s) e.g. gate RDY and possibly $\overline{STB}$ with lines from the addressing port. Further, addressing the ZN558('s) as above allows the data port to be swapped between input and output modes.

Above port A has been used for outputting the data and port B used for addressing the ZN558's. This need not be the case, the ports could be swapped round or even be from different PIO's.

Also the programs given above have been terminated with the HALT command. For evaluation purposes this could be replaced for example with some command(s) that will return control to the monitor. In practice the program used will probably form part of a subroutine or loop.

## SUMMARY

The foregoing describes the ease with which the ZN558 can be interfaced to the Z80 microprocessor. Clearly, many other variations are possible on loading, processing and outputting the data and the user can tailor these to suit his own particular requirements.

Further the above principles can easily be extended to allow the ZN558 to be interfaced to other popular microprocessors.

# A 3-Wire Microcontroller Interface for the ZN509 ADC

AN101

**The following is intended to demonstrate the ease with which the ZN509 8-bit serial output analog-to-digital converter can be interfaced to any microcontroller with standard I/O ports. In this example, the 68705 P3, with on chip EPROM, from the 6805 family of microcontrollers has been chosen.**

## CIRCUIT DESCRIPTION

The data converter is operated in single shot mode. The CHIP SELECT and CLOCK lines are under software control. Serial data is collected via a standard port line and manipulated internally to reconstruct an eight-bit word.

## PROGRAM DISCUSSION

The CHIP SELECT and CLOCK lines are connected to port C. After reset, the ports are initialised as inputs. Port C 'data register' is loaded with '1's prior to being initialised as an output. This avoids the possibility of an unwanted conversion being triggered by initial undefined port levels.

In the example program, a clock pulse is generated by decrementing and incrementing port C because this is slightly faster than the bit set/clr instruction but this could easily be used instead.

Data is loaded from port B into the accumulator and rotated right into the carry flag. The carry is then rotated left into a memory location. After each data bit is read, the software generates a new clock pulse in order to continue the conversion.

This routine is then repeated until the full eight-bit conversion result is contained in the nominated memory location.

Once the last data bit has been acquired, an extra clock pulse is generated in order to complete the ZN509 conversion sequence.

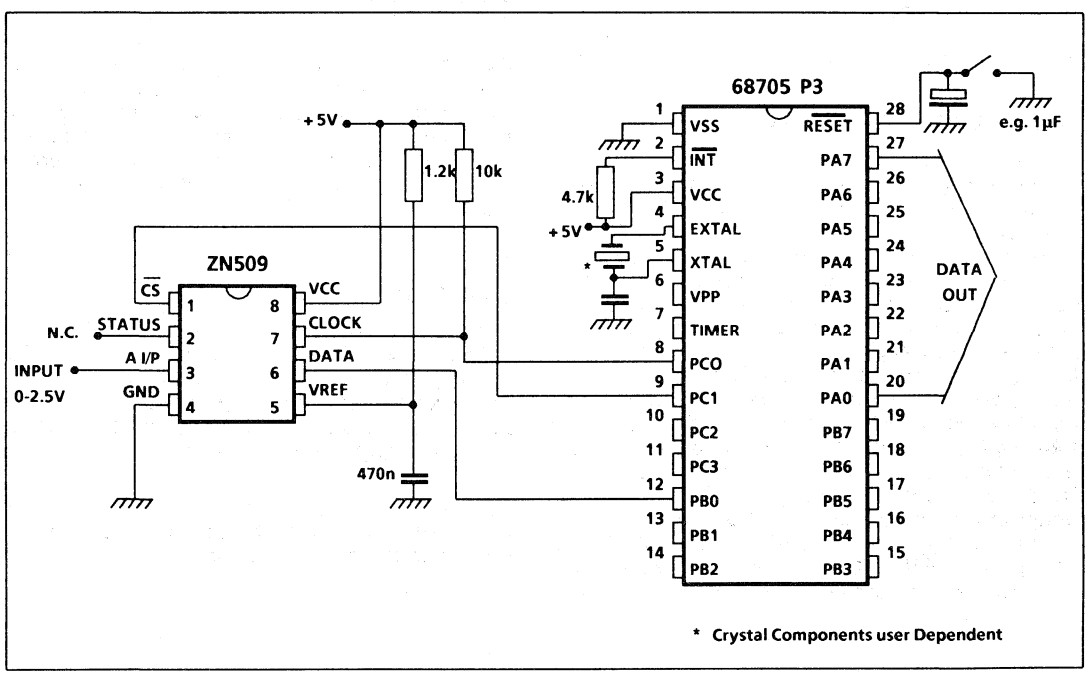



*Fig.1. Complete circuit diagram for minimum configuration in single shot mode.*

Since this program is intended for demonstration purposes, the conversion result is output via port A for testing and the program loops to provide repeated single shot conversions.

The ZN509 is capable of performing a conversion in 8μs. However, this is too fast for the microcontroller to read directly without any additional hardware.

The execution time of the 'converting' part of this program is 311 machine cycles. The limiting factor here is the instruction execution times of the microcontroller. Any software controlled conversion is inherently slow, but the simple hardware offered here is very appealing.

Note that the conversion time can be almost halved, by using one of the eight bit ports instead of a memory location as a shift register and writing out the program longhand instead of looping round.

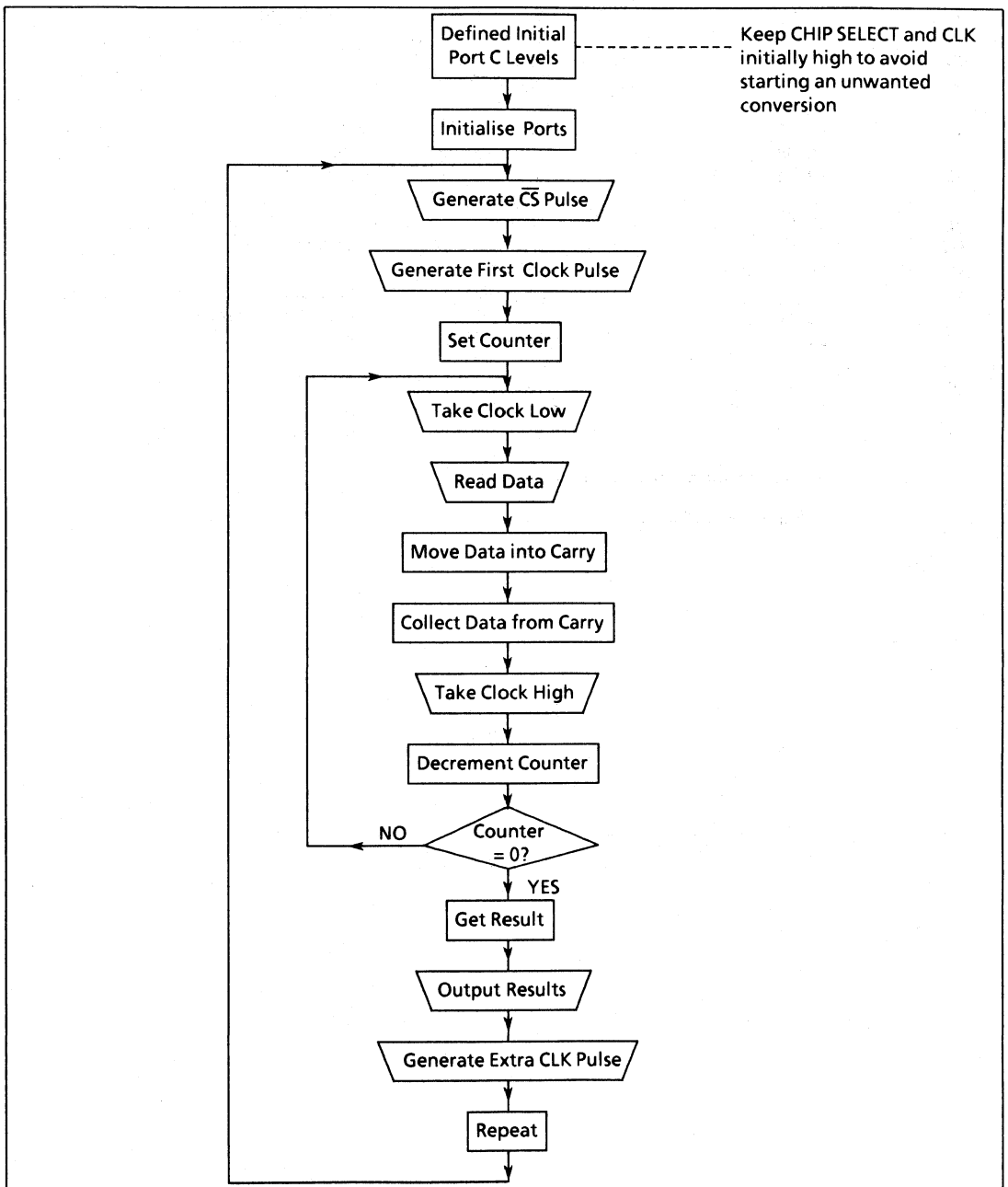



*Fig.2 .Example Program FlowChart*

## EXAMPLE PROGRAM LISTING

| ADDRESS | OBJECT CODE | LABEL | SOURCE CODE | COMMENT |
|---|---|---|---|---|
| 0100 | A6 FF | | LDA #SFF | |
| 02 | B7 02 | | STA PORT C | Define inital port C levels |
| 04 | B7 04 | | STA DDRA | Port A = output |
| 06 | B7 06 | | STA DDRC | Port C = output |
| 08 | 3F 05 | | CLR DDRB | Port B = input |
| 0A | 13 02 | START | BCLR C,1 | Toggle Chip Select |
| 0C | 12 02 | | BSET C,1 | |
| 0E | 3A 02 | | DEC PORT C | Clock low |
| 10 | 3C 02 | | INC PORT C | Clock high |
| 12 | AE 08 | | LDX #$08 | Set counter |
| 14 | 3A 02 | NEXT | DEC PORT C | Clock low |
| 16 | B6 01 | | LDA PORT B | Get data bit |
| 18 | 46 | | ROR ACC | Move data into carry |
| 19 | 39 10 | | ROL $10 | Relocate data in memory |
| 1B | 3C 02 | | INC PORT C | Clock high |
| 1D | 5A | | DEC X | |
| 1E | 26 F4 | | BNE NEXT | Get next bit |
| 20 | B6 10 | | LDA $10 | Get result from memory |
| 22 | B7 00 | | STA PORT A | Output result |
| 24 | 3A 02 | | DEC PORT C | Extra clock pulse |
| 26 | 3C 02 | | INC PORT C | |
| 28 | CC 010A | | JMP START | Repeat |
| 07FE | 01 00 | | | Reset vector |

# Signifies immediate addressing mode

$ Signifies hexadecimal

# Fibre Optic Components for use with 50 and 200 Mbit Chips

AB21

**The choice of optical component for a given application will be determined by a number of factors. The most important of these are wavelength, bandwidth and power output (for LEDs) or capacitance (for PIN diodes). The tables below detail these characteristics for a number of LED and PIN diodes from various manufacturers. The following notes explain how bandwidth should be determined.**

### 50 MBIT CHIP SET

The 50 MBit chip set comprises th SL9901 Transimpedance Amplifier, SP9921 Manchester Decoder and SP9960 Manchester Encoder/ LED Driver. For these devices, select a component with a bandwidth at least equal to 1.4 times the application bit rate.

### 200MBIT CHIP

For the SP9944E 200 Mbit Data Regenerator, select a component with a bandwidth at least equal to 0.7 times the application bit rate being used. If a coding system is used this will have to be divided by the efficiency of the code, as shown in the example below :

Data is 100 Mbits Manchester code (50% efficient)

$$BW_{MIN} = (0.7 \times 100 \div \frac{50}{100} = 140MHz$$

where $BW_{MIN}$ is minimum bandwidth of optical component

### LEDS (810-900 nm)

| Manufacturer | Type No. | Wavelength (nm) | Power O/P ($\mu$W) (into core size in $\mu$m) | Bandwidth (MHz) |
|---|---|---|---|---|
| Motorola | MFOE1200 | 820 | 60 (200) | 70 |
| Motorola | MFOE1100 | 815 | 60 (100) | 20 |
| Motorola | MFOE1101 | 815 | 120 (100) | 20 |
| Motorola | MFOE1102 | 815 | 180 (100) | 20 |
| Motorola | MFOE1201 | 815 | 60 (100) | 100 |
| Motorola | MFOE1202 | 815 | 100 (100) | 100 |
| Honeywelll | HFE4020-012 | 850 | 60 (100) | 80 |
| Honeywell | HFE4020-013 | 850 | 100 (100) | 80 |
| Honeywell | HFE4000-012 | 850 | 60 (100) | 80 |
| Honeywell | HFE4000-013 | 850 | 140 (100) | 80 |
| Honeywell | HFE4000-014 | 850 | 100 (100) | 80 |
| Honeywell | HFE4003-023 | 850 | 200 (100) | 120 |
| Texas Opto | TOX 9011/2 | 840 | 5-45 (50) | 50 |
| Abb-Hafo | 1A1742 | 860 | 110 (85) | 40 |
| Abb-Hafo | 1A148A | 860 | 40 (50) | 50 |
| Abb-Hafo | 1A18A | 895 | 25 (50) | 115 |
| Abb-Hafo | 1A184A | 895 | 40 (50) | 115 |

### PIN DIODES (820-860 nm)

| Manufacturer | Type No. | Wavelength (nm) | Capacitance (pF) | Bandwidth (MHz) |
|---|---|---|---|---|
| Honeywell | SD3322 | 820 | 1.5 | 125 |
| Abb-Hafo | 1A211 | 860 | 5.0 | 70 |
| Mitsubishi | PD2101 | 850 | 5.0 | 150 |
| Motorola | MFOD1100 | 820 | 2.5 | 250 |
| Siemens | SFH202A | 850 | 3.0 | 100 |
| Siemens | SFH2012A | 850 | 3.0 | 100 |

# A new approach to Comparator Design



**When launched in the 1970s, the SP9687 was regarded as 'state of-the-art'. With switching times of less than 3ns, other manufacturers were not easily able to supply similar products. However, market needs mean that there is now a need to supply a range of sub-nanosecond comparators.**

The Dual (SP93802), Quad (SP93804) and Octal (SP93808) comparators have been specially designed for systems that require low propagation delay and ultra fast switching, with minimum power consumption.

To achieve the above, some of the systems design approaches had to be re-examined, to create a device with the optimum speed versus power.

Originally it was decided that the new range of comparators needed the capabilities of both latched and transparent modes of operation. In transparent mode the output simply changes its state when the differential inputs cross each other. The latched mode of operation is more subtle as it will only change its output when a sample pulse is applied. This creates the ability to sample an input voltage at a known instant in time.

When used in the transparent mode the new range of comparators have low gain. Gain is one of the most important factors often ignored by the systems designers when using comparators.

Take a standard high speed comparator system used in transparent mode as shown in Fig. 1.

A standard comparator has a gain of 50dB or more. This gain figure also applies to the line receiver that follows the comparator. If we now calculate the actual minimum gain required for a full ECL output from our system for, say, a 10mV input ONLY x160 (equivalent to +40dB) is required AND NOT x100000 (+100dB) that is commonly provided.

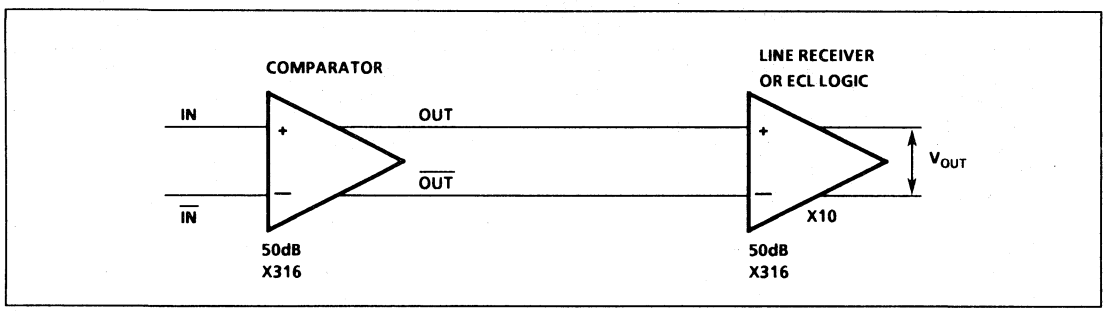



*Fig.1 Standard system*

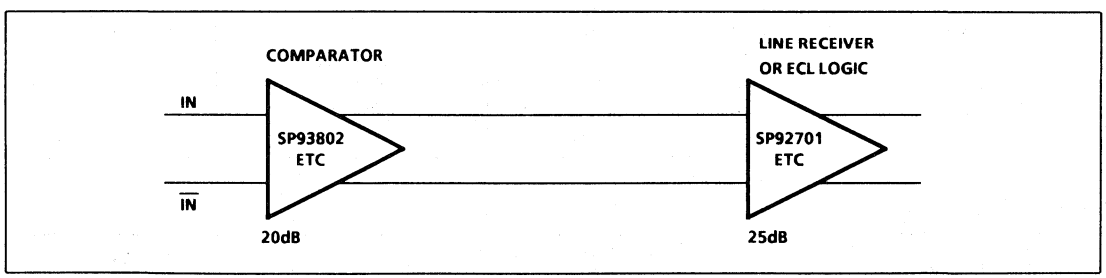



*Fig. 2 Lower gain distributed within system*

By optimising the gain to a lower value, we have reduced the system propagation delay, and hence reduced the effects of variation in propagation with temperatures and signal conditions.

This philosophy has been implemented within the new range of comparators to produce outstanding signal capture performance.

The lower gain also allows these new comparators to be used as linear amplifiers when the latch is held in transparent mode. When the latch function is used the gain of the device is regenerated, for fast accurate acquisition of the input at the desired sample time.

Another unique feature of these new comparators is the addition of a fast glitch capture latch. This latch continuously monitors the output of the comparator when used in transparent mode. The latch is set when the inputs cross and stays set until an external reset is applied. This is not only ideal for logic analysers but also many other applications where the timing of the input signal is unknown.

## THE GEC SEMICONDUCTORS RANGE OF SUB-NANOSECOND COMPARATORS

**SP93802 B DG** (Dual-in-line) Dual comparator
**SP93802 B HG** (Quad Cerpac) Dual comparator
**SP93804 B HG**(Quad Cerpac) Quad comparator
**SP93808 B HG**(Quad Cerpac) Octal comparator

### FEATURES

- -40°C to +85°C Temperature Range
- Typical delay < 1ns
- Glitch Capture 20mVns (Typ)
- On Chip Band Gap Reference Circuitry
- 50 Ohm Drive Capability
- On Chip Clock Buffers
- Channel Propagation Delay Matching < 100ps
- High Input Impedance

### APPLICATIONS

- Automatic Test Equipment
- Instrumentation
- Line Receiver/Driver
- Cascadable Differential Amplifier
- Analog to Digital Conversion
- Fibre Optics
- Logic Analysers

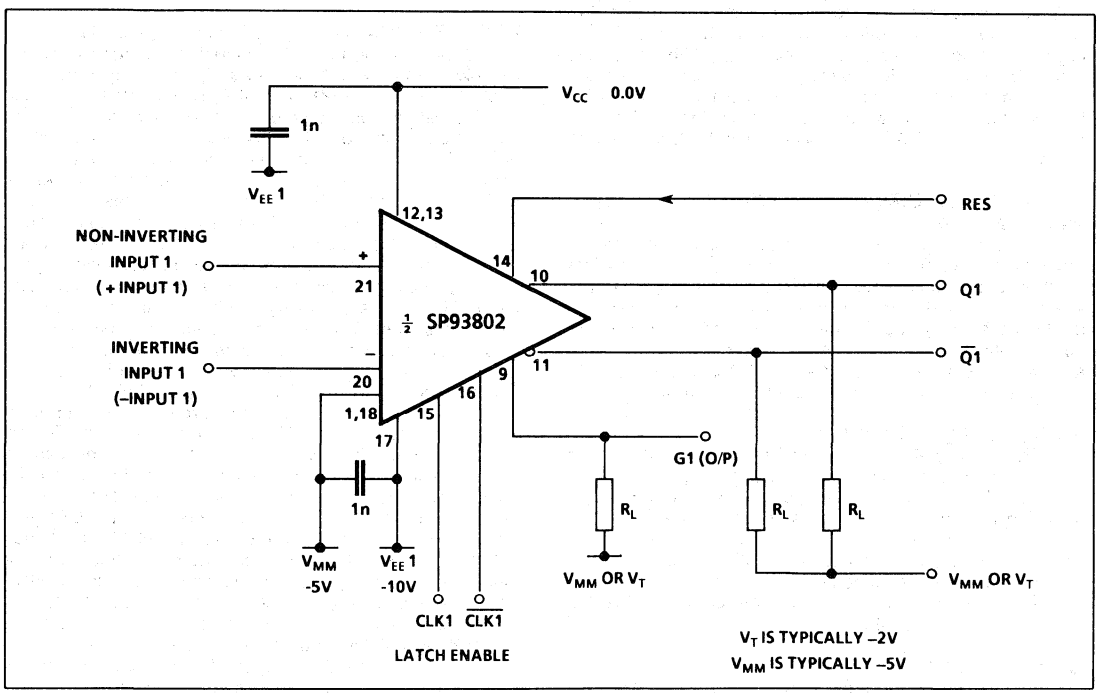



*Fig. 3 Application circuit, one channel. (Pin numbers refer to Quad Cerpac package)*

# 50MB/s Fibre Optic Video System

## SYSTEM DESCRIPTION

The system operates with a standard 1V p-p composite video signal and digitises this into 4 bits at a sampling rate of 10MHz. A fifth bit, which is permanently connected to logic '1', is added and acts as a frame signal. The 5-bit parallel signal is converted to a serial bit stream and sent over a fibre optic link at 50MB/s using the 50MB/s chip set. These chips use Manchester Biphase-Mark encoding for transmission and the receiver incorporates its own phase locked loop for clock recovery. The frame format of the transmission is:

F : D0 : D1 : D2 : D3

where D3 is the most significant bit.

A sampling rate of 10MHz allows all frequencies below 5MHz to be digitised, which is adequate for monochrome signals; with colour signals some of the colour information is attenuated.

At the receive end, the signal is recovered using a PIN diode and a transimpedance amplifier. After decoding, the signal undergoes a serial-to-parallel conversion. Frame alignment is accomplished by detacted the fifth bit (always logic '1'). During the video sync period the ADC transmits a 0000 pattern and it is possible to detect the frame during this period. The 4-bit words are then sent to a Digital-to-Analog converter (DAC) and reconstructed into a standard video signal.

## TRANSMITTER CIRCUIT DESCRIPTION (FIG. 1)

### Video Amplifier

An SL9999 high speed operational amplifier is used to drive the SP94308 ADC. An anti-aliasing filter with a –3dB point at approximately 7MHz is incorporated to filter the video input signal. The amplifier operates in non-inverting mode and has a gain of 2, which is reduced to unity by the 75Ω output/input resistors. When laying out the SL9999 amplifier, it is advisable to refer to the application notes in the datasheet as this device is sensitive to layout.

### Analog-to-Digital Converter

Although only 4 bits are required, the SP94308 8-bit ADC is used in this system because it has been specifically designed for video A-D applications with a maximum sampling rate of up to 20MHz. A separate circuit using an SL3145 transistor array recovers the sync pulse from the video signal ; this pulse causes the ADC to stop conversion and produce an all zeros code.

For further applications information on the SP94308, refer to AN52 on page 4-23.

### Clock Generator

A 10MHz crystal controlled clock is used to drive the ADC; for the remaining serial logic, this clock is multiplied to 50MHz using the phase locked loop (PLL) of the SP9921. This chip has an ECL output which is converted to TTL levels by a Motorola MC10H125.

### Parallel-to-Serial Conversion

The 4-bit output of the ADC is converted to serial form by the 74F299 shift register. Data is loaded into the register when $S_1$ is high and shifted out on $Q_7$ when $S_1$ is low.

The $S_1$ signal is generated at the output of the clock synchroniser and pulse generator circuit. Serial data from the 74F299 is clocked into the optical transmitter at 50MB/s.

### Optical Transmitter

The SP9960 Fibre Optic Transmitter chip internally encodes the TTL data input into Manchester Biphase-Mark code. This code generates clock related transitions such that there is always a transition at the bit boundary; a logic '1' is coded as a transition in the centre of the bit time slot, a logic '0' as no transition. The SP9960 has a built in constant current LED driver which can be used to drive most commercially-available fibre optic LEDs. It is important that the rise and fall times of the LED is <6ns; the Honeywell HOR4023-A33 is an 850nm Led that meets these requirements. Drive current for the LED can be pin-selected from 15mA to 150mA (refer to the SP9960 datasheet).

## RECEIVER CIRCUIT DESCRIPTION (FIG. 2)

Regeneration of the optical signal is performed using a PIN diode and the 50MB/s Fibre Optic Receiver pair, the SL9901 and the SP9921. The SL9901 is a transimpedance amplifier with a typical gain of 40kΩ. This amplifier converts the photo-current from the PIN diode into a voltage at its output. A PIN diode with a capacitance <5pF and response time <5ns should be used. Decoding and clock recovery is performed by the SP9921, which incorporates two PLLs. The first PLL is used as a reference, while the second performs the clock recovery from the Manchester encoded data. The reference PLL sets the centre frequency of the recovery PLL and requires a clock of one fifth the operating bit rate (in this case, 10MHz). Each PLL has an associated filter that requires external components; a full description of these is given in the SP9921 datasheet. The decoded data and the recovered clock from the SP9921 are ECL outputs which are converted to TTL levels by an MC10H125.

Conversion of the serial data stream back into 5-bit words is achieved with a 74F299 shift register. The first bit is the frame and is always a logic '1'. The frame can be simply detected during the video sync period, when the transmitted word is 10000. Four wire-ORed diodes detect the 4 zeros; this signal is connected to a NOR gate together with the inverted first bit to detect the 10000 pattern. Fast Schottky diodes should be used as the detection window is very narrow. The output of the NOR gate is the frame sync pulse, which is used to load a 74F161 synchronous counter with a count of 11. After a further 4 clock pulses the count reaches 15, at which point a carry output is produced at pin 15 to reload the counter with 11. The 74F161 is therefore configured as a divide-by five counter. The output of the counter is thus synchronised to the 5-bit word pattern and is used to clock the last 4 bits of the word into the 74F174 register. This 4-bit word is a digital representation of the analog video signal.

The MV95308 8-bit low cost DAC converts the digital signal back into analog form, producing a current output which is proportional to the digital input. The current output is converted into a standard 1Vp-p using a 75Ω resistor, which can be the termination in the monitor.

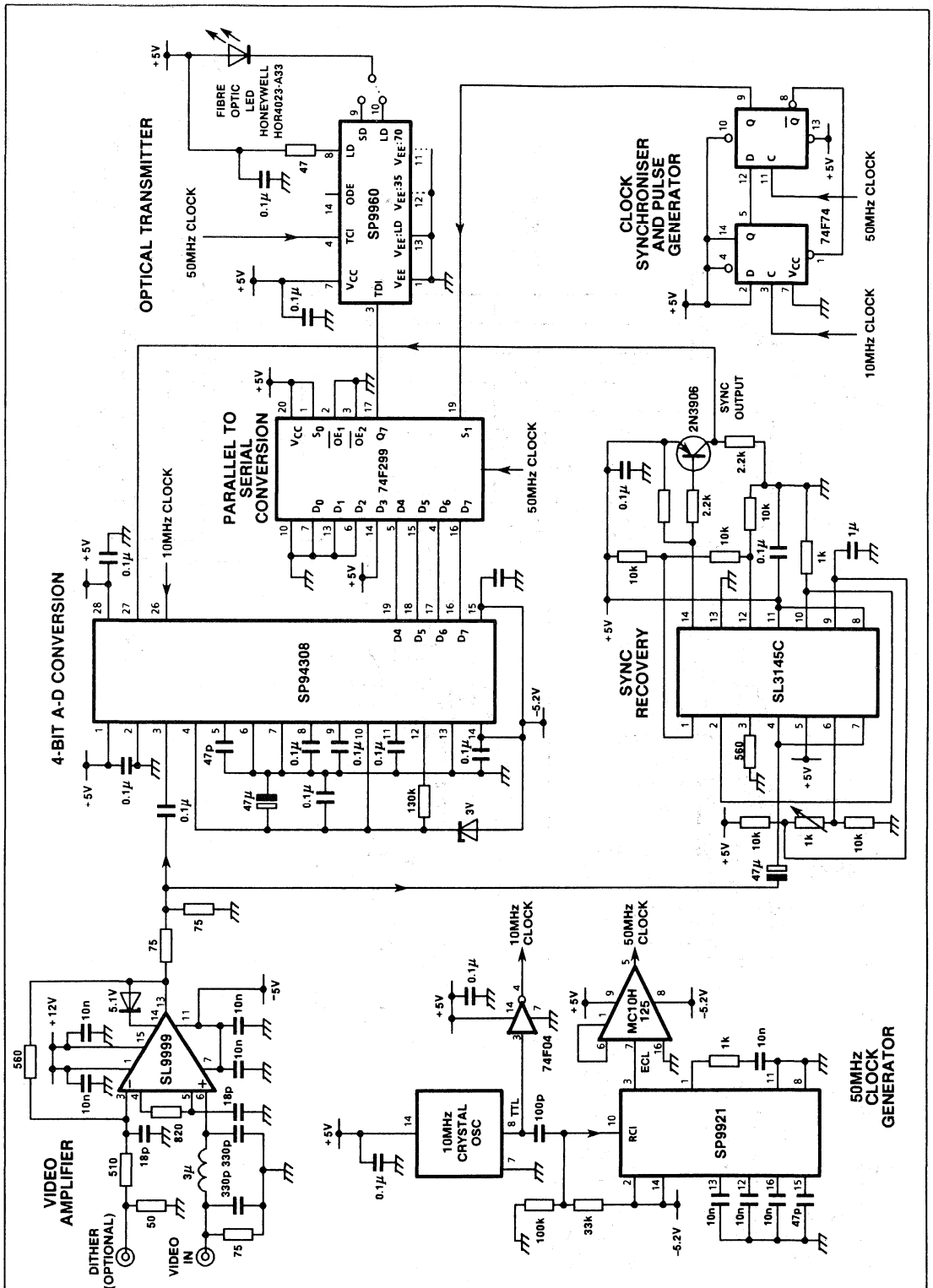



*Fig.1 Four-bit digitised video and 50MB/s fibre optic transmitter*

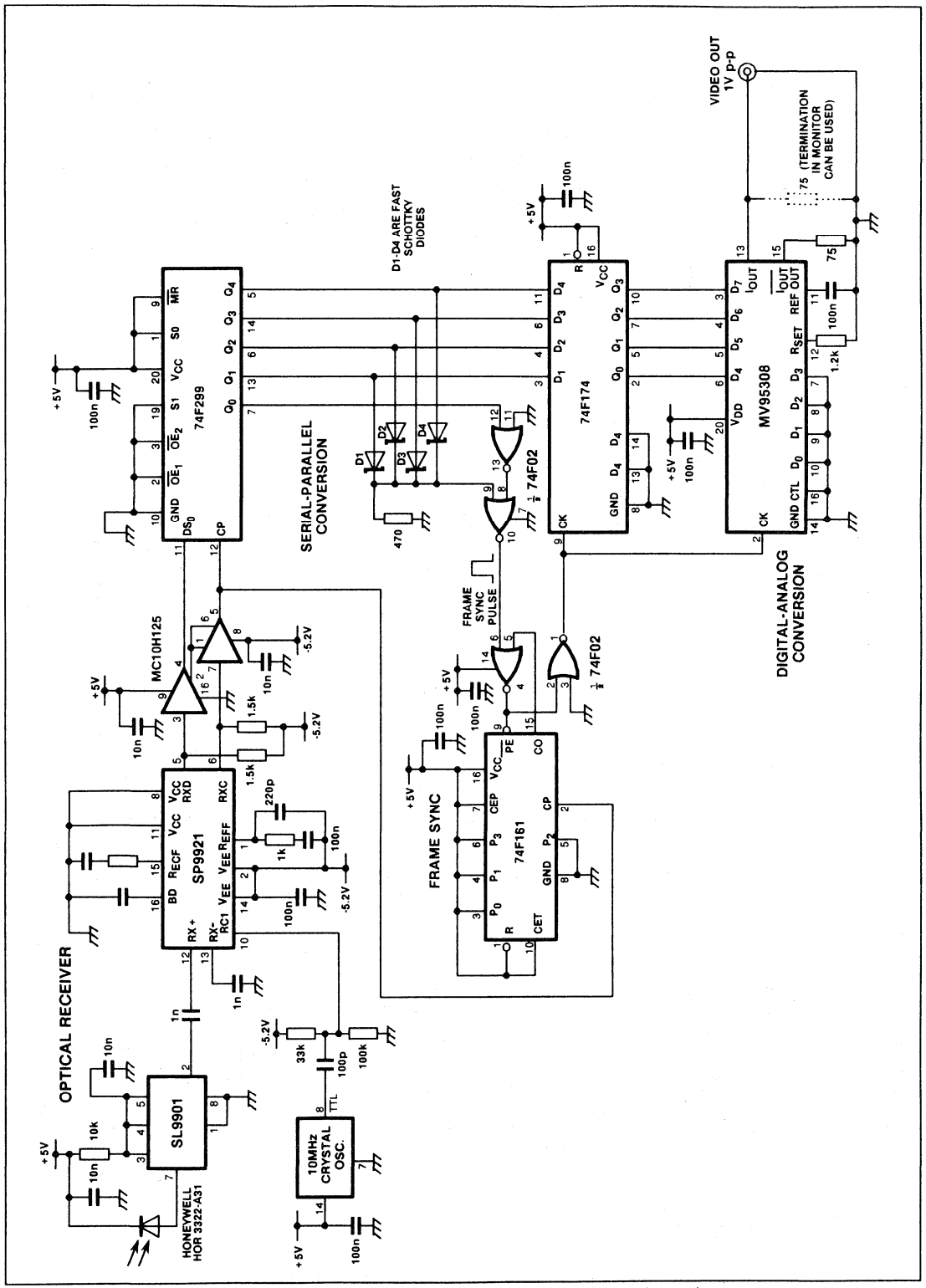



*Fig.2 Four-bit digitised video decoder and 50MB/s fibre optic receiver*

# FDDI
# Fibre Distributed Data Interface

AN66

**FDDI (Fibre Distributed Data Interface) is a standard defined by ANSI (American National Standard Institute) for a token passing ring network operating at a user rate of 100MB/S. The standard consists of 4 documents;**

1. **Physical Media Dependent (PMD)**
2. **Physical Layer Protocol (PHY)**
3. **Media Access Control (MAC)**
4. **Station Management (SMT)**

**These documents correspond closely with the OSI seven layer model, PMD and PHY are sublayers of the OSI physical layer. The MAC document implements some of the OSI Data link layer. Overall control of the PHY and MAC functions is provided by the SMT.**

## INTRODUCTION

### Technical Overview (The Physical Layer)

Fig 1 shows a block diagram of the Physical Layer, the first section is the 4B/5B codec, here the data is in symbols, four bits wide at a rate of 25MB/S. Each four bit code received, is converted into a 5 bit code according to a pre-defined table. This extra bit is added to prevent long runs of zeros, it also allows the addition of signalling words by the control section. A circuit incorporating the Codec function is not yet available could be implemented in semi-custom CMOS, such as the CLA60000 series.

After conversion to a 5-bit word the data undergoes a parallel to serial conversion, this multiplies the transmission rate up to 125MB/S. In order to clock the data out at this rate the clock needs to be multiplied five times up to 125MHz, this is achieved with a phase locked loop in Plessey's chip set. Before transmission over the fibre the data is converted to a code called NRZI, in this code a 'I' is represented by a transistion and '0' as no transition. This coding maximises transistions without increasing the bandwidth of the signals, and when combined with the 4B/5B coding this system minimises the DC content of the signal. On the receive side the transistions within the NRZI code are used to recover the 125MHz clock.

FDDI specifies a fibre optic transmission medium of 62.5 $\mu$m core multimode fibre (this is the recommended core size; 50, 85 and 100$\mu$m cored fibres are allowed alternatives), a 1300nm LED source, and a maximum distance between nodes of 2km. The optical interface can be implemented using circuits such as the 200MB/s SP9944E, which incorporates an optical flag that is raised when the receive signal fails to meet the required power level and is a requirement of FDDI.

Up to 500 nodes and a total fibre length of 200km are supported by FDDI. A distance of up to 2km is supported by the present multimode interface, and work is in progress to modify the standard to allow a single mode interface for larger distances.

A further modified network called FDDI-II is proposed that uses 6MB/S time slots for isochronous data such as voice, low rate video and point to point data links. FDDI-II uses the same physical layer as FDDI-I.

## THE FDDI CHIPS

### Introduction

The FDDI chips available for the 4B/5B to NRZI interface comprise a transmitter chip and a receiver chip, contained in two 28-pin packages,

The block diagrams of these circuits are shown in Fig.2 and Fig. 3 respectively. Figs. 4 and 5 show the pin connections and Tables 1 and 2 detail the operating mode. Both chips operate on a supply of +5V/-5.2V. TTL and differential ECL interfaces are used for the 25MB/S and 125MB/S signals respectively; all control and alarm signals are TTL levels. The ECL interfaces are 10KH compatible. Although the devices are designed to operate at a line rate of 125MB/S, performance up to 170MB/S can be expected at 25°C. Both transmitter and receiver have a loopback mode, serial data from the local transmitter is looped back to the local receiver. The devices are manufactured using a high speed bipolar process.

### Transmitter

The SP9970 transmitter (Fig.2) is the simpler of the two devices and takes a supply of approximately 30 mA and 80 mA on the +5V and -5.2V supplies respectively. Only two external components are required, a capacitor and resistor; these provide the phase lock loop filter.

An on-chip phase locked loop, consisting of a phase/frequency comparator, charge pump and a VCO is used to multiply the local symbol clock (LSCLK) by five. This provides a transmit bit clock (TBCLK) of 125MHz and a differential ECL output allows monitoring of this signal.

A parallel to serial converter changes the input data into a serial data stream of 125MB/s. No framing signal is added, as the 4B/5B code is constructed such that the bit sequence can be recovered in the 5B/4B decoder in the receiver. Immediately after conversion to serial form the data is encoded as NRZI (Non Return to Zero Invert on Ones), i.e. a transition occurs if the input is at a logic 'I' but no change if it is at a logic '0'. Use of this code minimises the DC component and therefore allows the signal to be AC coupled as is common practice on high rate fibre optic receivers. With the 4B/5B code no more than nine zeros occur and this only in the 'Master Line' state. TDATA 4 is transmitted first and TDATA 0 last.

Differential ECL output buffers are provided for the Transmit coded data (TRCD) and loopback transmit data (LTXD), these minimise noise and DC level problems. When the 'FOTOFF' control signal is at a logic '0' the TRRD buffer is forced to a known state (see Table 1), this control signal is normally used to switch off the optical transmitter. The 'NRZI' data is also connected to the loopback buffer (LTXD), this output is enabled when 'LP BACK' is at a logic '0'. If disabled the 'LTXD' output is forced to a known state. (see Table 1)

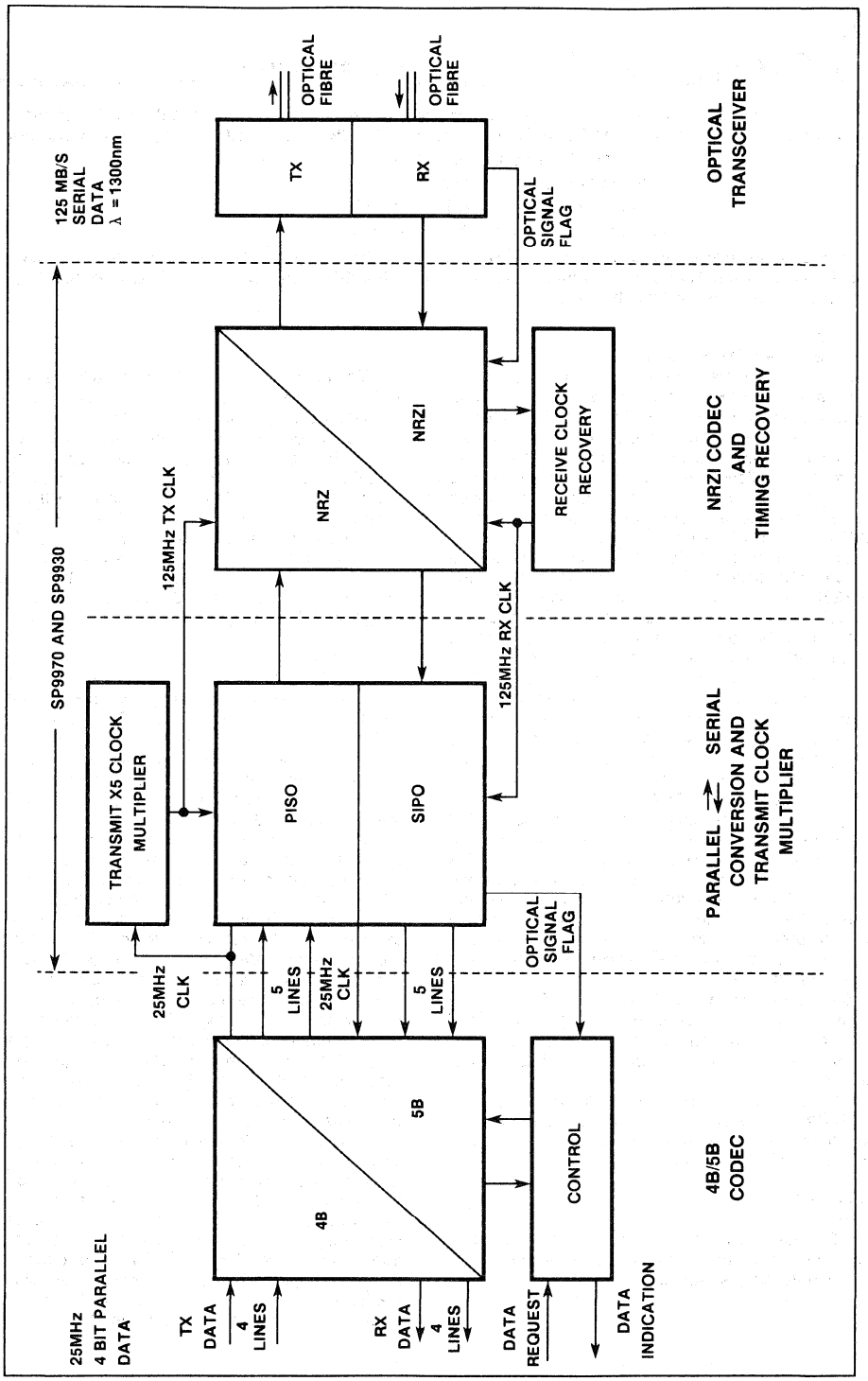



*Fig.1 FDDI physical layer (block diagram)*

**Receiver**

The SP9930 receiver is powered from +5V and -5.2V supplies with currents of 40 and 170 mA respectively. Again only two external components are required, a capacitor and a resistor, these provide the phase lock loop filtering.

A block diagram of the receiver is shown in Fig. 3. The serial data is input from the fibre optic receiver through a differential ECL input stage. When no data is present at the input, indicated by a low on Signal Detect Input (SDI), the internal VCO is locked to five times the local symbol clock (LSCLK). This arrangement gives an accurate 125MHz free running clock and a very short lock-on time of $<1\mu S$. When the SDI pin is high the device changes mode and locks to the received data (RCVD), the 'MODE' pin is used to indicate which mode the device is operating in.

While the VCO is locked to the RCVD its frequency is continuously monitored, if the frequency error exceeds $\pm$`1% the phase locked loop (PLL) changes back to the LSCLK mode. Once a frequency accuracy of $\pm 0.5\%$, relative to the LSCLK is achieved the PLL returns to the RCVD mode, provided SDI is high. Jitter on the receive bit clock should be $<2.27$ns pk-pk provided the RCVD jitter is $<4.2$ns pk-pk. External components are used to select the time constant of the PLL, and the error voltage from the comparator is available at an external pin (ERROR) through a buffer.

Following clock recovery the data is converted from NRZI to NRZ before the parallel to serial conversion. Parallel data is presented as five-bit wide symbols at the RDATA outputs (TTL levels). The data bits transmitted will not necessarily appear on the same pins as they were transmitted, this is because the framing is performed in the 4B/5B decoder. A 25MHz Receive Byte Clock (RBYCLK) is provided, to allow data to be clocked into the following word alignment and decoding circuits.

A Signal Detect Output (SDO) is provided; this directly reflects the SDI input, except that it is clocked out on the next LSCLK positive edge after SDI changes.

**PHASE LOCKED LOOP CHARACTERISTICS**

**Transmitter**

The transmitter PLL uses the 25MHz LSCLK as the reference and provides a 125MHz TBCLK locked to five times this reference. Although not normally used the TBCLK is provided as a differential output. Internally the PLL comprises a phase frequency comparator, a charge pump and a VCO (see Fig. 2). The phase/frequency comparator outputs correction pulses which are converted to current pulses by the charge pump. These current pulses are used to charge an internal reservoir capacitor through a resistor, and allows small instantaneous changes in the VCO frequency, aiding the capture time and improving supply noise rejection. Fig. 8 shows the alignment of the TBCLK with the LSCLK. Refer to Fig. 12 and parts list for the recommended PLL filter components.

Fig. 6 shows the VCO frequency against the control voltage on the FLTR pin, and shows that the device has a resonably linear characteristic. Typically, the device will operate between 50 and 170MHz and can therefore be used for applications other than FDDI, jitter is likely to increase at the extremities of operation.

**3.2 Receiver**

The receiver PLL is more complex than the transmitter as it is required to lock on to varying data patterns. Under worst conditions (Master Line State) 1 transistion occurs every 10 bits. However the device will still recover clock with only 1 transition in every 16 timeslots with the filter components shown in Fig. 12.

Unlike the transmitter the receiver PLL operates in two modes as described in section above. In mode 0 the VCO is locked to five times the LSCLK input and in mode 1 the VCO is locked to the incoming data. As shown in Table 2, the actual operating mode is indicated by the logic level at the mode output pin. While in mode 1 a frequency counter monitors the VCO frequency to check that it is five times the LSCLK frequency, if the error is more than $\pm$ 1% the PLL defaults back to mode 0 and this indicates that lock has been lost. Before switching back to mode 1 the VCO must achieve an accuracy of $\pm$ 0.5% when compared to five times the LSCLK input. Note that the measurement period is 40 cycles of the LSCLK so that at 25MHz at least $1.6\mu S$ must be allowed before the PLL will switch back to mode 1.

Whenever the SDI flag is raised the PLL will automatically switch to mode 0 as this indicates there is no valid input signal. Conversely when the 'LP BACK' signal goes 'low' the device will default to mode '1', this allows loopback to be used regardless of the optical input signal condition.

Internally the PLL consists of a patented integrate and hold phase comparator driving a charge pump with an internal reservoir capacitor. The reservoir capacitor smoothes the current pulses from the charge pump and provides a relatively noise free voltage to control the VCO. A small resistor in series with the capacitor allows small instantaneous changes in frequency, increasing this resistor improves the capture time but adversely affects the jitter. In practice using the values shown in Fig. 11 will produce a capture time of $<1\mu S$ and very low jitter.

Fig. 7 shows the VCO frequency against the control voltage at the FLTR pin, the control voltage goes positive for the higher frequencies. As shown by the graph, the device has a wide range of operation from 60 to 175MHz. If the device is used at a non FDDI frequency the LSCLK must always be a fifth of the operating frequency ($\pm 0.25\%$), otherwise the frequency comparator will switch into mode 0. The reliability of operation at the frequency extremes is not guaranteed, jitter does increase at the low frequencies but at the higher frequencies it is minimal.

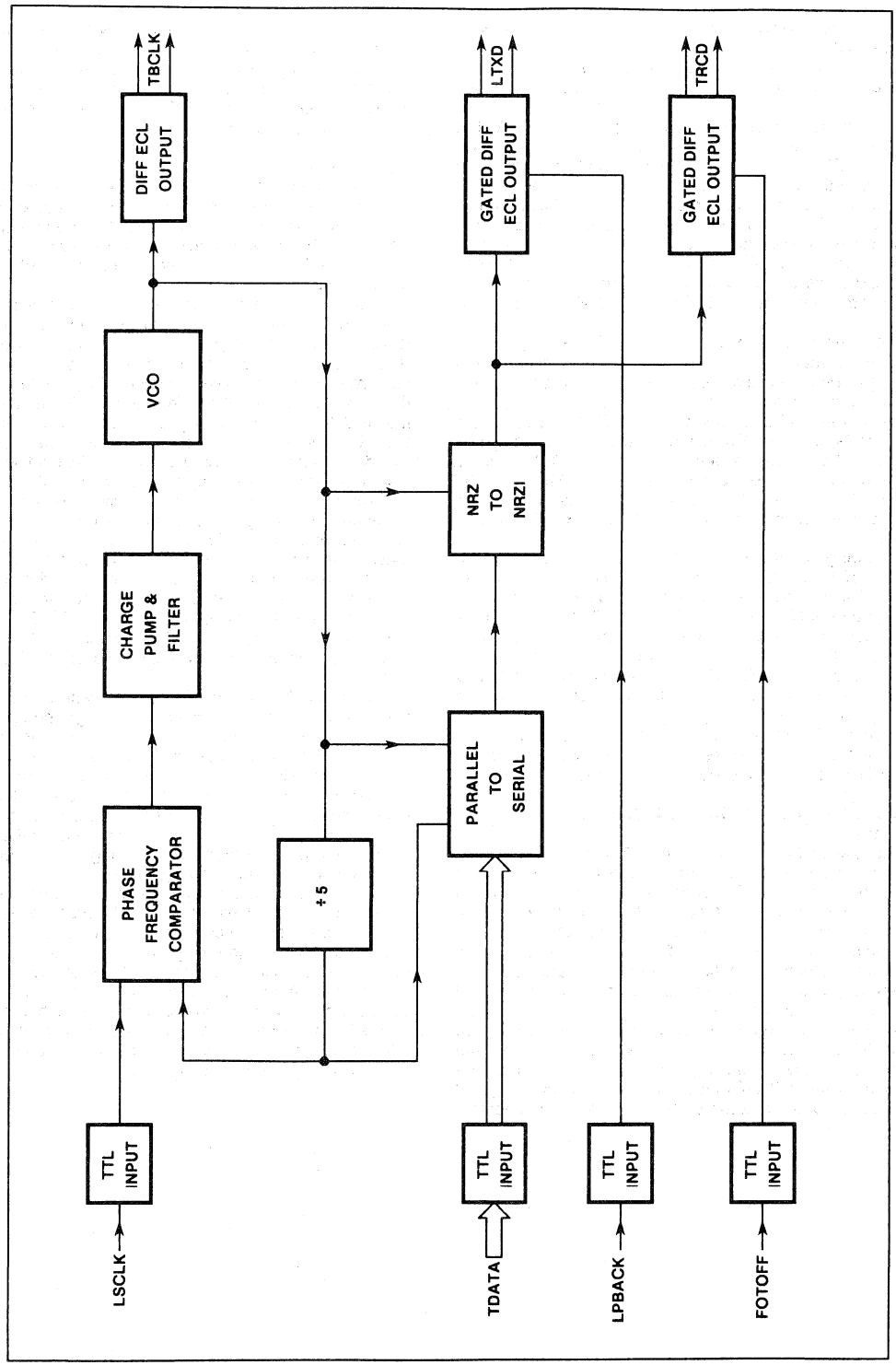



*Fig.2 SP9970 transmitter block diagram*

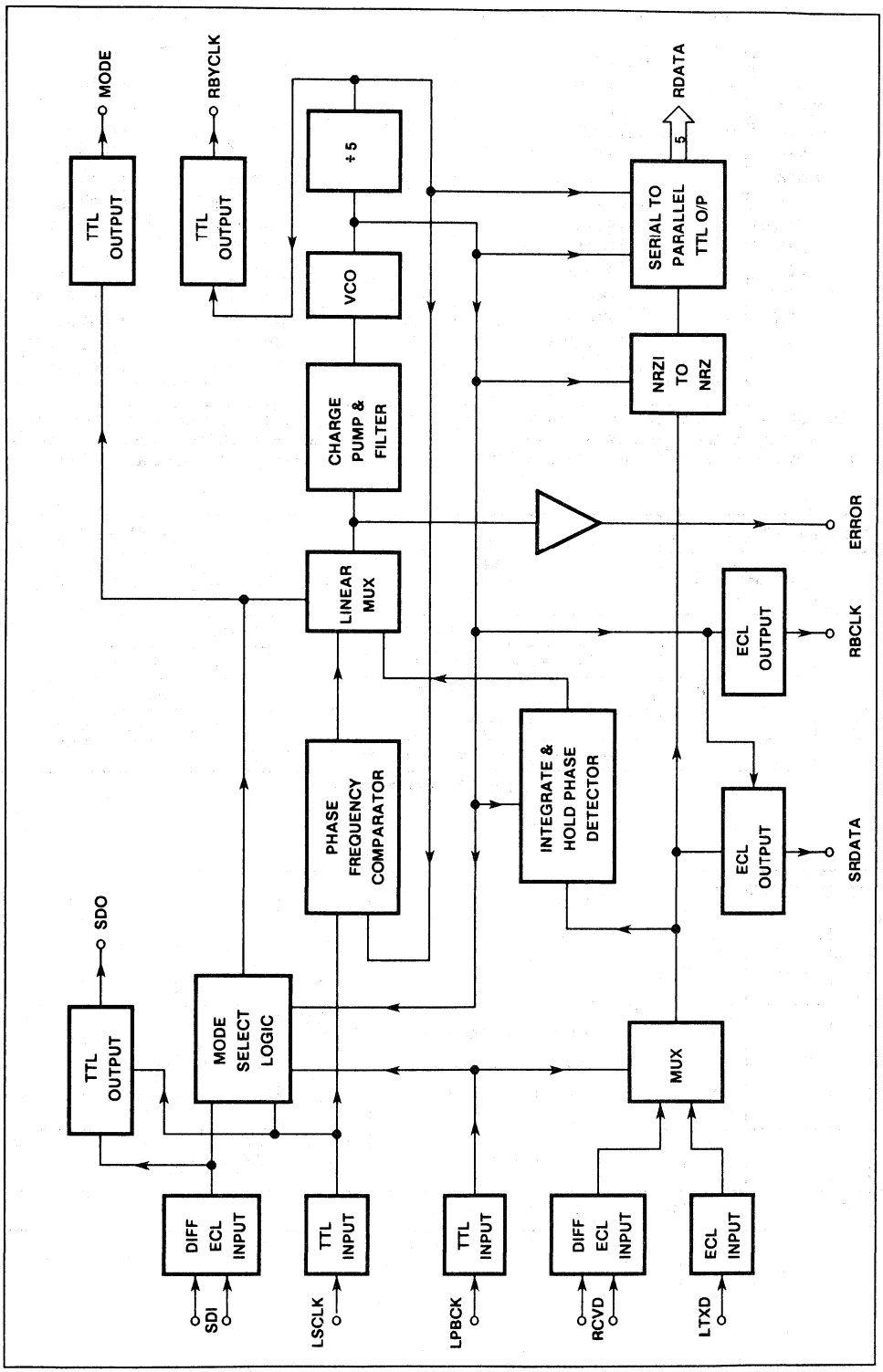



*Fig.3 SP9930 receiver block diagram*

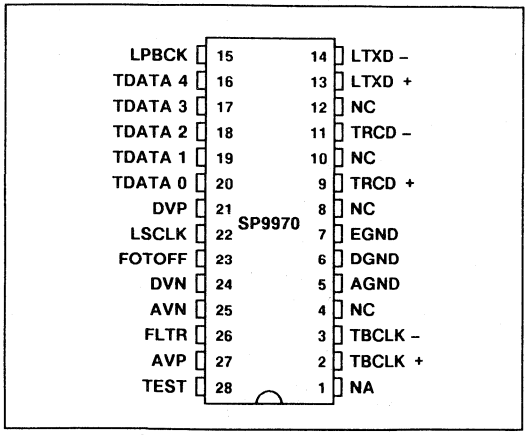



*Fig.4 SP9970 pin connections - top view (Dual-in-line package variant for evaluation purposes only. See datasheet for package availability)*

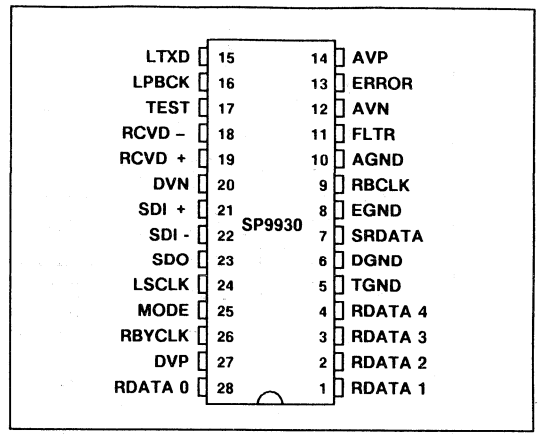



*Fig.5 SP9930 pin connections - top view (Dual-in-line package variant for evaluation purposes only. See datasheet for package availability)*

| CONTROL INPUTS (TTL) | | | FUNCTION | DATA OUTPUTS (ECL) | | | |
|---|---|---|---|---|---|---|---|
| | | | | TRCD | | LTXD | |
| FOTOFF | LPBCK | TEST | | + | – | + | – |
| 1 | 1 | 0 | Normal operation | Coded data | | Lo | Hi |
| 0 | 1 | 0 | Fibre optic transmit disabled | Lo | Hi | As above | |
| 1 | 0 | 0 | Loopback mode | Coded data | | Coded data | |
| 0 | 0 | 0 | Loopback mode | Lo | Hi | Coded data | |
| X | X | 1 | Test mode for manufacturer's use only | X | | X | |

*Table 1 Transmitter function*

| CONTROL INPUTS (TTL) | | | | FUNCTION | SRDATA (ECL) | RDATAn (TTL) | SDO (TTL) | MODE (TTL) |
|---|---|---|---|---|---|---|---|---|
| SDI (ECL) | | LPBACK (TTL) | TEST (TTL) | | | | | |
| + | - | | | | | | | |
| Hi | Lo | 1 | 0 | Normal operation | RCVD data | Decoded data from RCVD | 1 | 1 = locked 0 = unlocked |
| Lo | Hi | 1 | 0 | Fibre optic receive disabled | Lo | 0 | 0 on next LSCLK ↑ edge | 0 |
| X | X | 0 | 0 | Loopback mode | LPBCK data | Decoded data from LPBCK | 1 | 1 = locked 0 = unlocked |
| X | X | X | X | Test mode for manufacturer's use only | X | 1 | X | X |

*Table 1 Receiver function table*

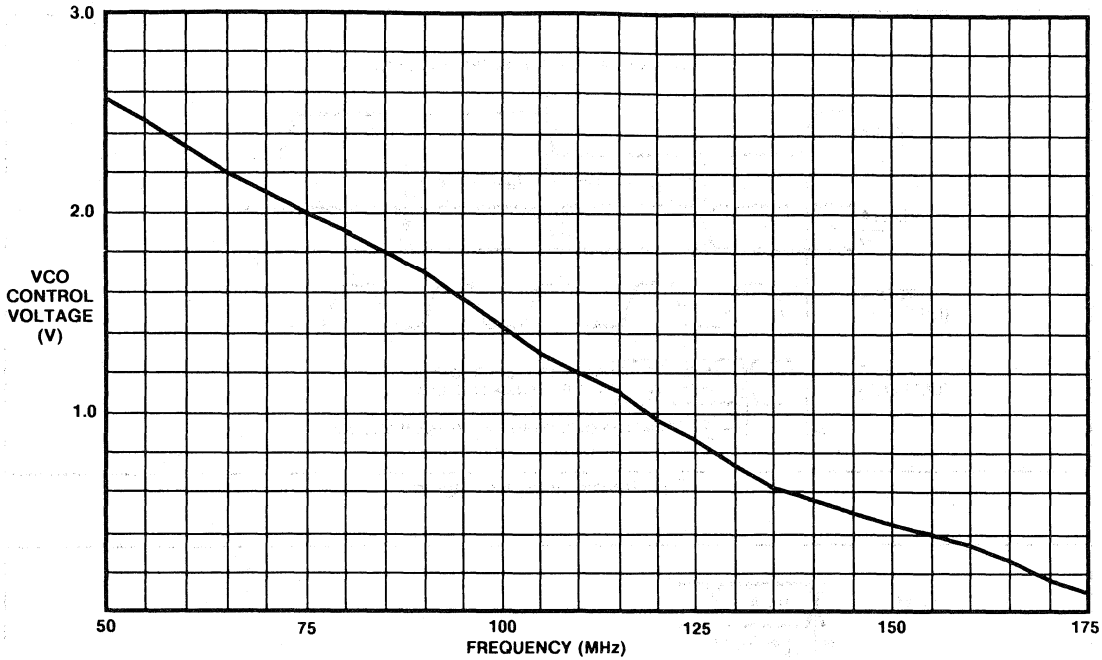



*Fig.6 Transmitter VCO characteristic (typical)*

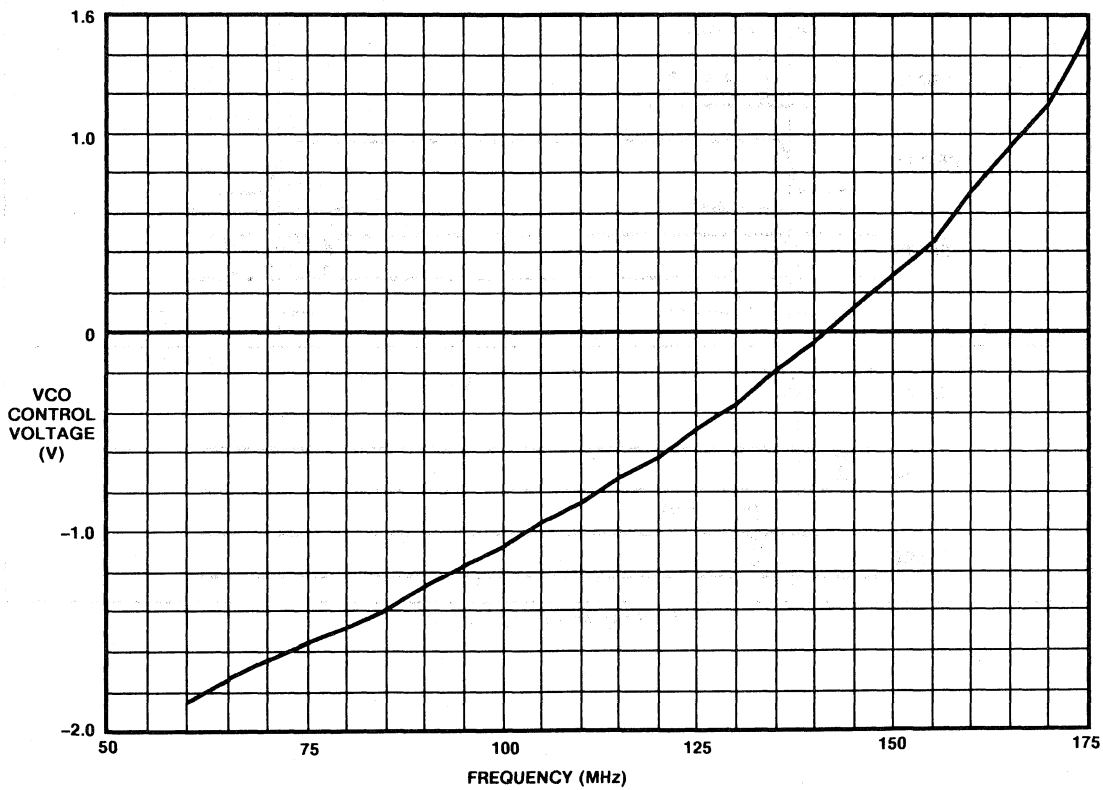



*Fig.7 Receiver VCO characteristic (typical)*

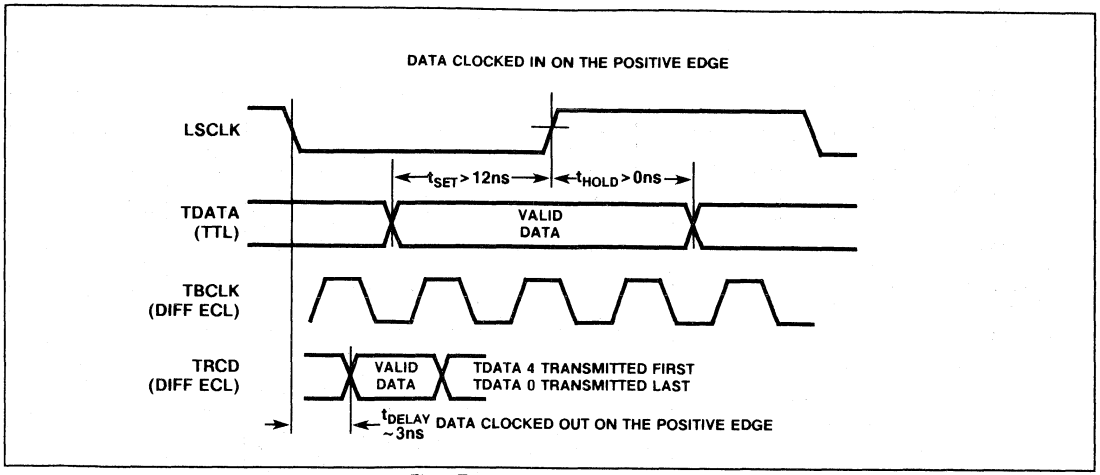



*Fig.8 Transmitter timing diagram*

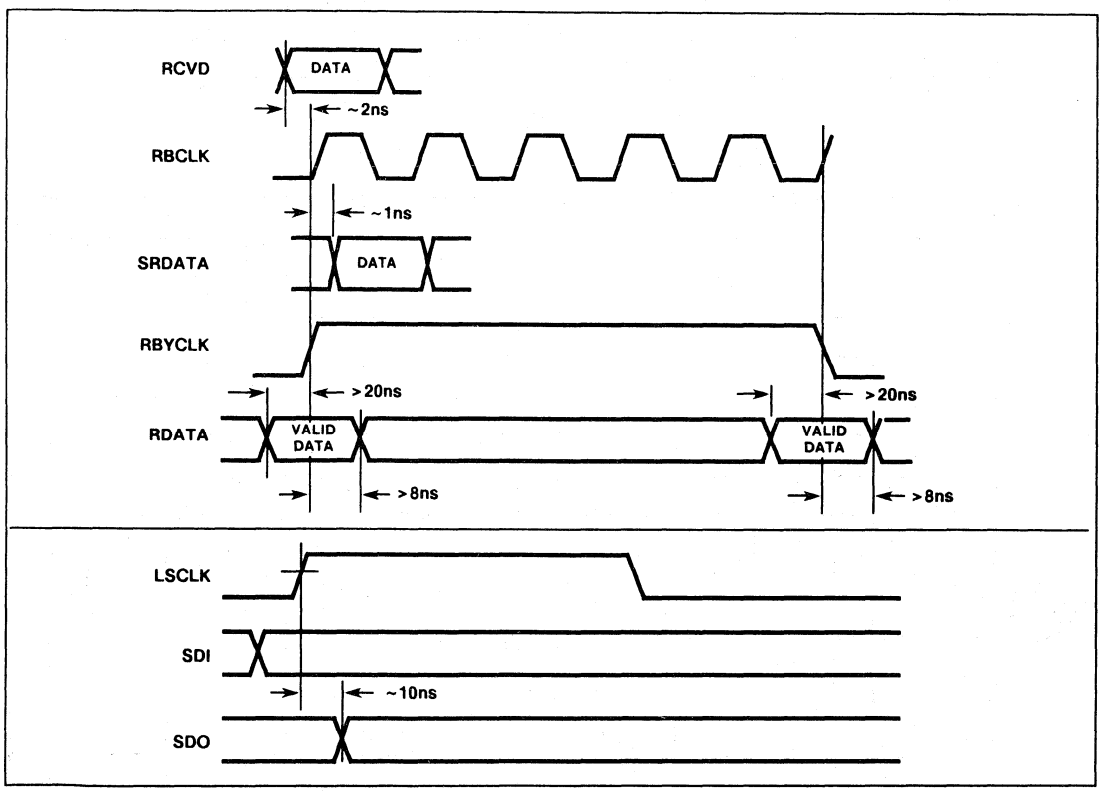



*Fig.9 Receiver timing diagram*

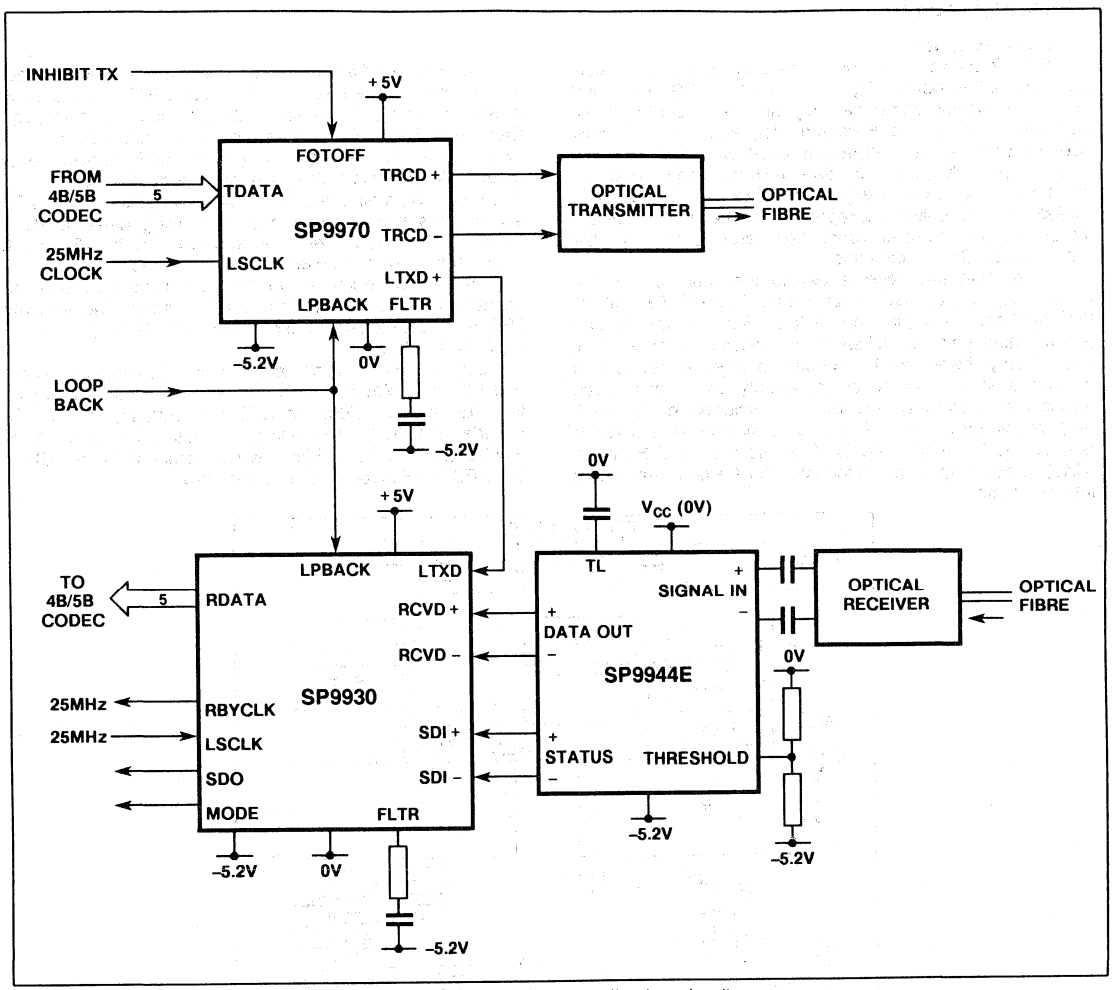



*Fig.10 Typical FDDI application circuit*

## EVALUATION BOARD

### Circuit Description

Fig. 12 shows the circuit diagram of the FDDI physical layer evaluation board, Fig. 13 shows the PCB layout and Fig. 11 shows the component layout. The board has been designed to fit into a Eurocard slot, although it is only 100mm long. A ground plane is used on the top layer to improve grounding and minimise noise problems. Note that the board has been designed to take the SP9970 and SP9930 in dual-in-line packages; whilst these are available for evaluation purposes, production versions are available only in Quad Cerpac packages.

A transmit and receive device are mounted on the board, they are connected as if used in an FDDI system, the loopback data pins are linked. Serial transmit and receive data pins are taken to test points for monitoring, alternatively these can be connected together (to form a second loopback) or taken externally to a fibre optic transceiver. Pulldown resistors are included on all ECL outputs except LTXD+. A subvis co-axial connector (SK2) is provided to monitor the Tx data and the serial Rx clock (SK3), these outputs are attenuated 50:1 when terminating into 50 Ohms.

An on-board 25MHz crystal oscillator is provided that can be used for the LSCLK to IC1 and/or IC2, but provision is also made for an external LSCLK, connected through SK1. Selection of the LSCLK source is made by SL1. A switch (SW1) is used to change the 5-bit paralled data input. SW1-6 selects the loopback mode for both chips. The received parallel data is indicated on LEDs LD1-5, LD6 showing the signal detect output. If using dynamic data, SW1 and IC3 may be removed and replaced by 16-pin DIL socket (using the two holes adjacent to SW1)

An IDC connector or pin header can then be used to connect the parallel data inputs and outputs, the transmit LSCLK is connected to pin1 (next to SW1-1) and the RBYCLK to IC3/7.

SW2 allows changing of the control inputs; SDI, TEST and FOTOFF. When SDI is active LD7 should illuminate, this LED also provides an ECL low voltage, DI and D2 provide an ECL 1.2V reference to bias the second input. SW2-2 (test) should be kept low for normal operation, SW2-3 the FOTOFF input should be kept low.

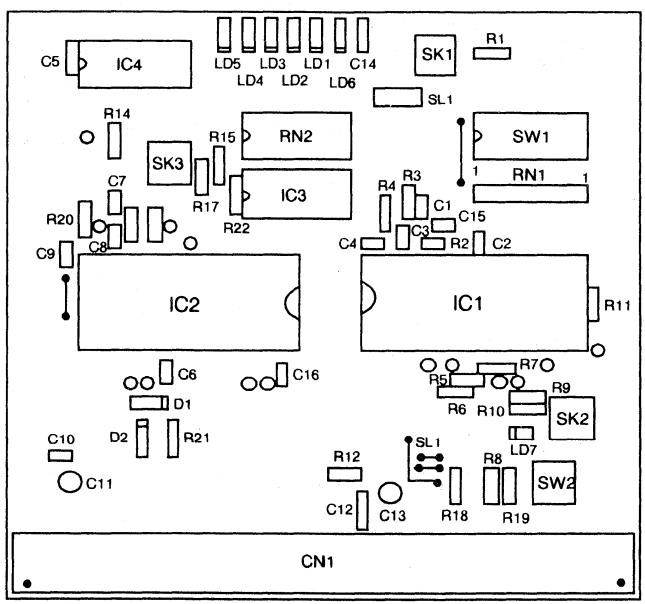



*Fig.11 Evaluation board component layout. Key: O = Test Point (TP), ●—● = link*

## COMPONENT LIST FOR EVALUATION BOARD

| | | | |
|---|---|---|---|
| IC1 | SP9970 | R1,10,15 | 51Ω 1/4 or 1/8 Watt |
| IC2 | SP9930 | R2,4,14,20 | 10Ω 1/4 or 1/8 Watt |
| IC3 | ULN2003A (Spague or SGS) or RS 307-109 | R3,13 | 390Ω 1/4 or 1/8 Watt |
| IC4 | 25MHz Crystal Oscillator (X120A from IQD Ltd.) | R7,17 | 560Ω 1/4 or 1/8 Watt |
| SW1 | 6-way DIL switch | R5,6,8,18,19 | 820Ω 1/4 or 1/8 Watt |
| SW2 | 4-way DIL switch | R9,16, 21 | 1.2kΩ 1/4 or 1/8 Watt |
| SK1-3 | Subvis Coaxial Connector | R11,12 | 10kΩ 1/4 or 1/8 Watt |
| CN1 | 32-way DIN 41612 Connector | C1, 2, 4-6 ,8-10,12,14-16 | 100nF Ceramic |
| RN1 | 8-pin SIL 10kΩ Resistor Network (AB 850-81-10K) | C3, 7 | 3.3nF Ceramic |
| RN2 | 14-pin DIL 150Ω Resistor Network (AB 760-3-150R) | C11, 13 | 47μF, 16V Electrolytic |

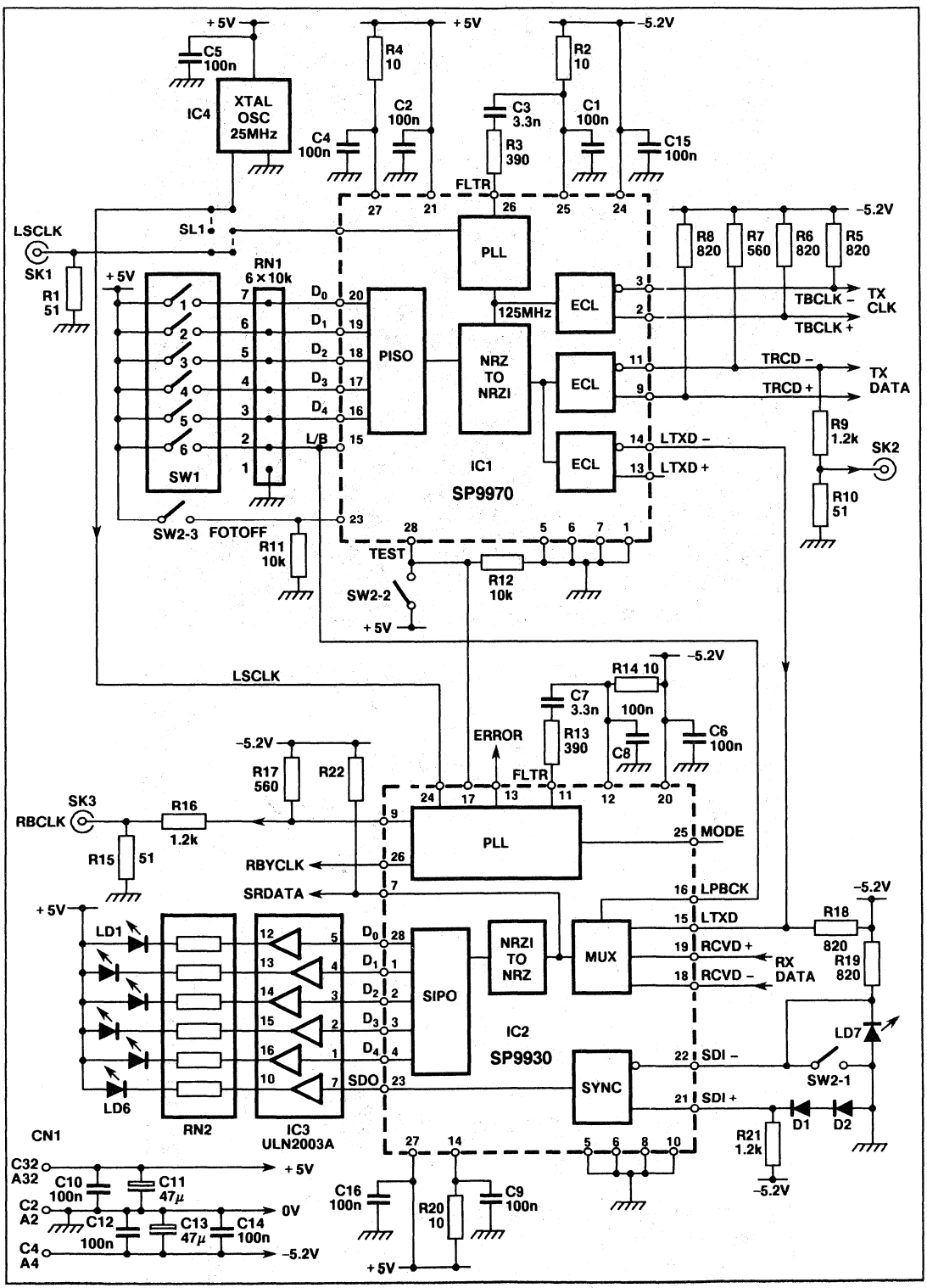



*Fig.12 FDDI evaluation board circuit diagram*

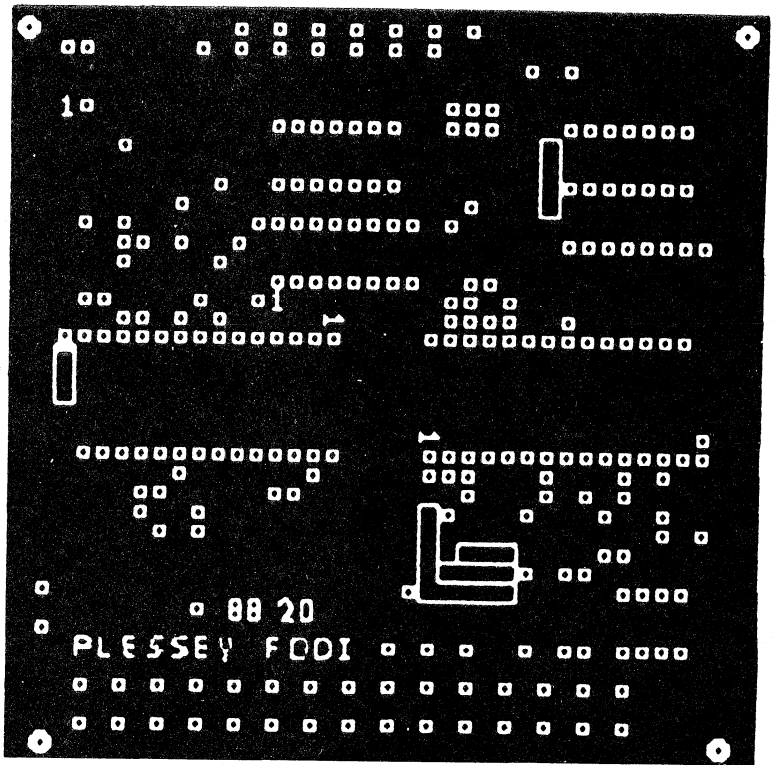



*Fig. 13a Evaluation board, track side*

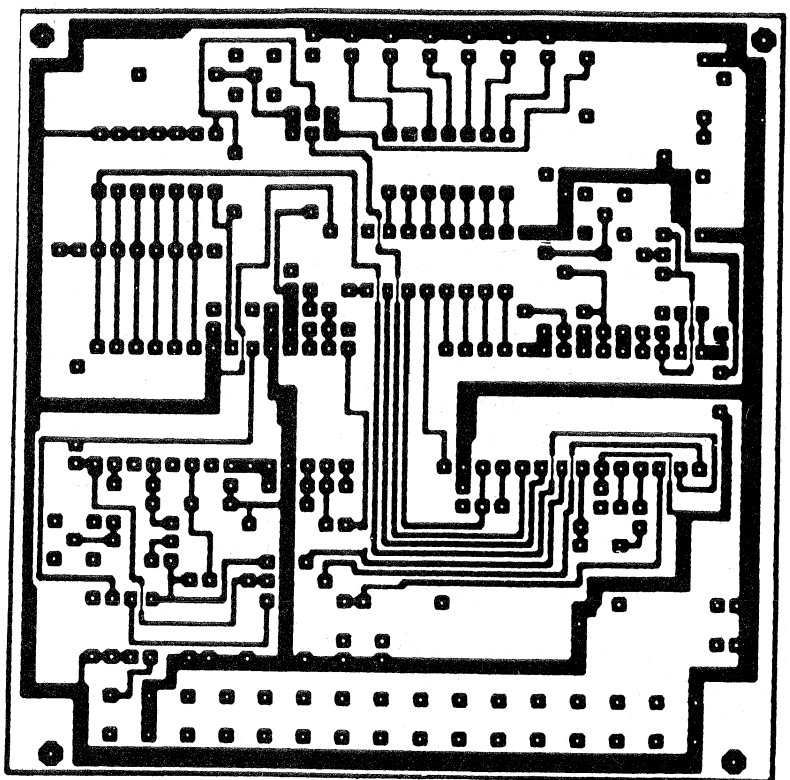


*Fig. 13b Evaluation board, component side (ground plane)*

# The SP92701 Used in Analog Circuits



**As an ECL line receiver/driver the SP92701 is mainly intended for digital applications, enhancing the edges of ECL and hence reducing time jitter. This is of importance especially when driving clock signals into analog to digital converters and other sampling circuits.**

**This Application Note is somewhat unusual in that it describes the use of this digital part in an analog circuit. This circuit can amplify low level signals and drive 50Ω differential lines with low noise and low distortion.**

The SP92701 can be considered as a simple differential pair with emitter follower outputs. The internal circuit design is enhanced by the addition of a constant current source in the tail of the input differential pair (see Fig. 1). This is unusual, as standard line receivers usualy incorporate just a simple resistor to provide the tail current.

This current source improves the input common mode range and common mode rejection ratio greatly. This gives a typical common mode voltage range of over 2V and therefore the device can be used in a wider range of applications.

Many glue circuits which connect one system to another consist of a differential pair with output followers and this is also how a simple op-amp could be constructed.

A particular feature of the SP92701 is its inherent stability. Unlike most line receivers the SP92701 has a low differential gain of 25dB which again allows the device to be used in more general analog applications.

The SP92701 has a non-inverting bandwidth of over 700MHz and an inverting bandwidth of 400MHz. The inverting bandwidth is reduced due to the reduced input to output Isolation; This is true for any differential pair.

Another feature which should not be overlooked is the on-board ECL reference ($V_{CC}$–1.28V) which can be used for biasing one of the inputs in analog circuits as well as in digital ECL circuits.

The device is packed in an 8-pin DIL and pinned out sensibly with inputs on one side and outputs on the other, see Fig. 2.

## THE SL560/SP92701 COMBINATION

This combination of low cost integrated circuits demonstrates the SP92701 as a wide band analog circuit. Fig. 3 shows the internal circuits of both parts and all the external components required to produce a high performance low noise amplifier.

The SL560 is a low noise pre amplifier which provides over 30dB of gain in the configuration shown. Following this is the SP92701 which is configured as an analog op-amp. In this circuit configuration the SP92701 receives the analog signal from the SL560 and provides true and inverse outputs capable of driving 50Ω . These complimentary outputs are ideal for differential drive of twisted pair cable with voltage swings up to 1.5V p-p.

The circuit operates up to 350MHz and remains flat to ±1dB at 30dB gain when driving 50Ω (see Fig. 4). This type of performance competes with hybrid amplifiers costing up to twenty times that of both these integrated circuits combined.

Fig. 6 shows a PCB and a layout incorporating these two devices. Other experiments with the SP92701 have been conducted, such as positive feedback for an ultra high speed Schmitt trigger application (see Fig. 5). Also, negative feedback was used for another linear project that required an ultra-wideband amplifier. All these circuits worked well as long as care was taken with layout and component placement, especially supply and bias decoupling. It is obvious that this device can be used in a very wide range of applications and product areas. It is therefore a good device to keep as general lab stock to solve the more tricky interface problems.

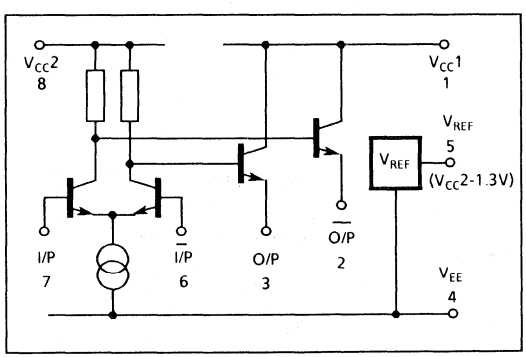



*Fig. 1*

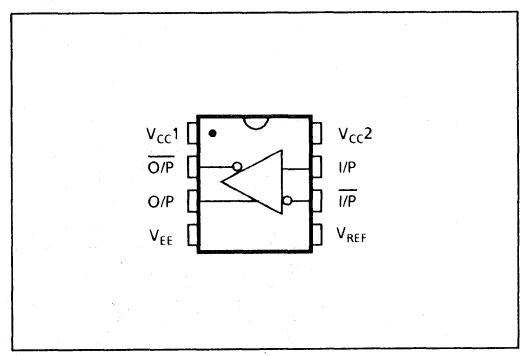



*Fig. 2*

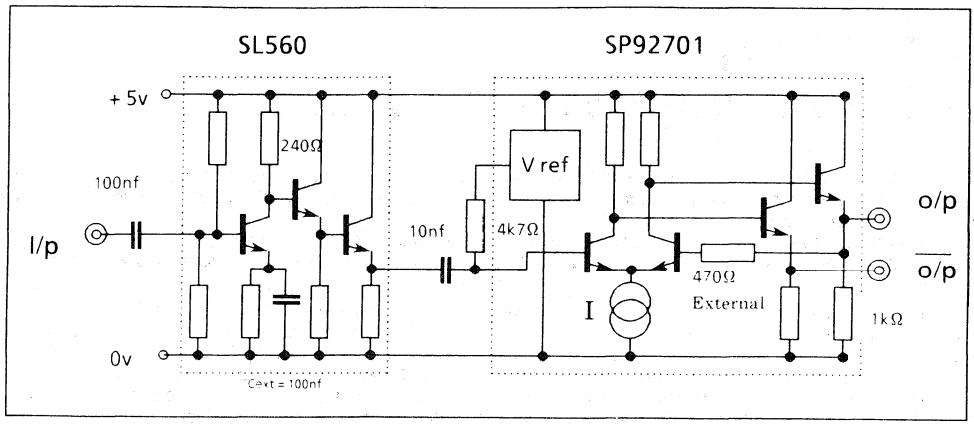



*Fig.3 Low noise amplifier and driver*

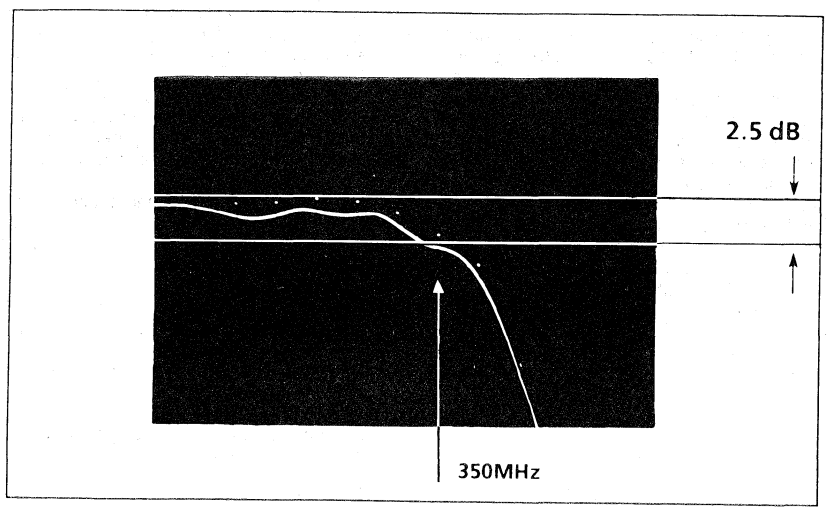



*Fig.4 Bandwidth with markers at 50MHz*

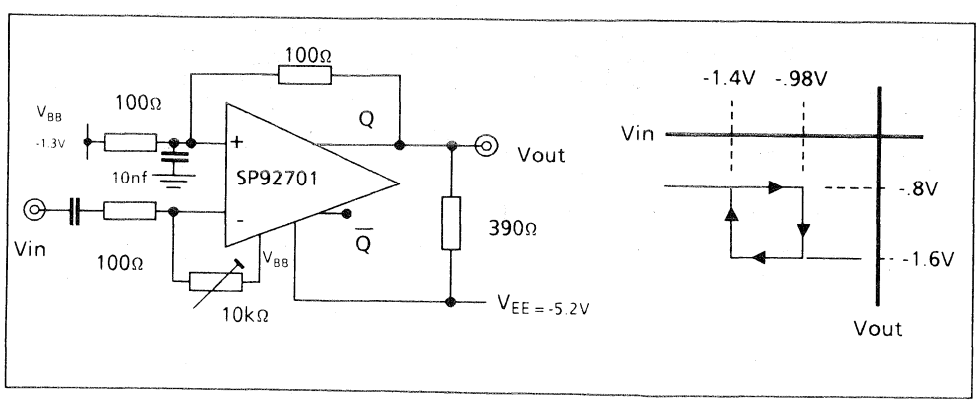
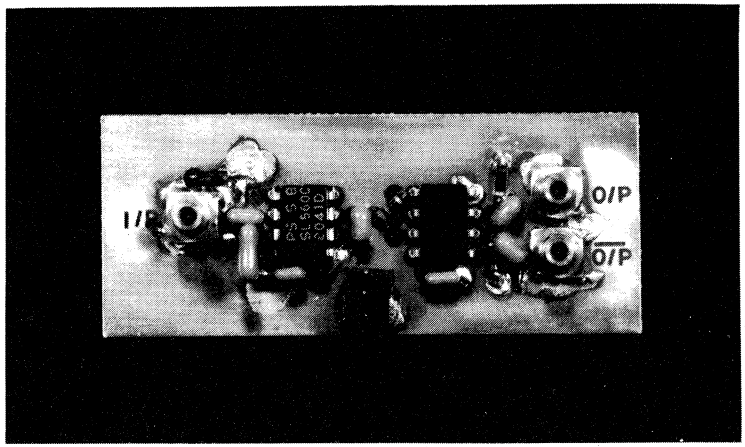



*Fig.5 Schmitt trigger application*

Low noise amp and differential line driver



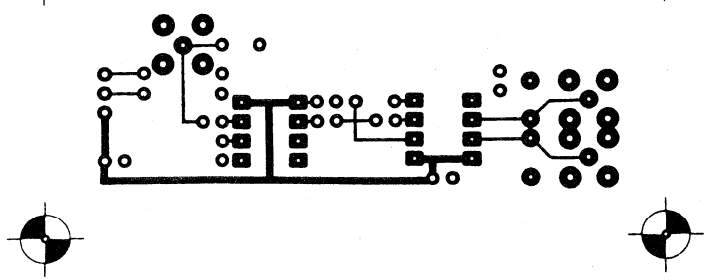



*Fig 6 Layout and experimental board*

# Section 5

## MIL-STD-883C Class B



GEC Plessey Semiconductors is in conformance with the requirements of MIL-STD-883C Notice 11 paragraph 1.2.1 and can supply product requiring the use of this standard.

Approval has been issued by DGDQA against DEF-STD 05-21 (equivalent to AQAP1) and by NSI to BS9000. A number of detailed device approvals to BS9300 and BS9400 have been granted.

The following pages detail the manufacturing procedures required to conform to MIL-STD-883C Class B.

# Screening procedures

## MIL-STD-883C Class B

| Stage/Operation | MIL-STD-883C Methods and Comments |
|---|---|
| Wafer processing | GPS process |
| Circuit probe test | To GPS probe test spec. |
| Chip separation | GPS process |
| Chip inspection and selection | Method 2010 condition B |
| Chip bond and inspect | GPS process |
| Wire bond and inspect | GPS process |
| Internal visual | Method 2010 condition B |
| Customer source inspection | Optional extra |
| Encapsulation | GPS process |
| Temperature cycling | Method 1010 condition C |
| Constant acceleration | Method 2001 condition E, Y1 only |
| Seal test | Method 1014 |
| Visual inspection | For catastrophics, as Method 5004 |
| Interim electrical test | To device spec. with read and record, as Method A |
| Burn-in test | Method 1015, 168 hours at 125°C |
| Post burn-in electrical | As interim electrical, as Method 5004 |
| PDA calculations | Subgroup 1 min. 5% max. |
| Final electrical test | 100% subgroups 1,2,3,4,5,6,7,8,9,10, and 11, as device spec. and Method 5004 |
| Code | As device spec. |
| Seal test | Method 1014 (as necessary) |
| External visual | Method 2009 |
| Form inspection lot | As MIL-M-38510 |
| Select samples for conformance test | As Method 5005 |
| Group A tests | Subgroups 1,2,3,4,5,6,7,8,9,10, and 11, as device spec. and Method 5005 |
| Group B tests | Subgroups 2,3 and 5 (devices classified as static sensitive) as device spec. and Method 5005 |
| Group C tests | Subgroup 1 as per device spec. and Method 5005 (generic data may be used if available) |
| Group D tests | Subgroups 1,2,3,4,5,6,7 and 8 as device spec. and Method 5005 (generic data may be used if available) |
| Prepare data package | |
| Inspect devices, pack and ship with data and C of C | As required |

# Conformance testing

## MIL-STD-883C Class B Method 5005.11

### Group A Electrical Tests

| Subgroup | MIL-STD-883C Methods and Comments | LTPD | Sample Size |
|---|---|---|---|
| 1 | Static tests at +25°C | 2 | 116 |
| 2 | Static tests at maximum rated operating temperature | 2 | 116 |
| 3 | Static tests at minimum rated operating temperature | 2 | 116 |
| 4 | Dynamic tests at +25°C | 2 | 116 |
| 5 | Dynamic tests at maximum rated operating temperature | 2 | 116 |
| 6 | Dynamic tests at minimum rated operating temperature | 2 | 116 |
| 7 | Functional tests at +25°C | 2 | 116 |
| 8 | Functional tests at max. and min. operating temperatures | 2 | 116 |
| 9 | Switching tests at +25°C | 2 | 116 |
| 10 | Switching tests at maximum rated operating temperature | 2 | 116 |
| 11 | Switching tests at minimum rated operating temperature | 2 | 116 |

All non-destructive. Performed on each inspection lot as per MIL-M-38510 3.1.3.8

### MIL-STD-883C Class B Group B Electrical Tests

| Subgroup | Test | Method | Sample Size | Destructive/ Non-destructive |
|---|---|---|---|---|
| 2 | (a) Resistance to solvents | 2015 | 4 | D |
| 3 | (a) Solderability | 2022 or 2003 | 3 | D |
| 5 | (a) Bond strength | 2011 | 4 | D |

Performed on each inspection lot as per MIL-M-38510 3.1.3.8

### MIL-STD-883C Class B Group C Electrical Tests

| Subgroup | Test | Method | Sample Size | Destructive/ Non-destructive |
|---|---|---|---|---|
| 1 | (a) Steady state life test<br>(b) End point electrical parameters | 1005 | 45 | ND |

Generic test data may be used for Group C tests

**MIL-STD-883C Notice 4 Page 3 Clause 17**

'... Group C and D shall have been completed on date codes within 52 weeks **prior** to the date code of product being submitted for acceptance. Group C data shall be on a die in the same microcircuit **group**....with the same **material, design** and **process** and from the same **plant** as the die represented.'

**MIL-M-38510F Page 5 Clause 3.1.3.13**

'Microcircuit group. Microcircuits which are designed to perform the same type of basic **circuit function**....within a given **circuit technology** (e.g. ....ECL....Linear, Hybrid, MOS) which are designed for the same supply, bias and signal voltages and for input/output compatibility and which are fabricated by use of the same basic **die construction** and **metallization**; the same **die attach** method; and by use of bonding interconnects of the same size, material and attachment method.'

# Conformance testing (continued)

## MIL-STD-883C Class B Group D Electrical Tests

| Subgroup | Test | Method | Sample Size | Destructive/ Non-destructive |
|---|---|---|---|---|
| 1 | (a) Physical dimensions | 2016 | 15 | ND |
| 2 | (a) Lead integrity | 2010 | 15 | D |
| | (b) Seal | 1014 | 15 | D |
| | (1) Fine | | | |
| | (2) Gross | | | |
| 3 | (a) Thermal shock | 1011 | 15 | D |
| | (b) Temperature cycling | 1010 | | |
| | (c) Moisture resistance | 1004 | | |
| | (d) Seal | 1014 | | |
| | (1) Fine | | | |
| | (2) Gross | | | |
| | (e) Visual examination | | | |
| | (f) End point electrical parameters | | | |
| 4 | (a) Mechanical shock | 2002 | 15 | D |
| | (b) Vibration, variable frequency | 2007 | | |
| | (c) Constant acceleration | 2001 | | |
| | (d) Seal | 1014 | | |
| | (1) Fine | | | |
| | (2) Gross | | | |
| | (e) Visual examination | | | |
| | (f) End point electrical parameters | | | |
| 5 | (a) Salt atmosphere | 1009 | 15 | D |
| | (b) Seal | 1014 | | |
| | (1) Fine | | | |
| | (2) Gross | | | |
| | (c) Visual examination | | | |
| 6 | (a) Internal water vapour content | 1018 | 5 | D |
| 7 | (a) Adhesion of lead finish | 2025 | 15 | D |
| 8 | (a) Lid torque | 2024 | 5 | D |

Generic test data may be used for Group D tests

**MIL-STD-883C Notice 4 Page 3 Clause 17**
'... Group C and D shall have been completed on date codes within 52 weeks **prior** to the date code of product being submitted for acceptance. Group D data shall be on the same package type....and from the same **plant** as the die represented.'
**MIL-M-38510F Page 5 Clause 3.1.3.12**
'Package type. A package type is a package which has the same **case outline, configuration**....(the physical shape of the case outline not including dimensions)...., **materials** (including bonding wire and die attach), **piece parts** (excluding preforms which differ only in size), and **assembly processes**.'

# Packaging and coding

## Lead finish

Devices will be supplied with the following lead finishes as standard:

| Package Type | Lead Finish (MIL-M-38510 3.5.6.3.2) |
|---|---|
| Metal Can (CM)<br>Sidebrazed Ceramic DIL (DC)<br>Leadless Chip Carrier (LC) | Gold plate over Nickel plate |
| Ceramic DIL (DG) | Hot solder dip over Tin plate |

## ESD protection

GEC Plessey Semiconductors considers all devices to be sensitive to electrostatic discharge to varying degrees (but at least to category A). All units are therefore marked with the equilateral triangle ESD sensitivity indicator.

In addition, all devices are packaged and shipped in conductive material or packaged in anti-static material with an external field shielding barrier in accordance MIL-M-38510.

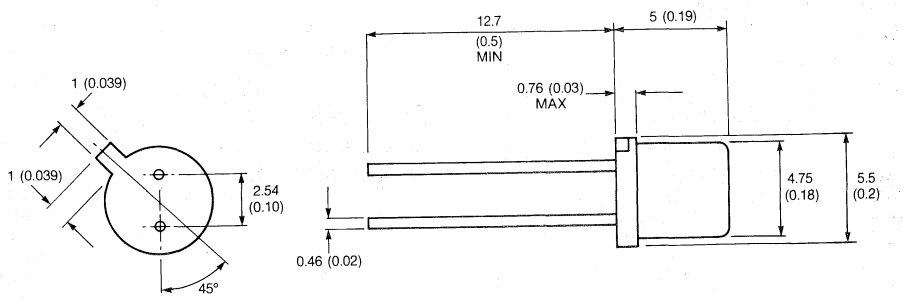
## Device marking

All devices are marked with the following coding:

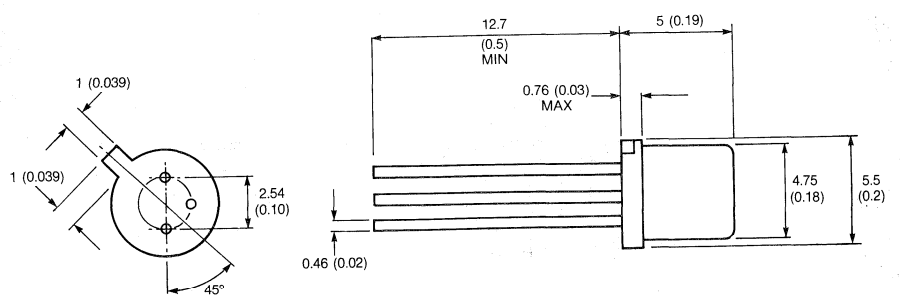
1. GPS logo or 'GPS' (manufacturer's identity).
2. ESD sensitivity indicator (equilateral triangle).
3. Date code (per MIL-M-38510).
4. Assembly lot identifier. Suffix letter added to date code indicating lot identity within production week.
5. Device type number - 'AC' indicating a MIL-STD-883C Class B compliant device.
6. Process/Assembly site identifier (two-letter code). Initial letter 'S' indicates GPS Swindon UK Wafer Process site. Second letter 'J' indicates GPS Swindon assembly site.
7. Pin 1 identifier. This may be either a package notch or dot for dual-in-line packages, gold corner for leadless chip carriers or tab for metal can packages.

# Section 6
## Package Outlines

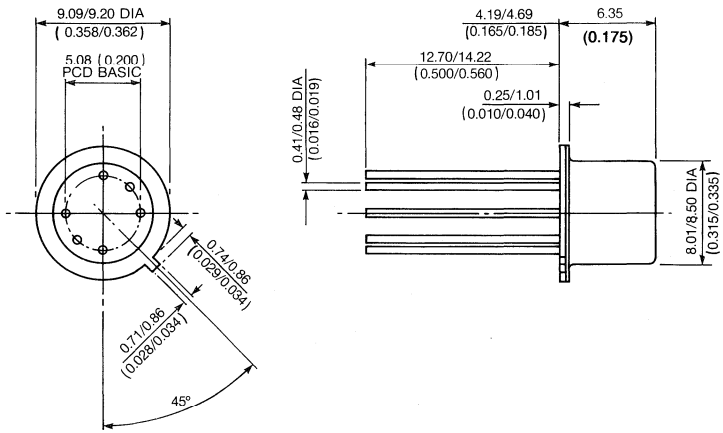
NOTE: On all package outlines, dimensions are shown thus: mm (in).



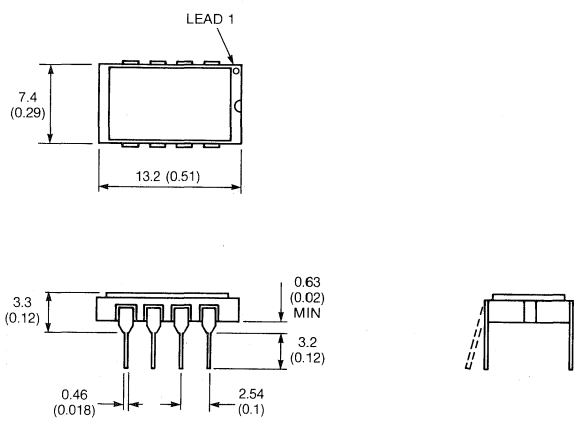

**2-LEAD METAL CAN - CM2**



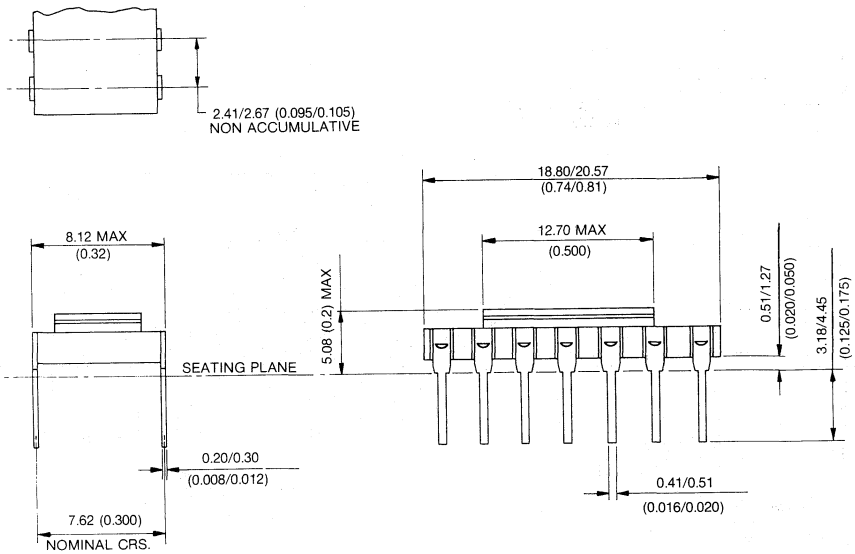

**3-LEAD METAL CAN - CM3**



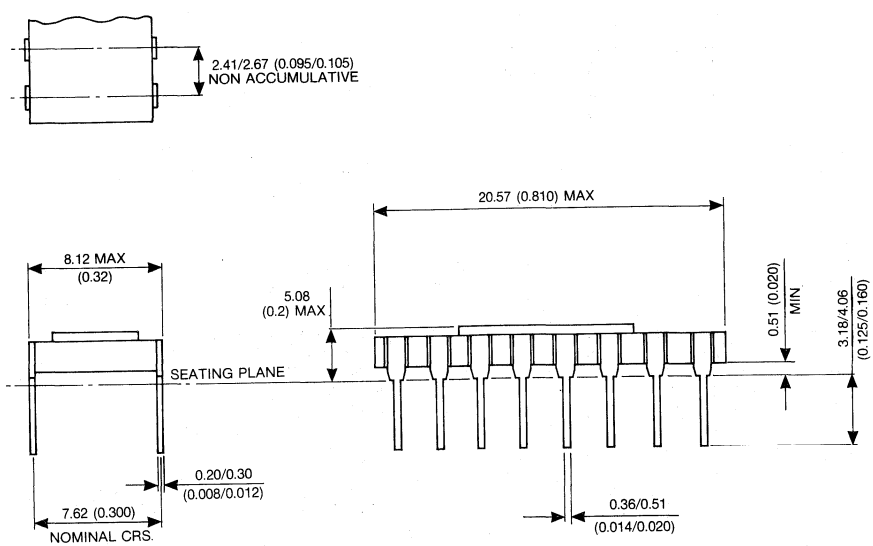

**6-LEAD METAL CAN - CM6**



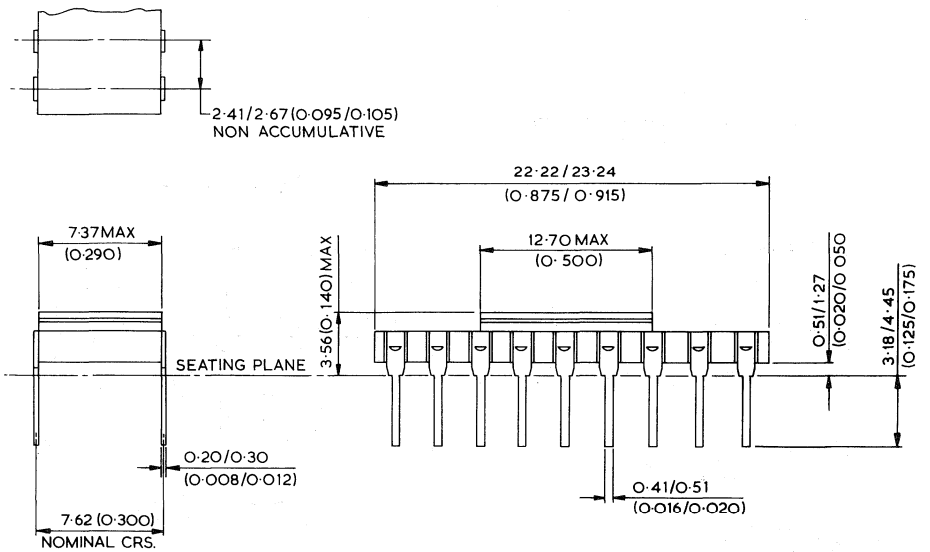

**8-LEAD SIDEBRAZED CERAMIC DIL - DC8**



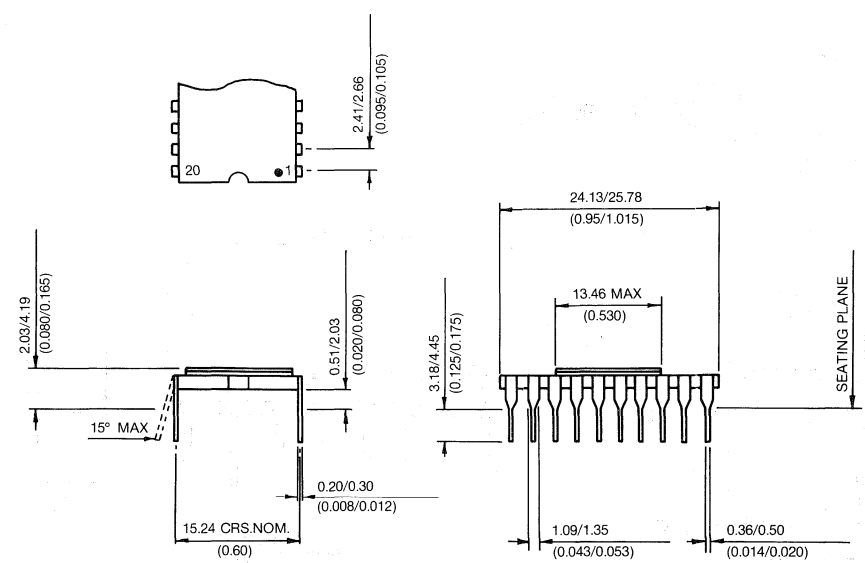

**14-LEAD SIDEBRAZED CERAMIC DIL - DC14**



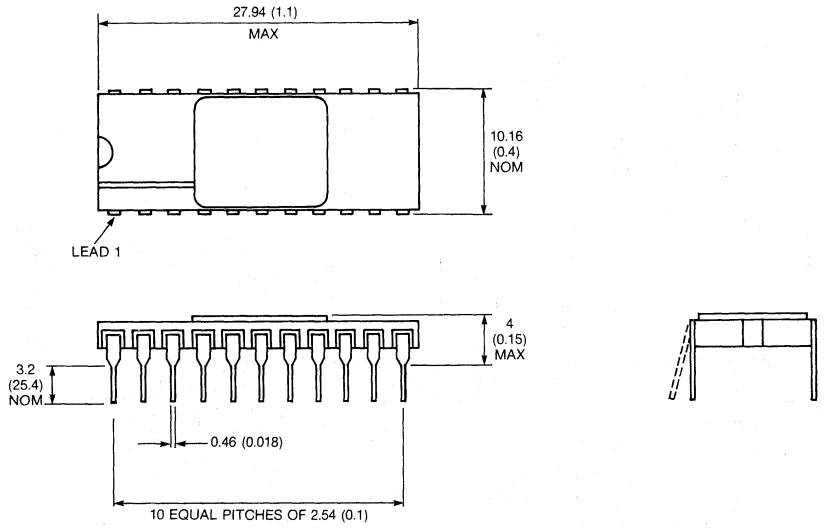

**16-LEAD SIDEBRAZED CERAMIC DIL - DC16**



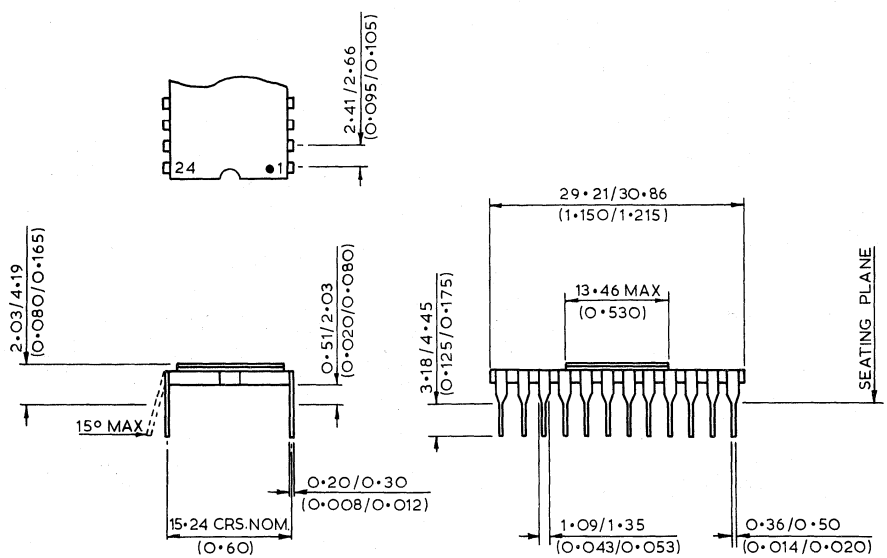

**18-LEAD SIDEBRAZED CERAMIC DIL - DC18**



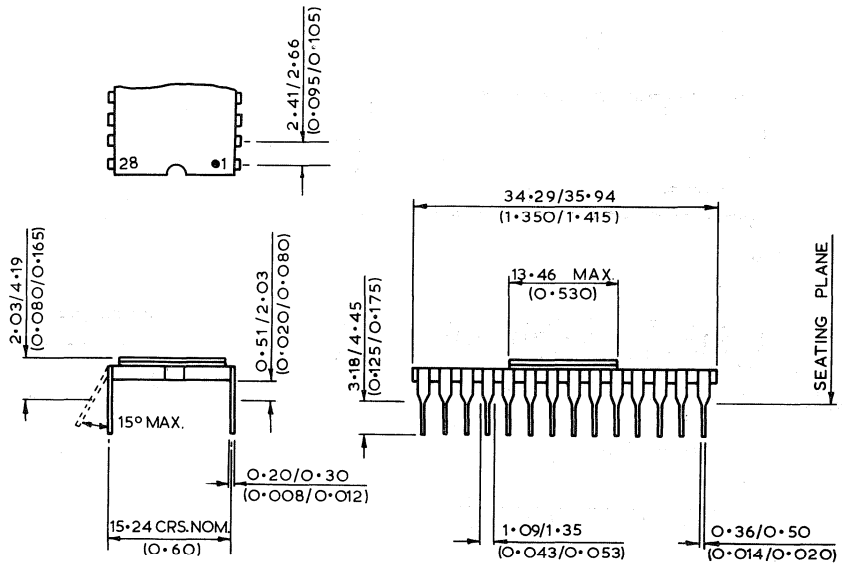

**20-LEAD SIDEBRAZED CERAMIC DIL - DC20**



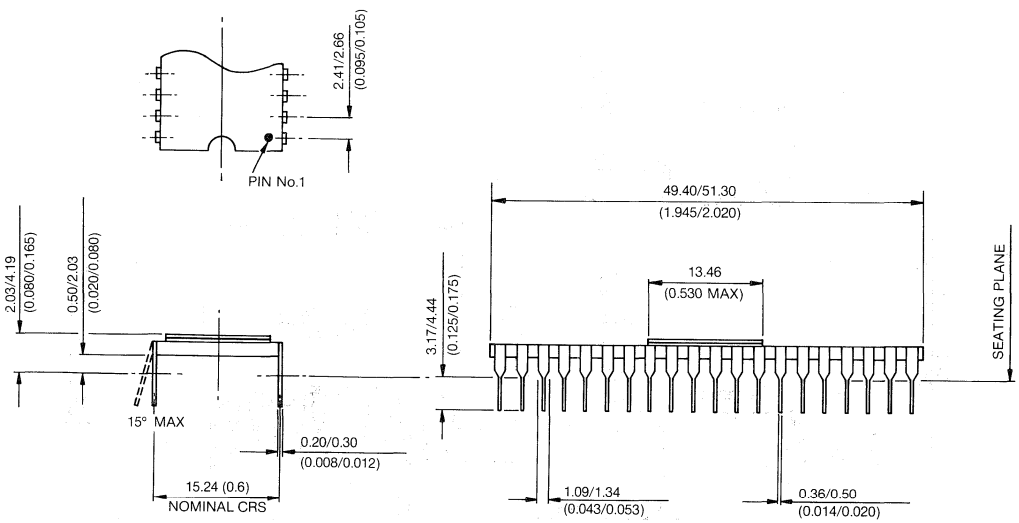

**22-LEAD SIDEBRAZED CERAMIC DIL - DC22**



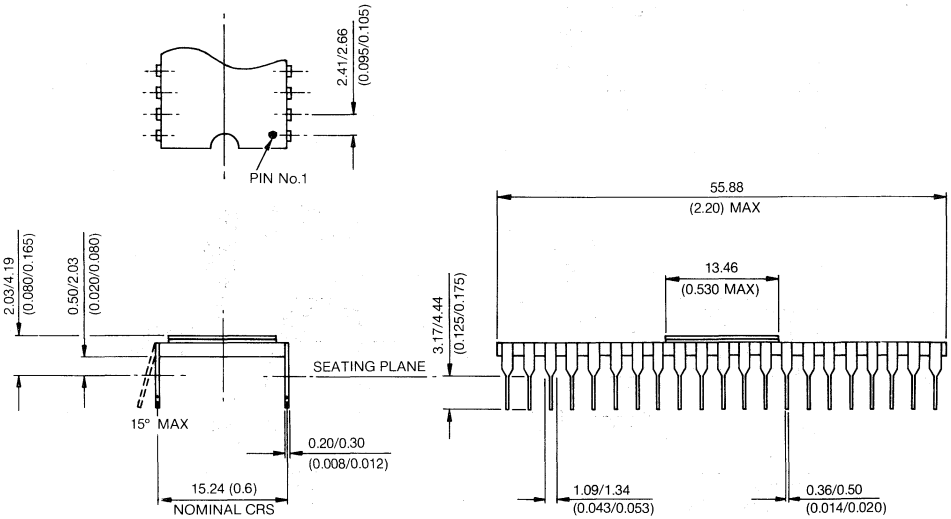

**24-LEAD SIDEBRAZED CERAMIC DIL - DC24**




**28-LEAD SIDEBRAZED CERAMIC DIL - DC28**




**40-LEAD SIDEBRAZED CERAMIC DIL - DC40**

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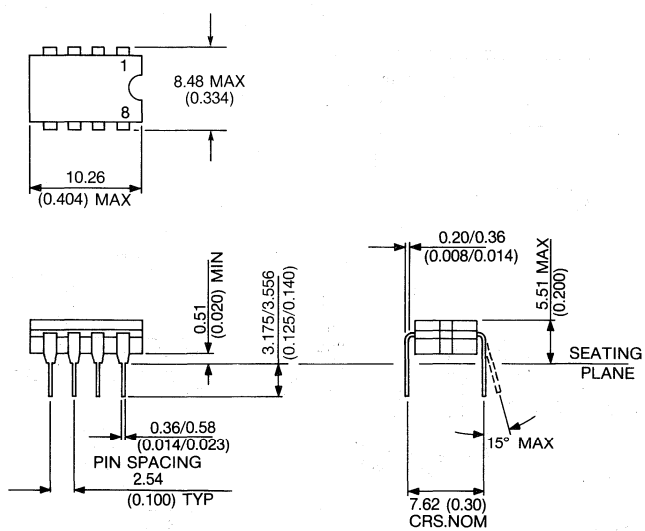
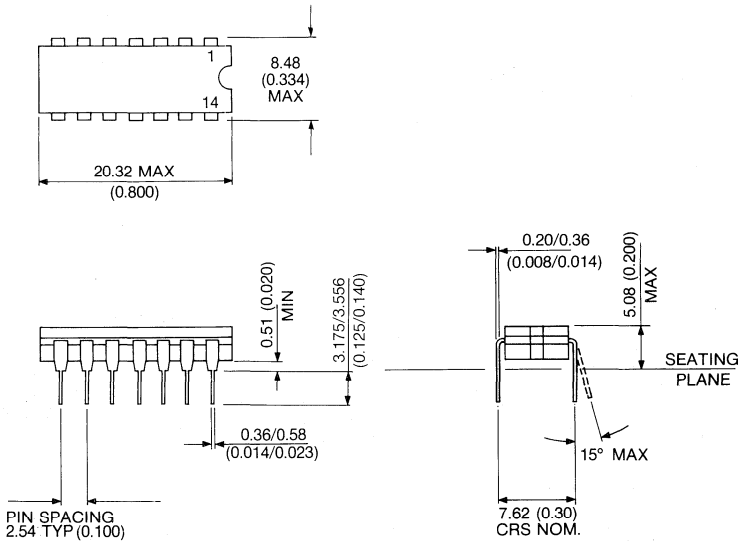



**8-LEAD CERAMIC DIL - DG8**

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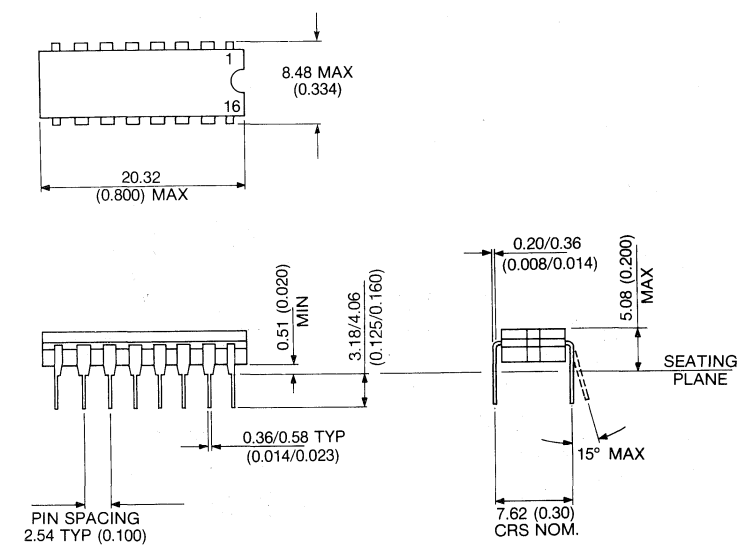


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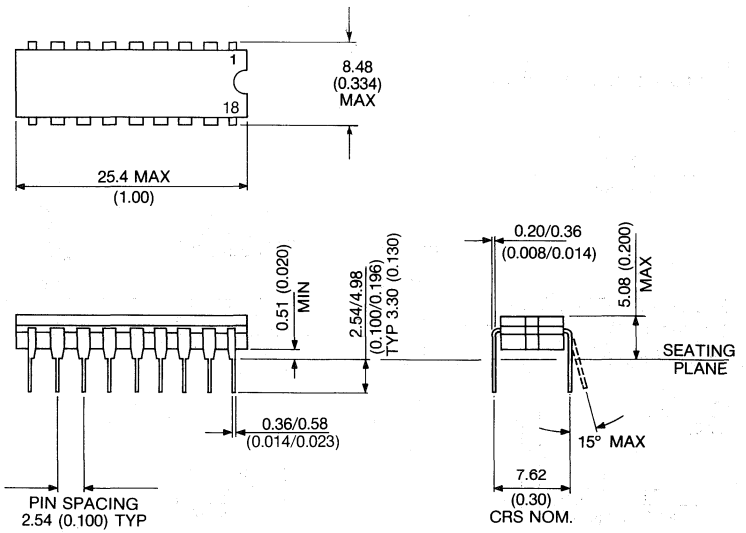


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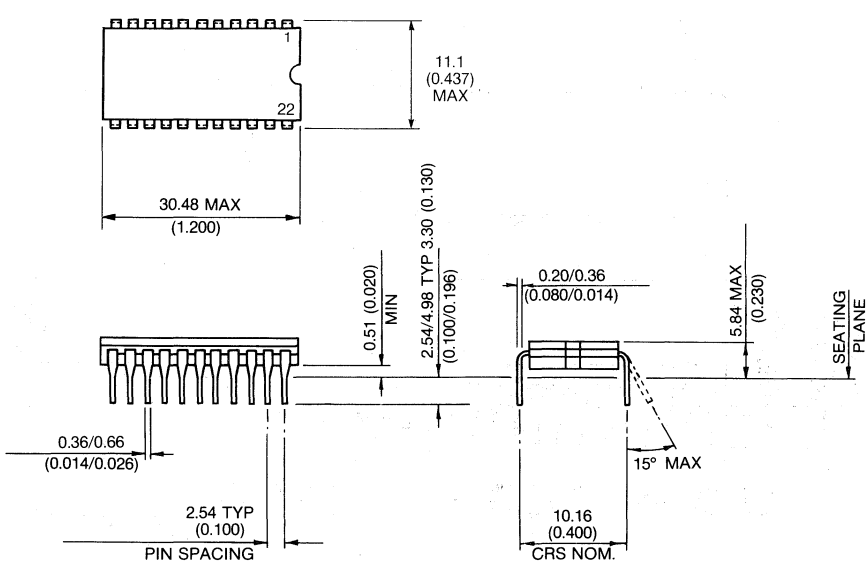
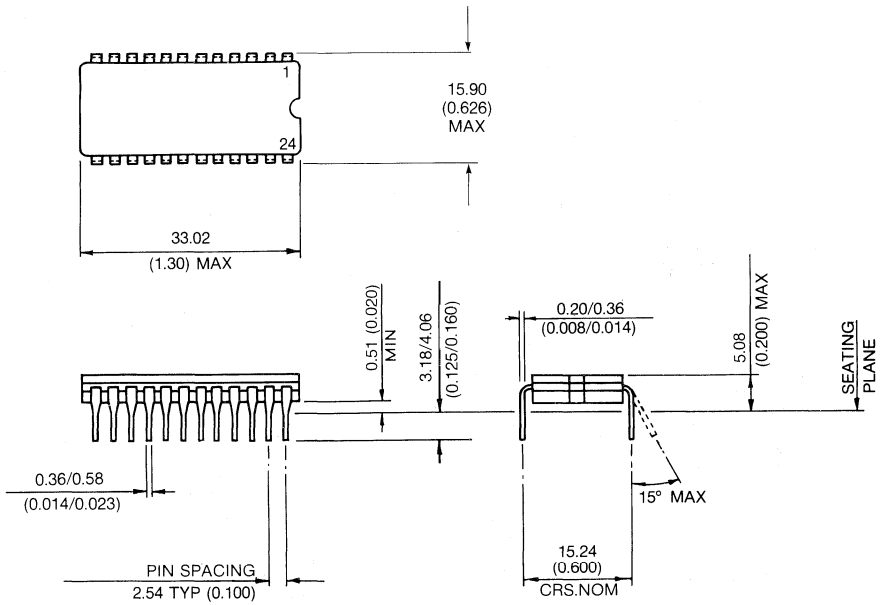
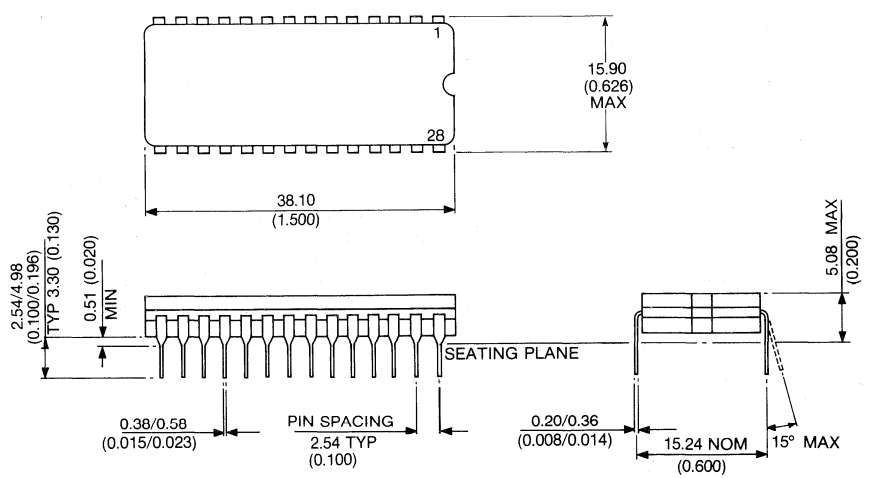


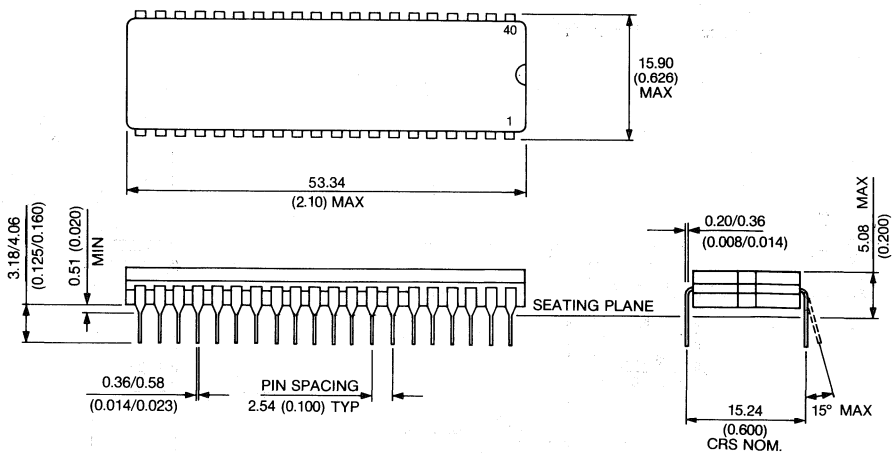

**22-LEAD CERAMIC DIL CERDIP - DG22**



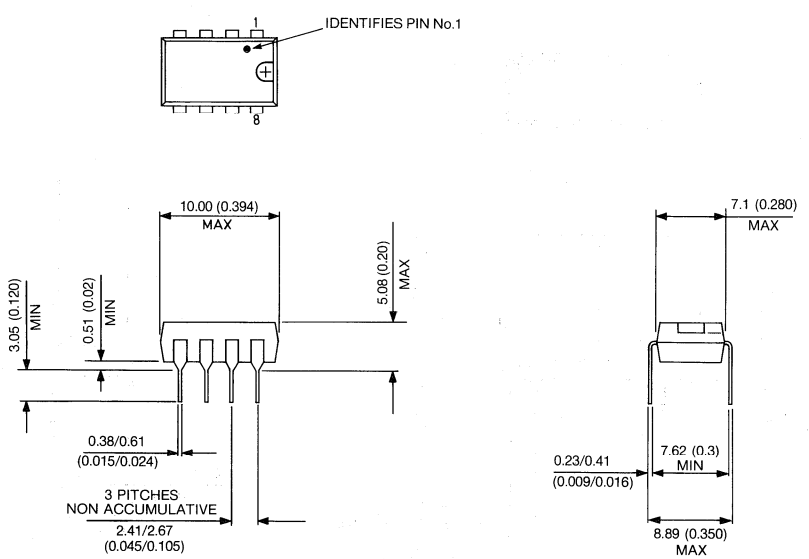

**24 LEAD CERAMIC DIL**
**CERDIP - DG24**



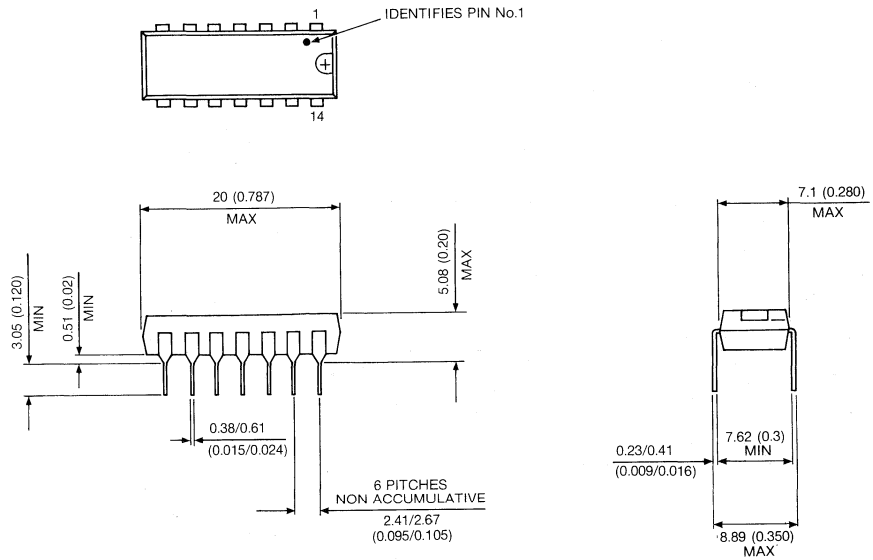

**28-LEAD CERAMIC DIL - DG28**




**40-LEAD CERAMIC DIL CERDIP - DG40**




**8-LEAD PLASTIC DIL - DP8**

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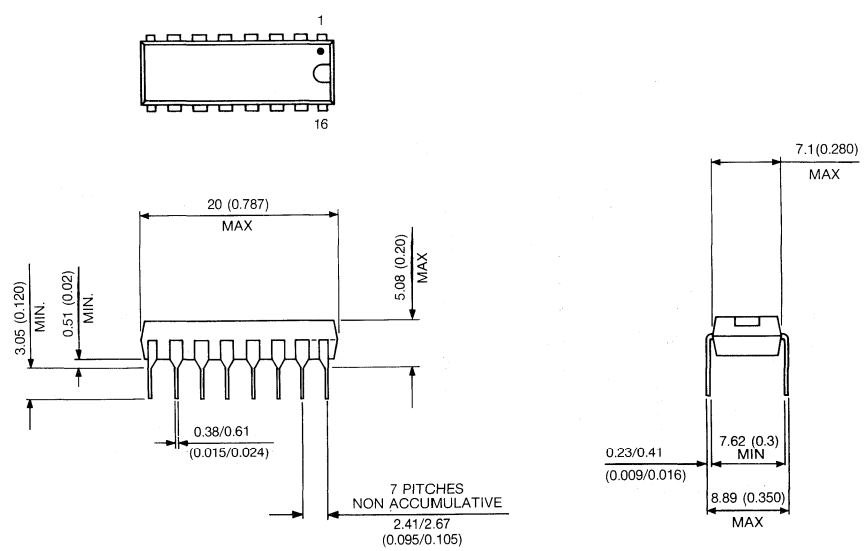
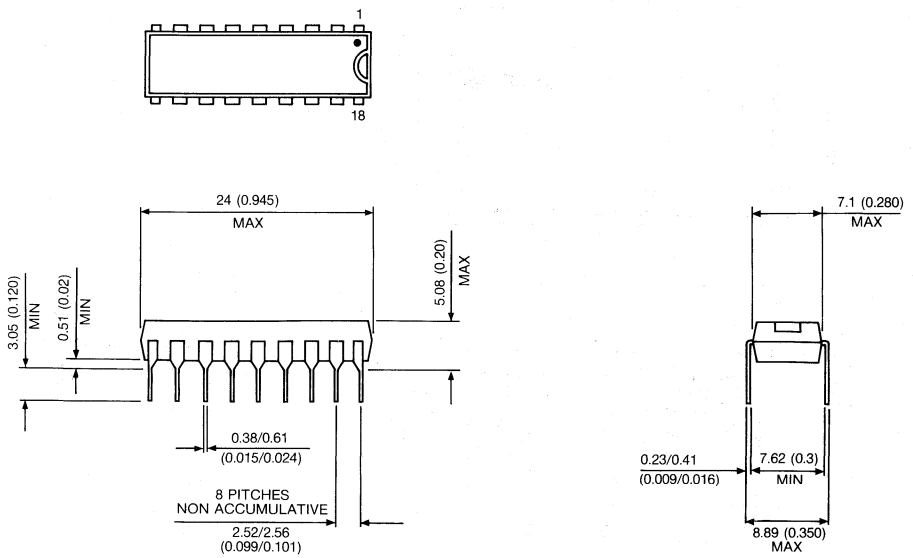
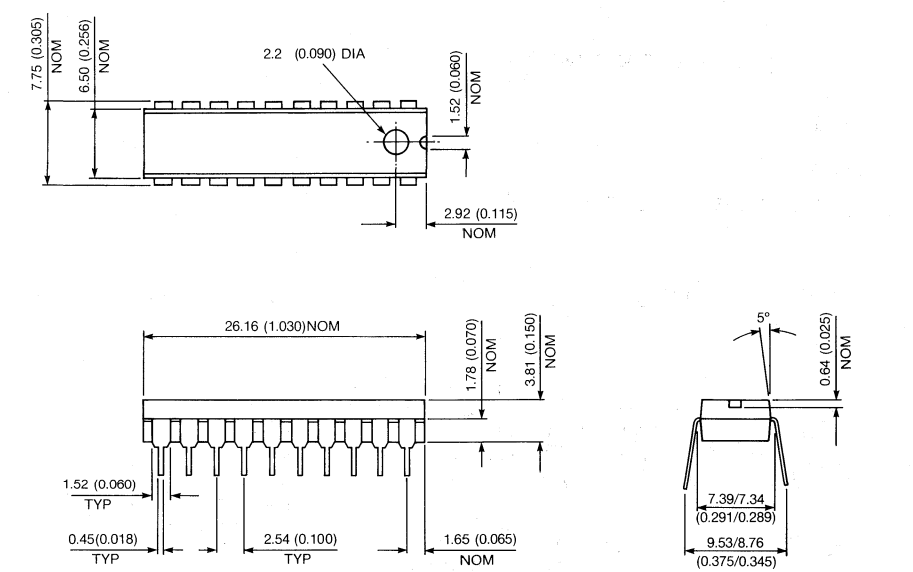


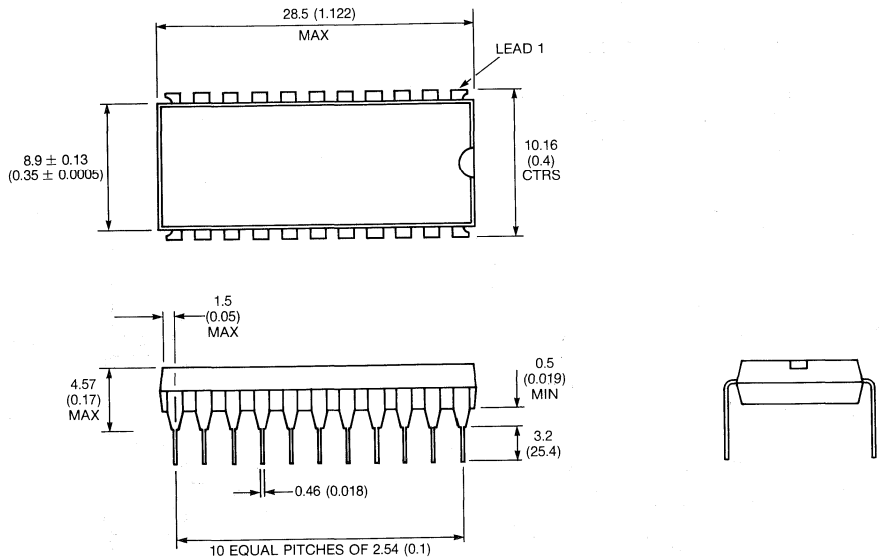

**16-LEAD PLASTIC DIL - DP16**



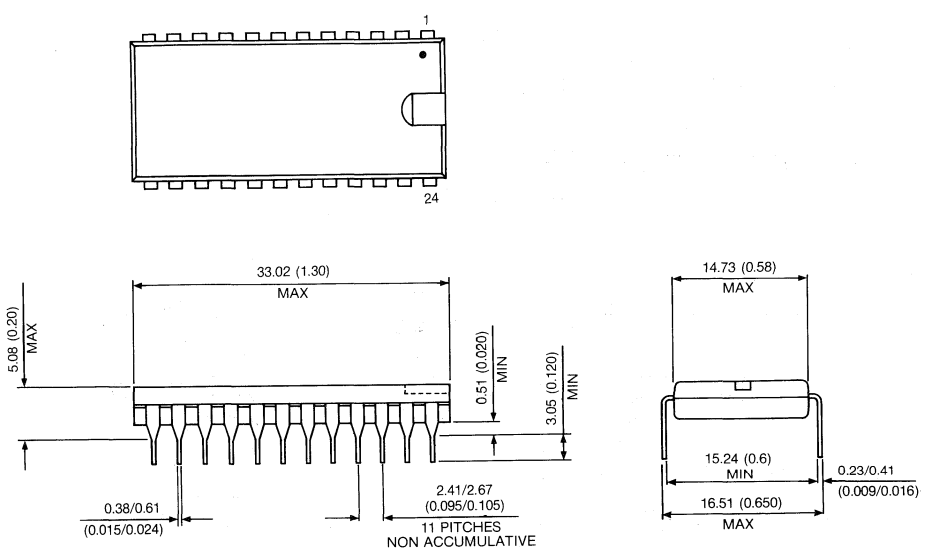

**18-LEAD PLASTIC DIL - DP18**




**20 LEAD PLASTIC DIL – DP20**




**22-LEAD PLASTIC - DP22**

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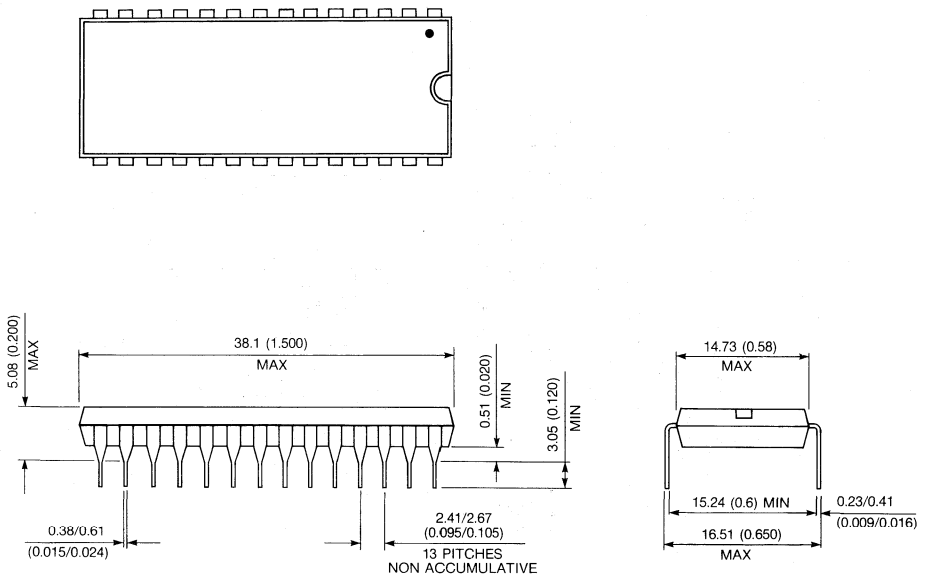


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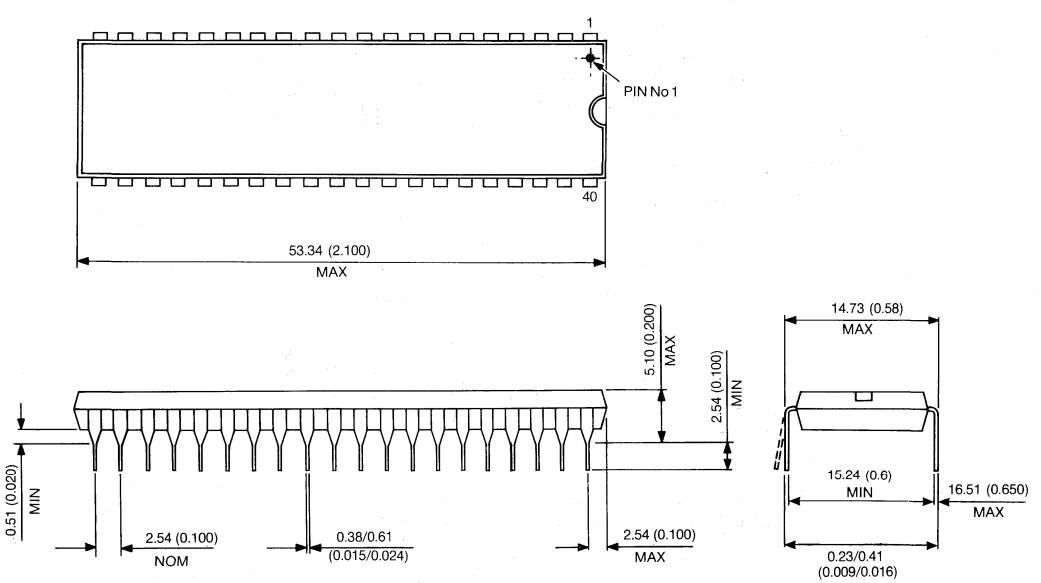


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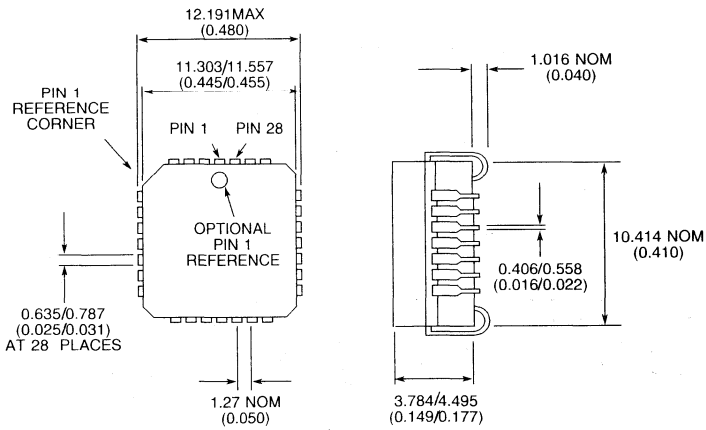
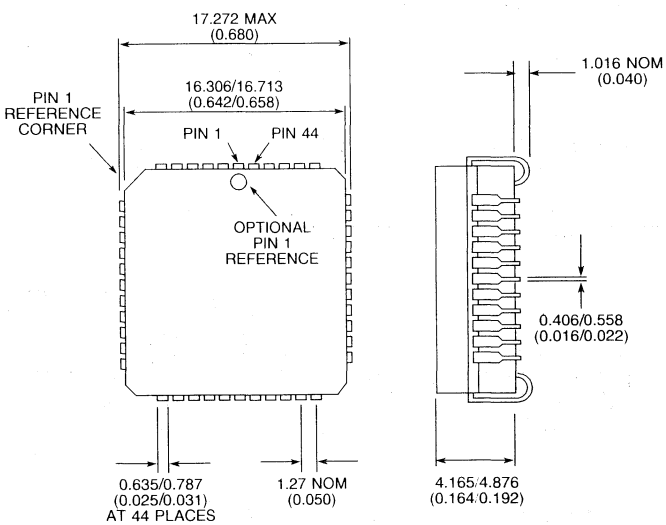
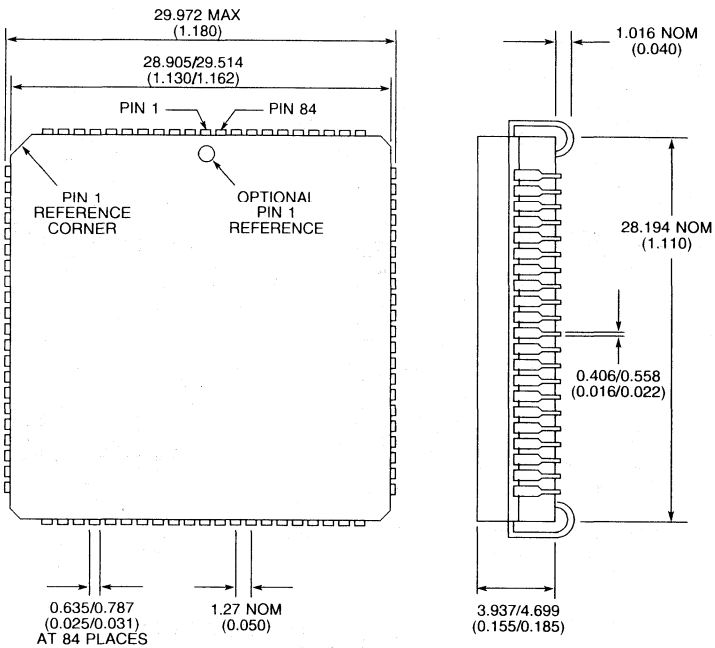


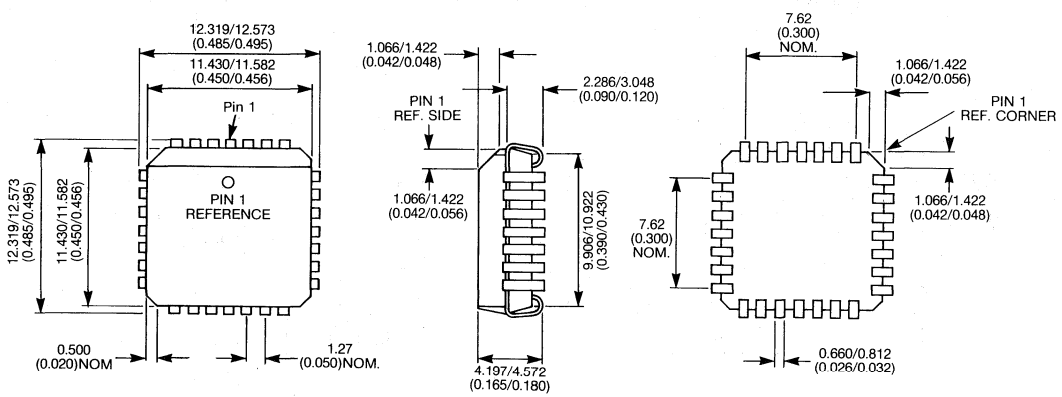

**28-LEAD QUAD CERPAC CHIP CARRIER - HG28**



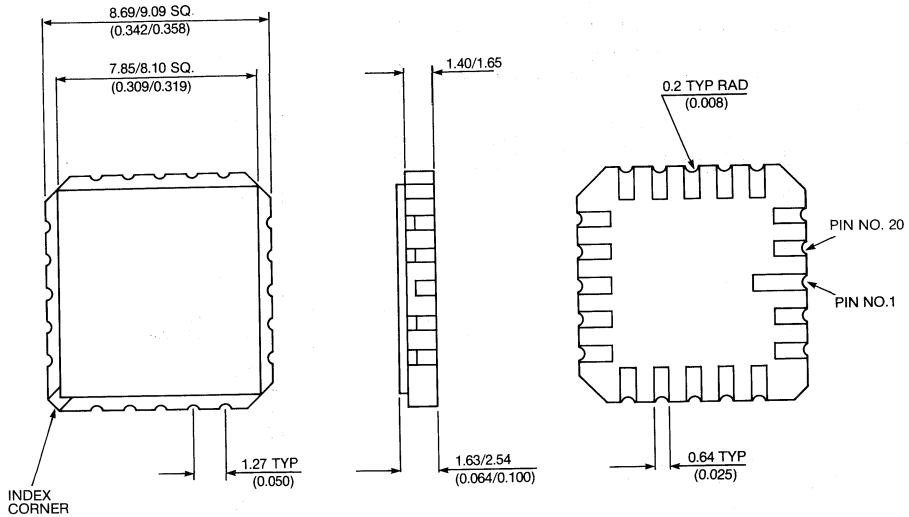

**44-LEAD QUAD CERPAC CHIP CARRIER - HG44**



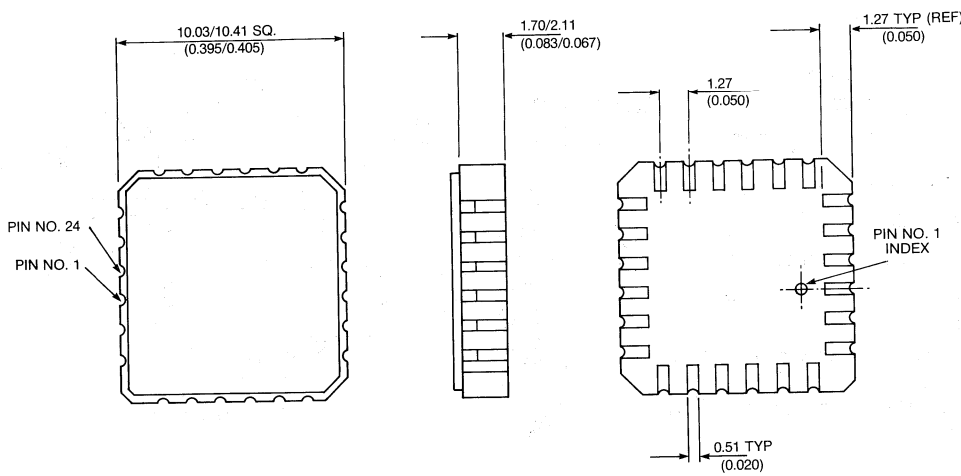

**84-LEAD QUAD CERPAC CHIP CARRIER - HG84**



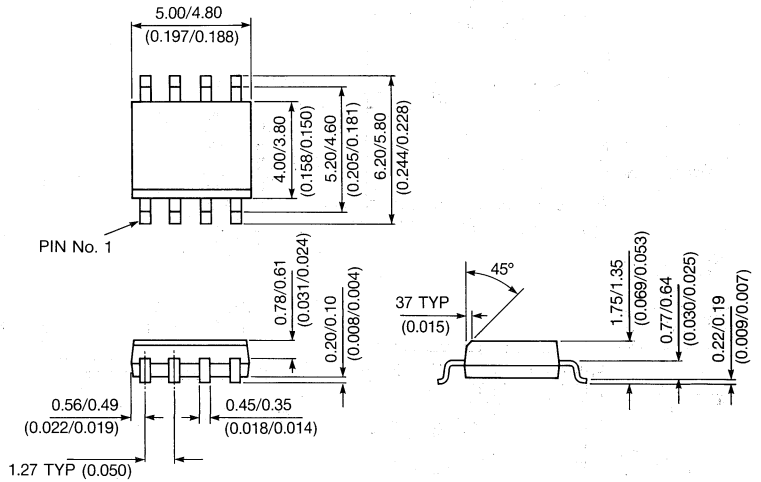

**28-LEAD QUAD PLASTIC J LEAD - HP28**



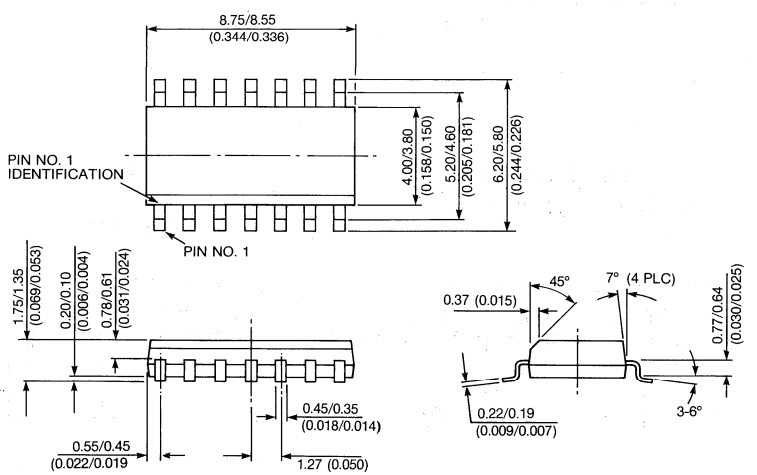

**20-PIN LEADLESS CHIP CARRIER - LC20**
**(HERMETIC)**



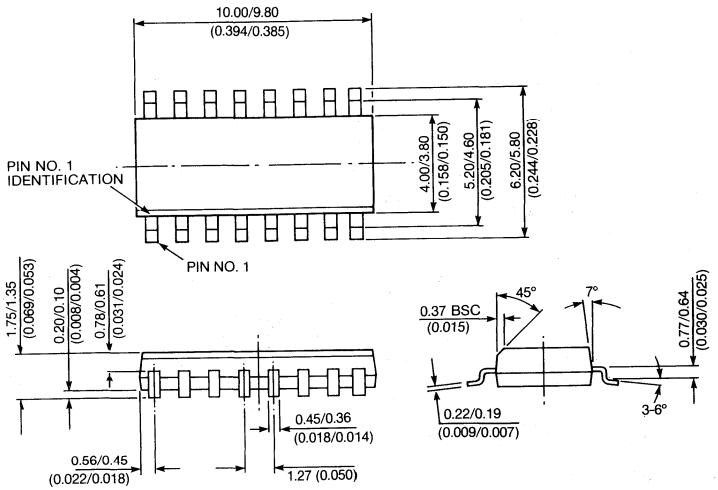

**24-PIN LEADLESS CHIP CARRIER - LC24**
**(HERMETIC)**




**8-LEAD MINIATURE PLASTIC DIL - MP8**




**14-LEAD MINIATURE PLASTIC DIL - MP14**

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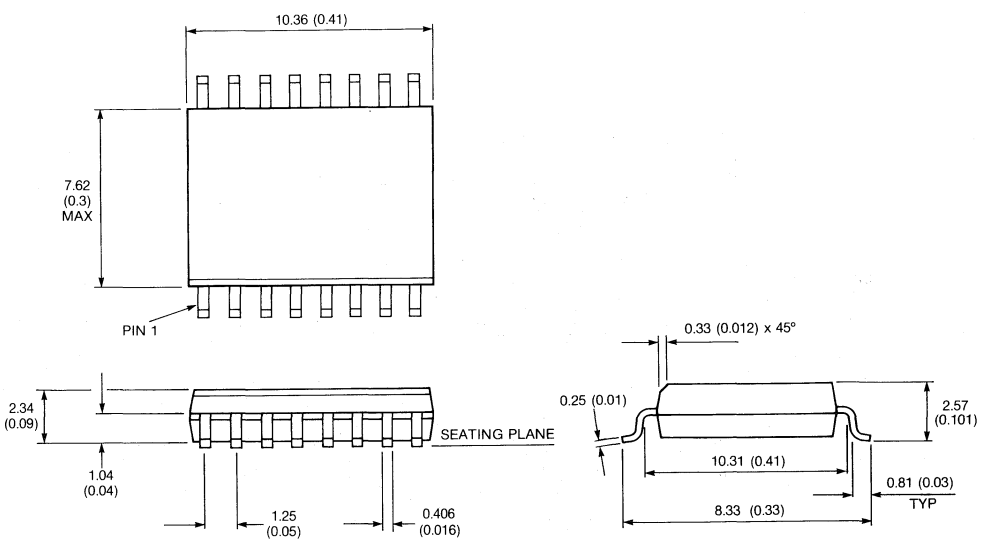
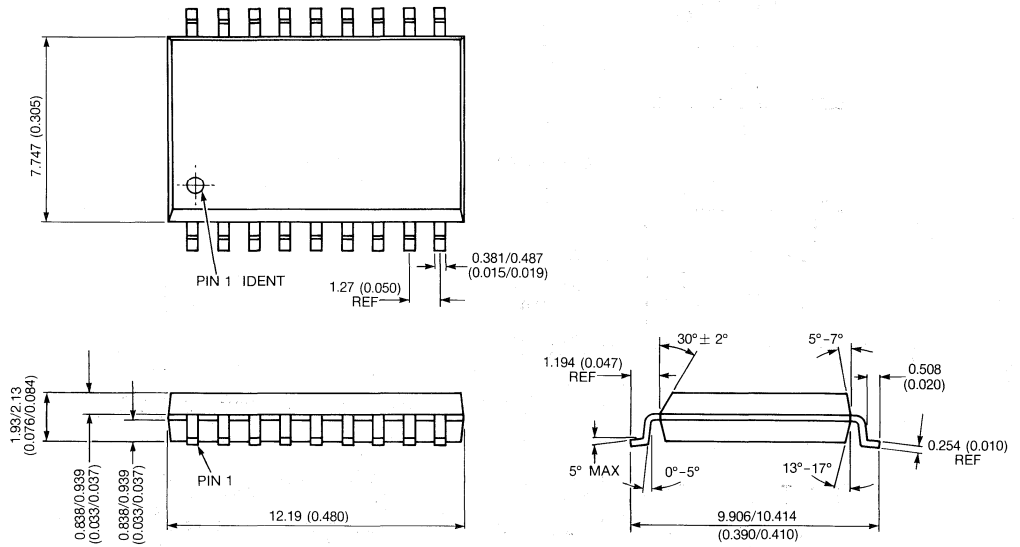



## 16-LEAD MINIATURE PLASTIC DIL - MP16/W (WIDE BODY)

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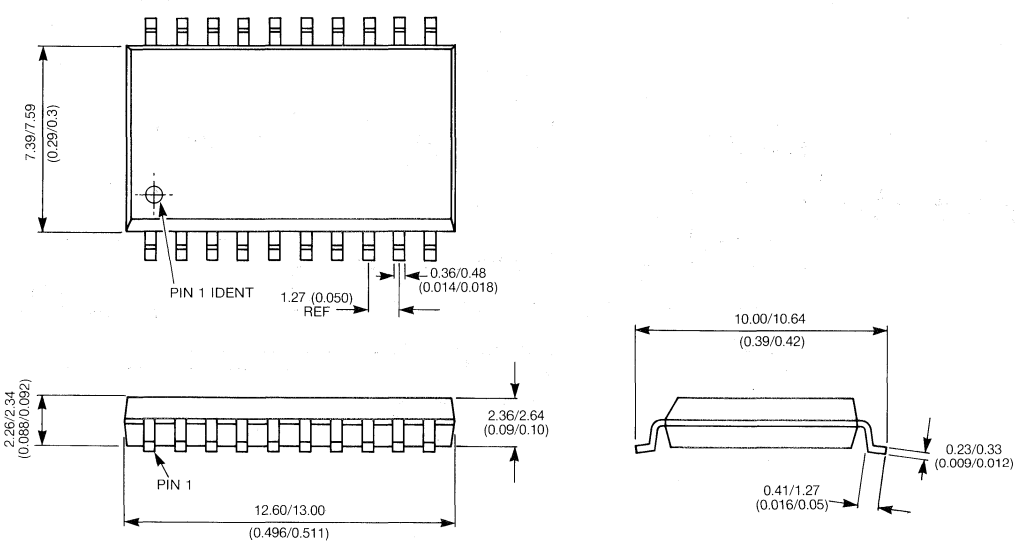
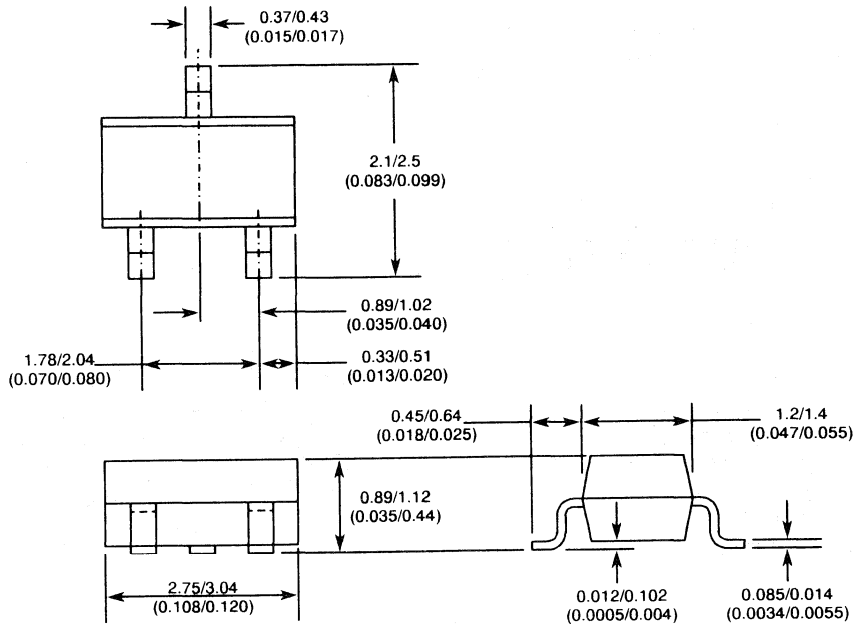
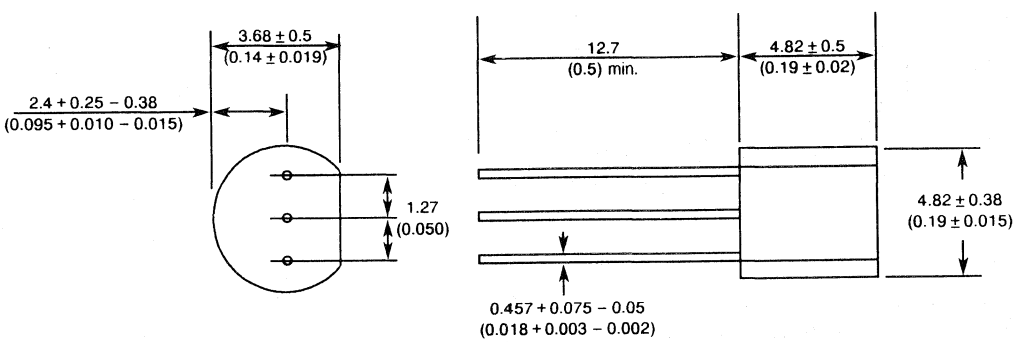



**20-LEAD MINIATURE PLASTIC DIL - MP20**




**3-PIN MINIATURE PLASTIC DIL - SOT-23**




**3-LEAD PLASTIC -TO-92**

# Section 7
## Locations

## HEADQUARTERS OPERATIONS

| | |
|---|---|
| UNITED KINGDOM | Cheney Manor, Swindon, Wiltshire SN2 2QW, United Kingdom.<br>Tel: (0793) 518000 Tx: 449637 Fax: 0793 518411. |
| NORTH AMERICA | Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, USA.<br>Tel:(408) 438 2900 ITT Telex: 4940840 Fax: (408) 438 5576 |

## CUSTOMER SERVICE CENTRES

| | |
|---|---|
| FRANCE & BENELUX | Z.A. Courtaboeuf, Miniparc-6, Avenue des Andes, Bat. 2-BP 142, 91944, Les Ulis Cedex A. France.<br>Tel: (1) 64 46 23 45 Fax: (1) 64 46 06 07 Tlx: 602 858 F. |
| GERMANY, AUSTRIA and SWITZERLAND | Ungererstraße 129, 8000 Munchen 40, Germany.<br>Tel: 089/36 0906-0. Fax: 089/360906-55 Tx: 523980. |
| ITALY | Viale Certosa, 49 20149 Milano. Tel: (02) 33 00 10 44/45. Fax: (GR3) 31 69 04. Tlx: 331347 |
| NORTH AMERICA | **Integrated Circuits**<br>Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066, USA.<br>Tel: (408) 438 2900 ITT Twx: 4940840 Fax: (408) 438 7023.<br>**Microwave and Hybrid Products**<br>160 Smith Street. Farmingdale, NY11735, USA. Tel: (516) 293 8636 Fax: (516) 293 0061. |
| SOUTH EAST ASIA | 152 Beach Road, #04-05 Gateway East, Singapore 0718.<br>Tel: 2919291. Fax: 2916455. |
| UNITED KINGDOM and SCANDINAVIA | Unit 1,Crompton Road,Groundwell Industrial Estate, Swindon, Wilts SN2 5AY, U.K.<br>Tel: (0793) 518510. Tx: 444410 Fax: (0793) 518582. |

## WORLD-WIDE AGENTS

| | |
|---|---|
| AUSTRALIA and NEW ZEALAND | **GEC Components Group.,** Electronic Division, 2 Giffnock Avenue, North Ryde, Sydney, New South Wales 2113, Australia.Tel: (2) 8876222. Tx: AA26080. Fax: (2) 8050272 |
| EASTERN EUROPE | **CTL Empexion Ltd..** Falcon House, 19 Deer Park Road, London SW19 3WX, U.K.<br>Tel: (081) 543 0911. Tx: 928472. Fax: (081) 540 0034.<br>**FA Bernhart GmbH,** Melkstattweg 27, PO Box 1628, D 8170 Bad Toelz., Germany. Tel: 80 41 41 676<br>Fax: 80 41 71 504 Tx: 526246 FABD. |
| HONG KONG | **YES Products Ltd.,** Block E, 15/F Golden Bear Industrial Centre, 66-82 Chaiwan Kolk Street,Tsuen Wan,<br>N.T. Hong Kong. Tel: 4144241-6. Tx: 36590. Fax: 4136078. |
| INDIA | **Mekaster Telecom PVT Ltd.,** 908 Ansal Bhawan, 16 Katuba Ghandi Marg, New Delhi, 100 001 India<br>Tel: 11 3312110 Fax: 11 3712155. |
| JAPAN | **Cornes & Company Ltd.,** Maruzen Building, 2-3-10 Nihonbashi, Chuo-ku. Tokyo 103.<br>Tel: 3 272 5771. Tx: 24874. Fax: 3 271 1479.<br>**Cornes & Company Ltd.,** 1-Chome Nishihonmachi, Nishi-Ku, Osaka 550.<br>Tel: 6 532 1012.Tx: 525-4496. Fax: 6 541-8850.<br>**Microtek Inc.,** Itoh Bldg, 7-9-17 Nishishinijuku. Tokyo 160. Tel: 3 371 1811. Tx: 27466. Fax: 3 369 5623. |
| KOREA | **KML Corporation,** 3rd Floor, Bang Bae Station Building, 981-15 Bang Bae, 3-Dong Shucho-Gu, Seoul, Korea,<br>CPO Box 7981. Tel: 2 588 2011/6. Tx: K25981. Fax: 2 588 2017. |
| MALAYSIA | **Adequip Enterprise Sdn Bhd,** #6-01 6th Floor, Wisjma Stephens, 88 Jalan Raya Chulan, 50200 Kualar Lumpur,<br>Malaysia. Tel: 2423522. Fax: 2423264. |
| SCANDINAVIA: Denmark | **Scansupply A/S,** 18-20 Nannasgade, DK-2200 Copenhagen N. Tel: 31 83 50 90. Tx: 19037. Fax: 31 83 25 40. |
| | **Scansupply A/S,** Marselisborg Havnevej 36, 8000 Arhus C. Tel: 45 86 12 77 88. Fax: 45 86 12 77 88. |
| Finland | **Oy Ferrado AB,** P.O.Box 54, SF-00381 Helsinki 38. Tel: 98 0550 002. Tx: 122214. Fax: 98 0551 117. |
| Norway | **Skandinavisk Elektronikk A/S,** Ostre Aker Vei 99, 0596 Oslo. Tel: 2 64 11 50. Tx: 71963 Fax: 2 643443. |
| TAIWAN | **King and King's Technology Ltd.,** 4, Alley 6, Lane 118, Ho Ping East Road. Taipei 10636. Taiwan, R.O.C.<br>Tel: 02-738-9145. Fax: 02-738-9146. |
| THAILAND | **Westech Electronics Co. Ltd,** 77/113 Moo Ban Kitikorn, Ladprao Soi 3, Ladprao Road, Ladyao, Jatujak,<br>Bangkok 10900. Thailand. Tel: 2 5125531. Fax: 2 2365949. |

## WORLD-WIDE DISTRIBUTORS

| | |
|---|---|
| AUSTRALIA | **GEC Components Group.,** Electronic Division, 2 Giffnock Avenue, North Ryde, Sydney, New South Wales 2113.<br>Tel: (2) 8876222. Tx: AA26080. Fax: (2) 8050272. |
| AUSTRIA | **Moor Lackner GmbH,** Lamezanstrasse 10, A-1230 Wien Tel: 222 610620. Tx: 135701. Fax: 222 61062151. |
| BELGIUM | **Heynen,** De Koelen 6, B-3530 Koutmalen. Tel: 011/52 57 57. Tx: 39047. Fax: 011/52 57 77.<br>**Tekelec Airtronic NV,** Bergensesteenweg 501, B-1500 Halle. Tel: 02 362 1288 Fax: 02 360 3807 |
| FRANCE | **Mateleco:**<br>**Ile de France**, 66 Avenue Augustin Dumont, 92240 Malakoff. Tel: 010 33 1 46 57 70 55. Tx: 203436.<br>**Rhône-Alpes**, 2, Rue Emile Zola, 38130 Echirolles. Tel: 010 33 76 40 38 33 Tx: 980837.<br>**ICC:**<br>**Bordeaux**, Rue de la Source, 33170 Gradignan. Tel: 56 31 17 17 Tx: 541539 Fax: 61 48 11 25.<br>**Clermont-Ferrand**, 2 bis, Avenue Fonmaure, 63400 Chamalières. Tel: 73 36 71 41 Tx: 990928.<br>**Marseille**, Z.A. Artizanord 11, 13015 Marseille. Tel: 91 03 12 12. Tx: 441313.<br>**Toulouse**, 78, Chemin Lanusse, 31200 Toulouse. Tel: 61 26 14 10. Tx: 520897. |

**CGE Composants SA:**
**Ile de France-6**, Avenue Maréchal-Juin - Z.I, Grange-Dame-Rose, 92363 Meudon La Forêt.
Tel: (1) 40 94 84 C0. Tx: 632253. Fax: (1) 46 30 01 29.
**Aquitaine**, Avenue Gustave Eiffel, 33605 Pessac Cedex. Tel: 56 36 40 40. Tx: 571224 F.
**Bretagne-9**, Rue du Général Nicolet, 35015 Rennes Cedex. Tel: 99 50 40 40 Tx: 740311 F.
**Centre/Pays-de-Loire**, Allée de la Détente, 86360 Chasseneuil du Poitou. Tel: 49 52 88 88. Tx: 791525 F.
**Est-27**, Rue Kleber, 68000 Colmar. Tel: 89 41 15 43. Tx: 870569 F.
**Midi-Pyrénées**, 55, Avenue Louis Breguet, 31400 Toulouse. Tel: 61 20 82 38. Tx: 530957 F.
**Nord**, 2 Rue de la Créativité, 59650 Villeneuve-d'Ascq. Tel: 20 67 04 04. Tx: 136887 F.
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| | Tweedale Way, Hollinwood, Oldham, Lancashire OL9 7LA. Tel: 061 682 6844. Tx: 666001. Fax:061 688 7898. |
| | Lincoln Industrial Park, Doddington Road, Lincoln LN6 3LF. Tel: 0522 500500 Tx: 56380. Fax (G2/G3): 0522 500550. |
| UNITED STATES OF AMERICA | Sequoia Research Park, 1500 Green Hills Road, Scotts Valley, California 95066. Tel: (408) 438 2900. ITT Twx: 4940840. Fax: (408) 438-5576. |
| | Two Dedham Place, Suite 1, Allied Drive, Dedham, Massachusetts 02026. Tel: 617/320-9790. Fax: 617/320-9383. |
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SEMICONDUCTORS

Marconi Electronic Devices Limited and Plessey Semiconductors Limited have been grouped together to form GEC Plessey Semiconductors.

However, until further notice, contracts, purchase orders, invoicing and payments should continue to be made to Marconi Electronic Devices Ltd and Plessey Semiconductors Ltd.